

# ANTREX Electronics

Electronic Components Sourcing Information

---

## Product Reference Information

**Part Number:** CYT4BB8CEBQ0AEEGS

**Manufacturer:** Infineon Technologies

**Package:** 176-LQFP Exposed Pad

**Availability:** Please confirm with sales

**Product Page:**

<https://antrexco.com/product/details/infineon-technologies/cyt4bb8cebq0aeegs.html>

**Request a Quote:**

[Submit RFQ for this part](#)



Scan for product page

## Contact Information

Email: [info@antrexco.com](mailto:info@antrexco.com)

WhatsApp: +86-186-8066-5326

Website: <https://antrexco.com>

## Quality & Trust

New & Original Components

Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

Secure sourcing support for OEM / EMS projects

### Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

# TRAVEO™ T2G 32-bit Automotive MCU

Based on Arm® Cortex®-M7 single/dual

## General description

CYT3BB/4BB is a family of TRAVEO™ T2G microcontrollers targeted at automotive systems such as high-end body-control units. CYT3BB/4BB has one or two Arm® Cortex®-M7 CPUs for primary processing, and an Arm® Cortex®-M0+ CPU for peripheral and security processing. These devices contain embedded peripherals supporting Controller Area Network with Flexible Data rate (CAN FD), Local Interconnect Network (LIN), and Ethernet. TRAVEO™ T2G devices are manufactured on an advanced 40-nm process. CYT3BB/4BB incorporates a low-power flash memory, multiple high-performance analog and digital peripherals, and enables the creation of a secure computing platform.

## Features

### • CPU subsystem

- One or two<sup>[1]</sup> 250-MHz 32-bit Arm® Cortex®-M7 CPUs, each with
  - Single-cycle multiply
  - Single/double-precision floating point unit (FPU)
  - 16-KB data cache, 16-KB instruction cache
  - Memory protection unit (MPU)
  - 16-KB instruction and 16-KB data tightly-coupled memories (TCM)
- 100-MHz 32-bit Arm® Cortex® M0+ CPU with
  - Single-cycle multiply
  - MPU
- Inter-processor communication in hardware
- Three DMA controllers
  - Peripheral DMA controller #0 (P-DMA0) with 100 channels
  - Peripheral DMA controller #1 (P-DMA1) with 58 channels
  - Memory DMA controller (M-DMA0) with 8 channels

### • Integrated memories

- 4160 KB of code-flash with an additional 256 KB of work-flash
  - Read-While-Write (RWW) allows updating the code-flash/work-flash while executing from it
  - Single- and dual-bank modes (specifically for Firmware update Over The Air [FOTA])
  - Flash programming through SWD/JTAG interface
- 768 KB of SRAM with selectable retention granularity

### • Cryptography engine

- Supports enhanced Secure Hardware Extension (eSHE) and Hardware Security Module (HSM)
- Secure boot and authentication
  - Using digital signature verification
  - Using fast secure boot
- AES: 128-bit blocks, 128-/192-/256-bit keys
- 3DES: 64-bit blocks, 64-bit key
- Vector unit supporting asymmetric key cryptography such as Rivest-Shamir-Adleman (RSA) and Elliptic Curve (ECC)
- SHA-1/2/3: SHA-512, SHA-256, SHA-160 with variable length input data
- CRC: supports CCITT CRC16 and IEEE-802.3 CRC32
- True random number generator (TRNG) and pseudo random number generator (PRNG)
- Galois/Counter Mode (GCM)

#### Note

1. Dual Cortex-M7 CPUs are supported in selected MPNs. For more information, refer to [Ordering information](#).

## Features

**• Functional safety for ASIL-B**

- Memory protection unit (MPU)
- Shared memory protection unit (SMPU)
- Peripheral protection unit (PPU)
- Watchdog timer (WDT)
- Multi-counter watchdog timer (MCWDT)
- Low-voltage detector (LVD)
- Brown-out detection (BOD)
- Over-voltage detection (OVD)
- Clock supervisor (CSV)
- Hardware error correction (SECDED ECC) on all safety-critical memories (SRAM, flash, TCM)

**• Low-power 2.7-V to 5.5-V operation**

- Low-power Active, Sleep, Low-power Sleep, DeepSleep, and Hibernate modes for fine-grained power management
- Configurable options for robust BOD
  - Two threshold levels (2.7 V and 3.0 V) for BOD on  $V_{DD}$  and  $V_{DDA}$
  - One threshold level (1.1 V) for BOD on  $V_{CCD}$

**• Wakeup**

- Up to two pins to wake from Hibernate mode
- Up to 220 GPIO pins to wake from Sleep modes
- Event Generator, SCB, Watchdog Timer, RTC alarms to wake from DeepSleep modes

**• Clocks**

- Internal main oscillator (IMO)
- Internal low-speed oscillator (ILO)
- External crystal oscillator (ECO)
- Watch crystal oscillator (WCO)
- Phase-locked loop (PLL)
- Frequency-locked loop (FLL)

**• Communication interfaces**

- Up to eight CAN FD channels
  - Increased data rate (up to 8 Mbps) compared to classic CAN, limited by physical layer topology and transceivers
  - Compliant with ISO 11898-1:2015
  - Supports all the requirements of Bosch CAN FD Specification V1.0 for non-ISO CAN FD
  - ISO 16845:2015 certificate available
- Up to 11 runtime-reconfigurable serial communication block (SCB) channels, each configurable as I<sup>2</sup>C, SPI, or UART
- Up to 16 independent LIN channels
  - LIN protocol compliant with ISO 17987
- One 10/100 Mbps Ethernet MAC interface conforming to IEEE-802.3bw
  - Supports the following PHY interfaces:
    - Media-independent interface (MII)
    - Reduced media-independent interface (RMII)
  - Compliant with IEEE-802.1BA Audio Video Bridging (AVB)
  - Compliant with IEEE-1588 Precision Time Protocol (PTP)

---

**Features****• External memory interface**

- One SPI (Single, Dual, Quad, or Octal) or HYPERBUS™ interface
- On-the-fly encryption and decryption
- Execute-in-place (XIP) from external memory

**• SDHC interface**

- One Secure Digital High Capacity (SDHC) interface supporting embedded MultiMediaCard (eMMC), Secure Digital (SD), or Secure Digital Input Output (SDIO)
  - Compliant with eMMC 5.1, SD 6.0, and SDIO 4.10 specifications
- Data rates up to SD High Speed 50 MHz, or eMMC 52-MHz DDR

**• Audio interface**

- Three inter-IC sound (I<sup>2</sup>S) interfaces for connecting digital audio devices
- I<sup>2</sup>S, left justified, or time division multiplexed (TDM) audio formats
- Independent transmit or receive operation, each in master or slave mode

**• Timers**

- Up to 75 16-bit and eight 32-bit timer/counter pulse-width modulator (TCPWM) blocks
  - Up to 12 16-bit counters for motor control
  - Up to 63 16-bit counters and eight 32-bit counters for regular operations
  - Supports timer, capture, quadrature decoding, pulse-width modulation (PWM), PWM with dead time (PWM\_DT), pseudo-random PWM (PWM\_PR), and shift-register (SR) modes
- Up to 16 Event Generation (EVTGEN) timers supporting cyclic wakeup from DeepSleep
  - Events trigger a specific device operation (such as execution of an interrupt handler, a SAR ADC conversion, and so on)

**• Real time clock (RTC)**

- Year/Month/Date, Day-of-week, Hour:Minute:Second fields
- 12- and 24-hour formats
- Automatic leap-year correction

**• I/O**

- Up to 220 programmable I/Os
- Three I/O types
  - GPIO Standard (GPIO\_STD)
  - GPIO Enhanced (GPIO\_ENH)
  - High-Speed I/O Standard (HSIO\_STD)

**• Regulators**

- Generates a 1.1-V nominal core supply from a 2.7-V to 5.5-V input supply
- Three regulators:
  - DeepSleep
  - Core internal
  - Core external

**• Programmable analog**

- Three SAR A/D converters with up to 75 external channels (72 I/Os + 3 I/Os for motor control)
  - ADC0 supports 32 logical channels, with 32 + 1 physical connections
  - ADC1 supports 32 logical channels, with 32 + 1 physical connections
  - ADC2 supports 8 logical channels, with 8 + 1 physical connections
  - Any external channel can be connected to any logical channel in the respective SAR
- Each ADC supports 12-bit resolution and sampling rates of up to 1 Msps
- Each ADC also supports six internal analog inputs like
  - Bandgap reference to establish absolute voltage levels

### Features

- Calibrated diode for junction temperature calculations
- Two AMUXBUS inputs and two direct connections to monitor supply levels
- Each ADC supports addressing of external multiplexers
- Each ADC has a sequencer supporting autonomous scanning of configured channels
- Synchronized sampling of all ADCs for motor-sense applications
- **Smart I/O**
  - Up to five Smart I/O blocks, which can perform Boolean operations on signals going to and from I/Os
  - Up to 36 I/Os (GPIO\_STD) supported
- **Debug interface**
  - JTAG controller and interface compliant to IEEE-1149.1-2001
  - Arm® serial wire debug (SWD) port
  - Supports Arm® Embedded Trace Macrocell (ETM) Trace
    - Data trace using SWD
    - Instruction and data trace using JTAG
- **Compatible with industry-standard tools**
  - GHS MULTI or IAR EWARM for code development and debugging
- **Packages**
  - 100-TEQFP, 14 × 14 × 1.6 mm (max), 0.5-mm lead pitch
  - 144-TEQFP, 20 × 20 × 1.6 mm (max), 0.5-mm lead pitch
  - 176-TEQFP, 24 × 24 × 1.6 mm (max), 0.5-mm lead pitch
  - 272-BGA, 16 × 16 × 1.7 mm (max), 0.8-mm ball pitch

## Contents

|                                                          |           |
|----------------------------------------------------------|-----------|
| <b>General description .....</b>                         | <b>1</b>  |
| <b>Features .....</b>                                    | <b>1</b>  |
| <b>Contents.....</b>                                     | <b>5</b>  |
| <b>1 Features list .....</b>                             | <b>7</b>  |
| 1.1 Communication peripheral instance list .....         | 9         |
| <b>2 Blocks and functionality .....</b>                  | <b>10</b> |
| 2.1 Block diagram .....                                  | 10        |
| <b>3 Functional description .....</b>                    | <b>11</b> |
| 3.1 CPU subsystem .....                                  | 11        |
| 3.1.1 CPU .....                                          | 11        |
| 3.1.2 DMA controllers.....                               | 11        |
| 3.1.3 Flash .....                                        | 11        |
| 3.1.4 SRAM .....                                         | 11        |
| 3.1.5 ROM .....                                          | 11        |
| 3.1.6 Cryptography accelerator for security.....         | 11        |
| 3.2 System resources.....                                | 12        |
| 3.2.1 Power system .....                                 | 12        |
| 3.2.2 Regulators .....                                   | 12        |
| 3.2.3 Clock system .....                                 | 14        |
| 3.2.4 Reset .....                                        | 15        |
| 3.2.5 Watchdog timer.....                                | 15        |
| 3.2.6 Power modes .....                                  | 15        |
| 3.3 Peripherals .....                                    | 16        |
| 3.3.1 Peripheral clock dividers .....                    | 16        |
| 3.3.2 Peripheral protection unit.....                    | 16        |
| 3.3.3 12-bit SAR ADC .....                               | 16        |
| 3.3.4 Timer/counter/PWM block (TCPWM) .....              | 17        |
| 3.3.5 Serial communication blocks (SCB).....             | 17        |
| 3.3.6 CAN FD .....                                       | 18        |
| 3.3.7 Local interconnect network (LIN) .....             | 18        |
| 3.3.8 Ethernet MAC.....                                  | 18        |
| 3.3.9 External memory interface.....                     | 18        |
| 3.3.10 SDHC interface .....                              | 18        |
| 3.3.11 Audio interface.....                              | 19        |
| 3.3.12 One-time-programmable (OTP) eFuse .....           | 19        |
| 3.3.13 Event generator .....                             | 19        |
| 3.3.14 Trigger multiplexer .....                         | 19        |
| 3.4 I/Os.....                                            | 19        |
| 3.4.1 Port nomenclature.....                             | 19        |
| 3.4.2 GPIO Standard (GPIO_STD) .....                     | 20        |
| 3.4.3 GPIO Enhanced (GPIO_ENH) .....                     | 20        |
| 3.4.4 HSIO Standard (HSIO_STD) .....                     | 20        |
| 3.4.5 Smart I/O .....                                    | 20        |
| <b>4 CYT3BB/4BB address map .....</b>                    | <b>21</b> |
| <b>5 Flash base address map.....</b>                     | <b>23</b> |
| <b>6 Peripheral I/O map.....</b>                         | <b>24</b> |
| <b>7 CYT3BB/4BB clock diagram .....</b>                  | <b>26</b> |
| <b>8 CYT3BB/4BB CPU start-up sequence .....</b>          | <b>27</b> |
| <b>9 Pin assignment .....</b>                            | <b>28</b> |
| <b>10 High-speed I/O matrix connections .....</b>        | <b>35</b> |
| <b>11 Package pin list and alternate functions .....</b> | <b>36</b> |

|                                                            |            |
|------------------------------------------------------------|------------|
| <b>12 Power pin assignments</b>                            | <b>45</b>  |
| <b>13 Alternate function pin assignments</b>               | <b>46</b>  |
| 13.1 Pin function description                              | 54         |
| <b>14 Interrupts and wake-up assignments</b>               | <b>56</b>  |
| <b>15 Core interrupt types</b>                             | <b>66</b>  |
| <b>16 Trigger multiplexer</b>                              | <b>67</b>  |
| <b>17 Triggers group inputs</b>                            | <b>69</b>  |
| <b>18 Triggers group outputs</b>                           | <b>73</b>  |
| <b>19 Triggers one-to-one</b>                              | <b>74</b>  |
| <b>20 Peripheral clocks</b>                                | <b>79</b>  |
| <b>21 Faults</b>                                           | <b>82</b>  |
| <b>22 Peripheral protection unit fixed structure pairs</b> | <b>85</b>  |
| <b>23 Bus masters</b>                                      | <b>99</b>  |
| <b>24 Miscellaneous configuration</b>                      | <b>100</b> |
| <b>25 Development support</b>                              | <b>102</b> |
| 25.1 Documentation                                         | 102        |
| 25.1.1 Software user guide                                 | 102        |
| 25.1.2 Technical reference manual                          | 102        |
| 25.2 Tools                                                 | 102        |
| <b>26 Electrical specifications</b>                        | <b>103</b> |
| 26.1 Absolute maximum ratings                              | 103        |
| 26.2 Device-level specifications                           | 110        |
| 26.3 DC specifications                                     | 111        |
| 26.4 Reset specifications                                  | 116        |
| 26.5 I/O                                                   | 117        |
| 26.6 Analog peripherals                                    | 123        |
| 26.6.1 SAR ADC                                             | 123        |
| 26.6.2 Calculating the impact of neighboring pins          | 124        |
| 26.6.3 Voltage divider accuracy                            | 128        |
| 26.7 AC specifications                                     | 129        |
| 26.8 Digital peripherals                                   | 130        |
| 26.9 Memory                                                | 140        |
| 26.10 System resources                                     | 142        |
| 26.10.1 SWD interface                                      | 152        |
| 26.11 Clock specifications                                 | 154        |
| 26.12 Clock timing diagrams                                | 161        |
| 26.13 Ethernet specifications                              | 163        |
| 26.14 SDHC specifications                                  | 166        |
| 26.15 Audio subsystem specifications                       | 171        |
| 26.16 Serial memory interface specifications               | 175        |
| <b>27 Ordering information</b>                             | <b>182</b> |
| 27.1 Part number nomenclature                              | 183        |
| <b>28 Packaging</b>                                        | <b>185</b> |
| <b>29 Appendix</b>                                         | <b>190</b> |
| 29.1 Bootloading or End-of-line (EoL) Programming          | 190        |
| 29.2 External IP revisions                                 | 191        |
| <b>30 Acronyms</b>                                         | <b>192</b> |
| <b>31 Errata</b>                                           | <b>194</b> |
| <b>Revision history</b>                                    | <b>199</b> |

# 1 Features list

**Table 1-1 CYT3BB/4BB feature list for all packages**

| Features                                                 | Packages                                                                  |           |           |                                                |
|----------------------------------------------------------|---------------------------------------------------------------------------|-----------|-----------|------------------------------------------------|
|                                                          | 100-TEQFP                                                                 | 144-TEQFP | 176-TEQFP | 272-BGA                                        |
| CPU                                                      |                                                                           |           |           |                                                |
| Core                                                     | One or two 32-bit Arm® Cortex®-M7 CPUs and a 32-bit Arm® Cortex® M0+ CPU  |           |           |                                                |
| Functional safety                                        | ASIL-B                                                                    |           |           |                                                |
| Operating voltage                                        | 2.7 V to 5.5 V                                                            |           |           |                                                |
| Operating voltage for HSIO_STD                           | Not supported                                                             |           |           | 2.7 V to 3.6 V                                 |
| Core voltage                                             | 1.05 V to 1.15 V                                                          |           |           |                                                |
| Operating frequency                                      | Arm® Cortex®-M7 250 MHz (max for each) and Arm® Cortex®-M0+ 100 MHz (max) |           |           |                                                |
| MPU, PPU                                                 | Supported                                                                 |           |           |                                                |
| FPU                                                      | Supports both single (32-bit) and double (64-bit) precision               |           |           |                                                |
| DSP-MUL/DIV/MAC                                          | Supported by Arm® Cortex®-M7 CPUs                                         |           |           |                                                |
| TCM                                                      | 16-KB instruction and 16-KB data for each Cortex-M7 CPU                   |           |           |                                                |
| Memory                                                   |                                                                           |           |           |                                                |
| Code-flash                                               | 4160 KB (4032 KB + 128 KB)                                                |           |           |                                                |
| Work-flash                                               | 256 KB (192 KB + 64 KB)                                                   |           |           |                                                |
| SRAM (configurable for retention)                        | 768 KB                                                                    |           |           |                                                |
| ROM                                                      | 64 KB                                                                     |           |           |                                                |
| Communication interfaces                                 |                                                                           |           |           |                                                |
| CAN0 (CAN-FD: Up to 8 Mbps)                              | 4 ch                                                                      |           |           |                                                |
| CAN1 (CAN-FD: Up to 8 Mbps)                              | 4 <sup>[3]</sup> /3 <sup>[4]</sup> ch                                     | 4 ch      |           |                                                |
| CAN RAM                                                  | 32 KB per instance (CAN0/1), 64 KB in total                               |           |           |                                                |
| Serial communication block (SCB/UART)                    | 9 ch                                                                      | 10 ch     |           | 11 ch                                          |
| Serial communication block (SCB/I²C)                     | 9 <sup>[5]</sup> /8 <sup>[6]</sup> ch                                     | 10 ch     |           | 11 ch                                          |
| Serial communication block (SCB/SPI)                     | 8 ch                                                                      | 10 ch     |           | 11 ch                                          |
| LIN                                                      | 9 ch                                                                      | 12 ch     | 16 ch     |                                                |
| Ethernet MAC                                             | 1 ch × 10/100 (ETH0, MII/RMII on GPIO_STD)                                |           |           |                                                |
| Memory interfaces                                        |                                                                           |           |           |                                                |
| eMMC/SD                                                  | 1 ch (GPIO_STD at 32 MHz)                                                 |           |           | 1 ch (HSIO_STD at 50 MHz, GPIO_STD at 32 MHz)  |
| Single SPI / Dual SPI / Quad SPI / Octal SPI / HYPERBUS™ | 1 ch (GPIO_STD at 32 MHz)                                                 |           |           | 1 ch (HSIO_STD at 100 MHz, GPIO_STD at 32 MHz) |

## Features list

**Table 1-1 CYT3BB/4BB feature list for all packages (continued)**

| Features                                        | Packages                                                                                                               |                                                          |                                                          |                                                          |
|-------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|----------------------------------------------------------|----------------------------------------------------------|
|                                                 | 100-TEQFP                                                                                                              | 144-TEQFP                                                | 176-TEQFP                                                | 272-BGA                                                  |
| Timers                                          |                                                                                                                        |                                                          |                                                          |                                                          |
| RTC                                             | 1 ch                                                                                                                   |                                                          |                                                          |                                                          |
| TCPWM (16-bit) (Motor Control)                  | 12 ch                                                                                                                  |                                                          |                                                          |                                                          |
| TCPWM (16-bit)                                  | 63 ch                                                                                                                  |                                                          |                                                          |                                                          |
| TCPWM (32-bit)                                  | 8 ch                                                                                                                   |                                                          |                                                          |                                                          |
| External interrupts                             | 72                                                                                                                     | 116                                                      | 148                                                      | 220                                                      |
| Analog                                          |                                                                                                                        |                                                          |                                                          |                                                          |
| 12-bit, 1 Msps SAR ADC                          | 3 Units (SAR0/32, SAR1/32, SAR2/8 logical channels)                                                                    |                                                          |                                                          |                                                          |
|                                                 | 37 external channels (SAR0/14 ch, SAR1/15 ch, SAR2/8 ch)                                                               | 52 external channels (SAR0/21 ch, SAR1/23 ch, SAR2/8 ch) | 64 external channels (SAR0/24 ch, SAR1/32 ch, SAR2/8 ch) | 72 external channels (SAR0/32 ch, SAR1/32 ch, SAR2/8 ch) |
|                                                 | 18 ch (6 per ADC) Internal sampling                                                                                    |                                                          |                                                          |                                                          |
| Motor control input                             | 3 ch (synchronous sampling of one channel on each of the 3 ADCs)                                                       |                                                          |                                                          |                                                          |
| Security                                        |                                                                                                                        |                                                          |                                                          |                                                          |
| Flash security (program/work read protection)   | Supported                                                                                                              |                                                          |                                                          |                                                          |
| Flash chip erase enable                         | Configurable                                                                                                           |                                                          |                                                          |                                                          |
| eSHE / HSM                                      | By separate firmware <sup>[2]</sup>                                                                                    |                                                          |                                                          |                                                          |
| Audio                                           |                                                                                                                        |                                                          |                                                          |                                                          |
| I <sup>2</sup> S / TDM                          | Tx 2 ch, Rx 2 ch                                                                                                       | Tx 3 ch, Rx 3 ch                                         |                                                          |                                                          |
| System                                          |                                                                                                                        |                                                          |                                                          |                                                          |
| DMA controller                                  | P-DMA0 with 100 channels (16 general-purpose), P-DMA1 with 58 channels (8 general-purpose), and M-DMA0 with 8 channels |                                                          |                                                          |                                                          |
| Internal main oscillator                        | 8 MHz                                                                                                                  |                                                          |                                                          |                                                          |
| Internal low speed oscillator                   | 32.768 kHz (nominal)                                                                                                   |                                                          |                                                          |                                                          |
| PLL                                             | Input: 3.988 to 33.34 MHz, PLL output: up to 250 MHz                                                                   |                                                          |                                                          |                                                          |
| FLL                                             | Input: 0.25 to 80 MHz, FLL output: up to 100 MHz                                                                       |                                                          |                                                          |                                                          |
| Watchdog timer and Multi-counter Watchdog timer | Supported                                                                                                              |                                                          |                                                          |                                                          |
| Clock supervisor                                | Supported                                                                                                              |                                                          |                                                          |                                                          |
| Cyclic wakeup from DeepSleep                    | Supported                                                                                                              |                                                          |                                                          |                                                          |
| GPIO_STD                                        | 68                                                                                                                     | 112                                                      | 144                                                      | 203                                                      |
| GPIO_ENH                                        | 4                                                                                                                      |                                                          |                                                          |                                                          |
| HSIO_STD                                        | Not supported                                                                                                          |                                                          |                                                          | 13                                                       |
| Smart I/O (Blocks)                              | 3 blocks, mapped through 15 I/Os                                                                                       | 5 blocks, mapped through 27 I/Os                         | 5 blocks, mapped through 36 I/Os                         |                                                          |
| Low-voltage detect                              | Two, 26 selectable levels                                                                                              |                                                          |                                                          |                                                          |

**Note**

2. Enhanced Secure Hardware Extension (eSHE) and Hardware Security Module (HSM) support are enabled by third-party firmware.

**Table 1-1 CYT3BB/4BB feature list for all packages (continued)**

| Features                    | Packages                                                            |           |           |         |
|-----------------------------|---------------------------------------------------------------------|-----------|-----------|---------|
|                             | 100-TEQFP                                                           | 144-TEQFP | 176-TEQFP | 272-BGA |
| Maximum ambient temperature | 105 °C for S-grade, 125 °C for E-grade                              |           |           |         |
| Debug interface             | SWD/JTAG                                                            |           |           |         |
| Debug trace                 | Arm® Cortex®-M7 ETB size of 8 KB, Arm® Cortex® M0+ MTB size of 4 KB |           |           |         |

## 1.1 Communication peripheral instance list

The following table lists the instances supported under each package for communication peripherals, based on the minimum pins needed for the functionality.

**Table 1-2 Communication peripheral instance list**

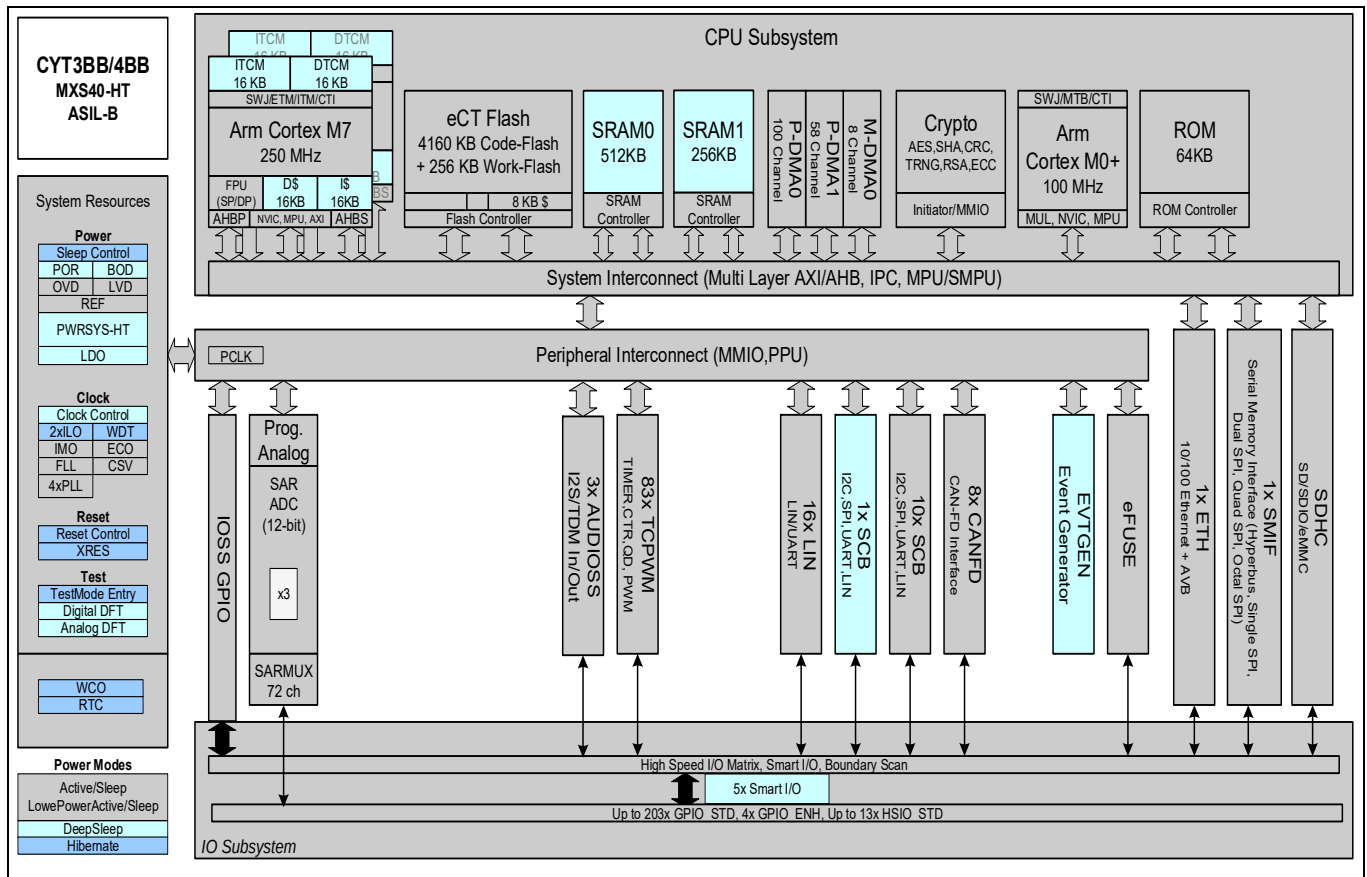
| Module   | 100-TEQFP                                                  | 144-TEQFP | 176-TEQFP | 272-BGA | Minimum pin functions    |
|----------|------------------------------------------------------------|-----------|-----------|---------|--------------------------|
| CAN0     | 0/1/2/3                                                    | 0/1/2/3   | 0/1/2/3   | 0/1/2/3 | TX, RX                   |
| CAN1     | 0/1/2/3 <sup>[3]</sup> or<br>0/2/3 <sup>[4]</sup>          | 0/1/2/3   | 0/1/2/3   | 0/1/2/3 | TX, RX                   |
| LIN0     | 0/1/2/3/4/6/7/8/9                                          | 0 to 11   | 0 to 15   | 0 to 15 | TX, RX                   |
| SCB/UART | 0 to 8                                                     | 0 to 9    | 0 to 9    | 0 to 10 | TX, RX                   |
| SCB/I2C  | 0 to 8 <sup>[5]</sup> or<br>0/1/2/3/4/5/7/8 <sup>[6]</sup> | 0 to 9    | 0 to 9    | 0 to 10 | SCL, SDA                 |
| SCB/SPI  | 0/1/2/3/4/5/7/8                                            | 0 to 9    | 0 to 9    | 0 to 10 | MISO, MOSI, SCK, SELECT0 |

### Notes

3. Function EXT\_PS\_CTL0 on P22.1 is not used.
4. Function EXT\_PS\_CTL0 on P22.1 is used.
5. Functions EXT\_PS\_CTL0 on P21.1 and EXT\_PS\_CTL1 on P21.2 are not used.
6. Function EXT\_PS\_CTL0 on P21.1 or EXT\_PS\_CTL1 on P21.2 is used.

## 2 Blocks and functionality

### 2.1 Block diagram



The **Block diagram** shows the CYT3BB/4BB architecture block diagram, giving a simplified view of the interconnection between subsystems and blocks. CYT3BB/4BB has four major subsystems: CPU, system resources, peripherals, and I/O<sup>[7, 8, 9]</sup>. The color-coding shows the lowest power mode where the particular block is still functional.

CYT3BB/4BB provides extensive support for programming, testing, debugging, and tracing of both hardware and firmware.

Debug-on-chip functionality enables in-system debugging using the production device. It does not require special interfaces, debugging pods, simulators, or emulators.

The JTAG interface is fully compatible with industry-standard third-party probes such as I-jet, J-Link, and GHS.

The debug circuits are enabled by default.

CYT3BB/4BB provides a high level of security with robust flash protection and the ability to disable features such as debug.

Additionally, each device interface can be permanently disabled for applications concerned with phishing attacks from a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled.

#### Notes

7. GPIO\_STD supports 2.7 V to 5.5 V  $V_{DDIO}$  range.
8. GPIO\_ENH supports 2.7 V to 5.5 V  $V_{DDIO}$  range with higher currents at lower voltages.
9. HSI0\_STD supports 2.7 V to 3.6 V  $V_{DDIO}$  range with high-speed signalling and programmable drive strength.

## **3 Functional description**

### **3.1 CPU subsystem**

#### **3.1.1 CPU**

The CYT3BB/4BB CPU subsystem contains a 32-bit Arm® Cortex®-M0+ CPU with MPU, and one or two 32-bit Arm® Cortex®-M7 CPUs, each with MPU, single/double-precision FPU, and 16-KB data and instruction caches. This subsystem also includes P-/M-DMA controllers, a cryptographic accelerator, 4160 KB of code-flash, 256 KB of work-flash, 768 KB of SRAM, and 64 KB of ROM.

The Cortex®-M0+ CPU provides a secure, un-interruptible boot function. This guarantees that, following completion of the boot function, system integrity is valid and privileges are enforced. Shared resources (flash, SRAM, peripherals, and so on) can be accessed through bus arbitration, and exclusive accesses are supported by an inter-processor communication (IPC) mechanism using hardware semaphores.

Each Cortex®-M7 CPU has 16 KB of instruction and 16 KB of data TCM with programmable read wait states. Each TCM is clocked by the associated Cortex®-M7 CPU clock.

#### **3.1.2 DMA controllers**

CYT3BB/4BB has three DMA controllers: P-DMA0 with 16 general-purpose and 84 dedicated channels, P-DMA1 with 8 general-purpose and 50 dedicated channels, and M-DMA0 with eight channels. P-DMA is used for peripheral-to-memory and memory-to-peripheral data transfers and provides low latency for a large number of channels. Each P-DMA controller uses a single data-transfer engine that is shared by the associated channels. General-purpose channels have a rich interconnect matrix including P-DMA cross triggering which enables demanding data-transfer scenarios. Dedicated channels have a single triggering input (such as an ADC channel) to handle common transfer needs. M-DMA is used for memory-to-memory data transfers and provides high memory bandwidth for a small number of channels. M-DMA uses a dedicated data-transfer engine for each channel. They support independent accesses to peripherals using the AHB multi-layer bus.

#### **3.1.3 Flash**

CYT3BB/4BB has 4160 KB (4032 KB with a 32-KB sector size, and 128 KB with an 8-KB sector size) of code-flash with an additional work-flash of 256 KB (192 KB with a 2-KB sector size, and 64 KB with a 128-B sector size). Work-flash is optimized for reprogramming many more times than code-flash. Code-flash supports Read-While-Write (RWW) operation allowing flash to be updated while the CPU is active. Both the code-flash and work-flash areas support dual-bank operation for over-the-air (OTA) programming.

#### **3.1.4 SRAM**

CYT3BB/4BB has 768 KB of SRAM with two independent controllers. SRAM0 provides DeepSleep retention in 32-KB increments while SRAM1 is selectable between fully retained and not retained.

#### **3.1.5 ROM**

CYT3BB/4BB has 64 KB of ROM that contains boot and configuration routines. This ROM enables secure boot and authentication of user flash to guarantee a secure system.

#### **3.1.6 Cryptography accelerator for security**

The cryptography accelerator implements (3)DES block cipher, AES block cipher, SHA hash, cyclic redundancy check, pseudo random number generation, true random number generation, galois/counter mode, and a vector unit to support asymmetric key cryptography such as RSA and ECC.

## 3.2 System resources

### 3.2.1 Power system

The power system ensures that the supply voltage levels meet the requirements of each power mode, and provides a full-system reset when these levels are not valid. Internal power-on reset (POR) guarantees full-chip reset during the initial power ramp.

Three BOD circuits monitor the external supply voltages ( $V_{DD}$ ,  $V_{DDA}$ ,  $V_{CCD}$ ). The BOD on  $V_{DD}$  and  $V_{CCD}$  is initially enabled and cannot be disabled. The BOD on  $V_{DDA}$  is initially disabled and can be enabled by the user. For the external supplies  $V_{DD}$  and  $V_{DDA}$ , BOD circuits are software-configurable with two settings; a 2.7-V minimum voltage that is robust for all internal signaling, and a 3.0-V minimum voltage, which is also robust for all I/O specifications (which are guaranteed at 2.7 V). The BOD on  $V_{CCD}$  is provided as a safety measure and is not a robust detector.

Three over-voltage detection (OVD) circuits are provided for monitoring external supplies ( $V_{DD}$ ,  $V_{DDA}$ ,  $V_{CCD}$ ), and overcurrent detection circuits (OCD) for monitoring internal and external regulators. OVD thresholds on  $V_{DD}$  and  $V_{DDA}$  are configurable with two settings; a 5.0-V and 5.5-V maximum voltage.

Two voltage detection circuits are provided to monitor the external supply voltage ( $V_{DD}$ ) for falling and rising levels, each configurable for one of the 26 selectable levels.

All BOD, OVD, and OCD circuits on  $V_{DD}$  and  $V_{CCD}$  generate a reset, because these protect the CPUs and fault logic. The BOD and OVD circuits on  $V_{DDA}$  can be configured to generate either a reset, or a fault.

### 3.2.2 Regulators

CYT3BB/4BB contains three regulators that provide power to the low-voltage core transistors: DeepSleep, core internal, and core external. These regulators accept a 2.7-V to 5.5-V  $V_{DD}$  supply and provide a low-noise 1.1-V supply to various parts of the device. These regulators are automatically enabled and disabled by hardware and firmware when switching between power modes. The core internal and core external regulators operate in Active mode, and provide power to the CPU subsystem and associated peripherals.

#### 3.2.2.1 DeepSleep

The DeepSleep regulator is used to maintain power in a small number of blocks when in DeepSleep mode. These blocks include the ILO and WDT timers, BOD detector, SCB0, SRAM memories, Smart I/O, and other configuration memories. The DeepSleep regulator is enabled when in DeepSleep mode, and the core internal regulator is disabled. It is disabled when XRES\_L is asserted (LOW) and when the core internal regulator is disabled.

#### 3.2.2.2 Core internal

The core internal regulator supports load currents up to 300 mA, and is operational during device start-up (boot process), and in Active/Sleep modes.

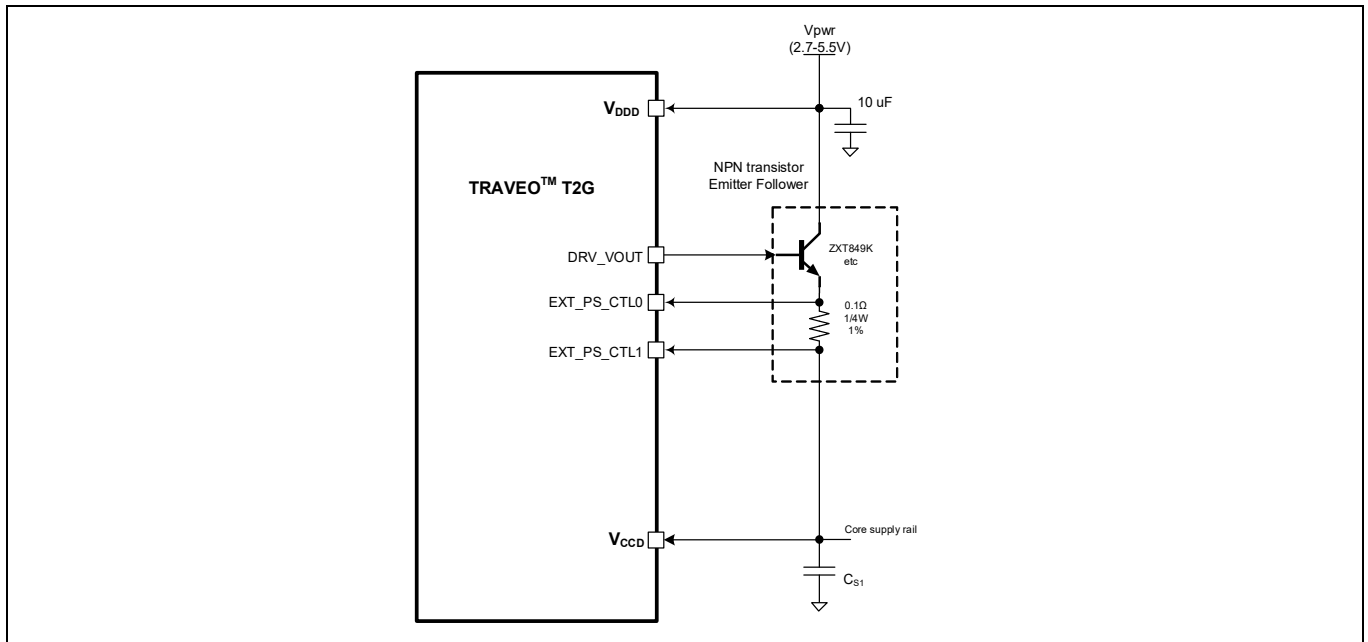
#### 3.2.2.3 Core external<sup>[10]</sup>

To support worst-case loading, with both M7 CPUs and the M0+ CPU at their maximum clock frequency and all integrated peripherals operating, a core external regulator is required, capable of load currents up to 600 mA. While the control and monitor circuits for the core external regulator are internal to CYT3BB/4BB, the power regulating element (NPN pass transistor, PMIC, or LDO) is external. This reduces the overall power dissipation within the CYT3BB/4BB package, while maintaining a well-regulated core supply.

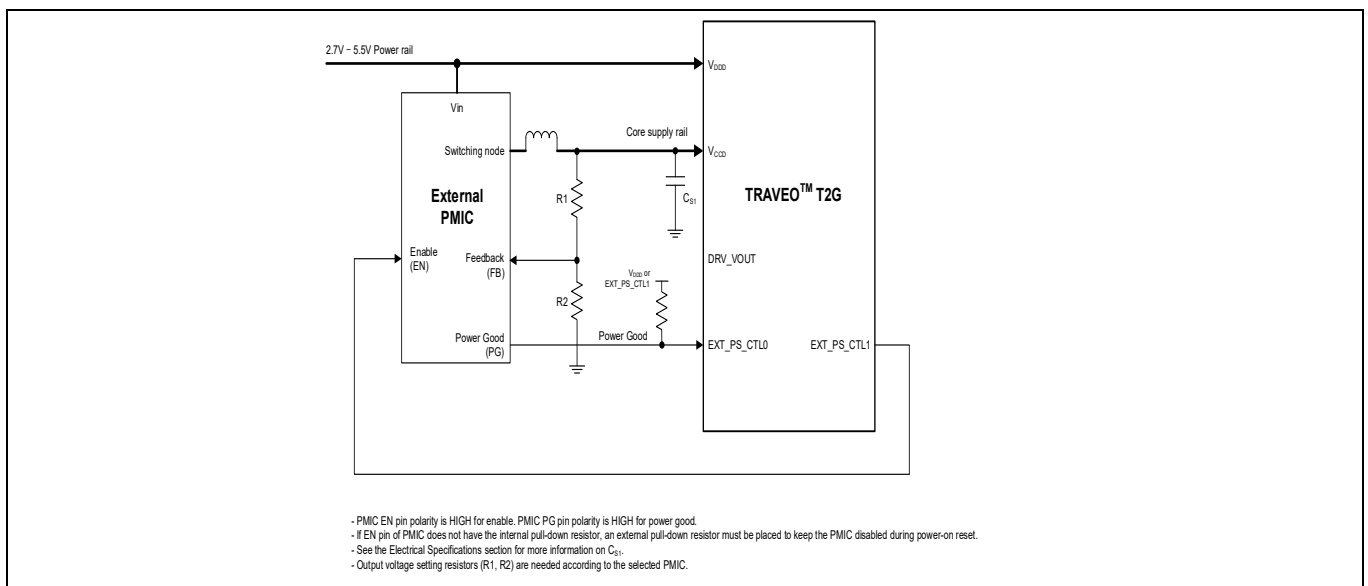
The core external regulator may be implemented with either an external NPN pass transistor, PMIC, or linear regulator (LDO). Each implementation requires different external components on the PCB, and different connections to CYT3BB/4BB for both regulation and control.

#### Note

10. When CYT3BB/4BB is in Hibernate mode, the GPIO used to control the core external regulator are High-Z. This may require an external pull-up or pull-down resistor to disable the external regulator and configure it for minimum operating current.



**Figure 3-1 Sample core external regulator with NPN transistor**



**Figure 3-2 Sample core external regulator with PMIC/LDO**

Both the core internal and core external regulators require an external bulk storage capacitor connected to the VCCD pin. This capacitor provides charge under the dynamic loads of the low-voltage core transistors.

### 3.2.3 Clock system

The CYT3BB/4BB clock system provides clocks to all subsystems that require them, and glitch-free switching between different clock sources. In addition, the clock system ensures that no metastable conditions occur.

The clock system for CYT3BB/4BB consists of the 8-MHz IMO, two ILOs, four watchdog timers, four PLLs, an FLL, five clock supervisors (CSV), a 8- to 33.34-MHz ECO, and a 32.768-kHz WCO.

The clock system supports three main clock domains: CLK\_HF, CLK\_SLOW, and CLK\_LF.

- CLK\_HF<sub>x</sub> are the active mode clocks. Each can use any of the high-frequency clock sources including IMO, EXT\_CLK, ECO, FLL, or PLL
- CLK\_SLOW provides a reference clock for the Cortex-CM0+ CPU, Crypto, P-/M-DMA, and other slow infrastructure blocks of CPU subsystem
- CLK\_LF is a DeepSleep domain clock and provides a reference clock for the MCWDT or RTC modules. The reference clock for the CLK\_LF domain is either disabled or selectable from ILO0, ILO1, or WCO.

**Table 3-1 CLK\_HF destinations**

| Name    | Description                                      |
|---------|--------------------------------------------------|
| CLK_HF0 | CPUSS (Memories, CLK_SLOW, Peripherals)          |
| CLK_HF1 | CPUSS (Cortex-M7 CPU 0, 1)                       |
| CLK_HF2 | CAN FD, LIN, TCPWM, SCB, SAR                     |
| CLK_HF3 | Event Generator                                  |
| CLK_HF4 | Ethernet Internal Clock                          |
| CLK_HF5 | Audio Subsystem (I <sup>2</sup> S), Ethernet TSU |
| CLK_HF6 | SDHC Interface, SMIF                             |

#### 3.2.3.1 IMO clock source

The IMO is the frequency reference in CYT3BB/4BB when no external reference is available or enabled. The IMO operates at a frequency of around 8 MHz.

#### 3.2.3.2 ILO clock source

An ILO is a low-power oscillator, nominally 32.768 kHz, which generates clocks for a watchdog timer when in DeepSleep mode. There are two ILOs to ensure clock supervisor (CSV) capability in DeepSleep mode. ILO-driven counters can be calibrated to the IMO, WCO, or ECO to improve their accuracy. ILO1 is also used for clock supervision.

#### 3.2.3.3 PLL and FLL

A PLL (one of the two 200 MHz and two 400 MHz) or FLL may be used to generate high-speed clocks from the IMO, ECO, or an EXT\_CLK. The FLL provides a much faster lock than the PLL (5  $\mu$ s instead of 45  $\mu$ s) in exchange for a small amount ( $\pm 2\%$ ) of frequency error<sup>[11]</sup>. A 400-MHz PLL supports spread spectrum clock generation (SSCG) with down spreading

#### 3.2.3.4 Clock supervisor

Each clock supervisor (CSV) allows one clock (reference) to supervise the behavior of another clock (monitored). Each CSV has counters for both the monitored and reference clocks. Parameters for each counter determine the frequency of the reference clock as well as the upper and lower frequency limits of the monitored clock. If the frequency-range comparator detects a stopped clock or a clock outside the specified frequency range, an abnormal state is signaled and either a reset or an interrupt is generated.

**Note**

11. Operation of reference-timed peripherals (such as a UART) with an FLL-based reference is not recommended due the allowed frequency error.

### **3.2.3.5 EXT\_CLK**

One of the three GPIO\_STD I/Os can be used to provide an external clock input of up to 80 MHz. This clock can be used as the source clock for either the PLL or FLL, or can be used directly by the CLK\_HF domain.

### **3.2.3.6 ECO**

The ECO provides high-frequency clocking using an external crystal connected to the ECO\_IN and ECO\_OUT pins. It supports fundamental mode (non-overtone) quartz crystals, in the range of 8 to 33.34 MHz. When used in conjunction with the PLL, it generates CPU and peripheral clocks up to the device's maximum frequency. ECO accuracy depends on the selected crystal. If the ECO is disabled, the associated pins can be used for any of the available I/O functions.

### **3.2.3.7 WCO**

The WCO is a low-power, watch-crystal oscillator intended for real-time-clock applications. It requires an external 32.768-kHz crystal connected to the WCO\_IN and WCO\_OUT pins. The WCO can also be configured as a clock reference for CLK\_LF, which is the clock source for the MCWDT and RTC.

### **3.2.4 Reset**

CYT3BB/4BB can be reset from a variety of sources, including software. Most reset events are asynchronous and guarantee reversion to a known state. The reset cause (POR, BOD, OVD, overcurrent, XRES\_L, WDT, MCWDT, software reset, fault, CSV, Hibernate wakeup, debug) is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES\_L pin is available for external reset.

### **3.2.5 Watchdog timer**

CYT3BB/4BB has one watchdog timer (WDT) and three multi-counter watchdog timers (MCWDT).

The WDT is a free-running counter clocked only by ILO0, which allows it to be used as a wakeup source from Hibernate. Watchdog operation is possible during all power modes. To prevent a device reset from a WDT timeout, the WDT must be serviced during a configured window. A watchdog reset is recorded in the reset cause register.

An MCWDT is available for each of the CPU cores. These timers provide more capabilities than the WDT, and are only available in Active, Sleep, and DeepSleep modes. These timers have multiple counters that can be used separately or cascaded to trigger interrupts and/or resets. They are clocked from ILO0 or the WCO.

### **3.2.6 Power modes**

CYT3BB/4BB has six power modes.

- Active – all peripherals are available
- Low-Power Active (LPACTIVE) – Low-power profile of Active mode where all peripherals and the CPUs are available, but with limited capability
- Sleep – all peripherals except the CPUs are available
- Low-Power Sleep (LPSLEEP) – Low-power profile of Sleep mode where all peripherals except the CPUs are available, but with limited capability
- DeepSleep – only peripherals which work with CLK\_LF are available
- Hibernate – the device and I/O states are frozen, the device resets on wakeup

### 3.3 Peripherals

#### 3.3.1 Peripheral clock dividers

Integer and fractional clock dividers are provided for peripheral and timing purposes.

**Table 3-2 Clock dividers - CPUSS Group (Nr. 0)**

| Divider type | Instances | Description              |
|--------------|-----------|--------------------------|
| div_8        | 3         | Integer divider, 8 bits  |
| div_16       | 1         | Integer divider, 16 bits |

**Table 3-3 Clock dividers - COMM Group (Nr. 1)**

| Divider type | Instances | Description                                                        |
|--------------|-----------|--------------------------------------------------------------------|
| div_8        | 16        | Integer divider, 8 bits                                            |
| div_16       | 17        | Integer divider, 16 bits                                           |
| div_24_5     | 16        | Fractional divider, 24.5 bits (24 integer bits, 5 fractional bits) |

#### 3.3.2 Peripheral protection unit

The Peripheral Protection Unit (PPU) controls and monitors unauthorized access from all masters (CPU, P-/M-DMA, Crypto, and any enabled debug interface) to the peripherals. It allows or restricts data transfers on the bus infrastructure. The access rules are enforced based on specific properties of a transfer, such as an address range for the transfer and access attributes (such as read/write, user/privilege, and secure/non-secure).

#### 3.3.3 12-bit SAR ADC

CYT3BB/4BB contains three 1-Msps SAR ADCs. These ADCs can be clocked at up to 26.67 MHz and provide a 12-bit result in 26 clock cycles. The references for all three SAR ADCs come from a dedicated pair of inputs: VREFH and VREFL<sup>[12]</sup>.

CYT3BB/4BB supports up to 93 logical ADC channels, and external inputs from up to 75 I/Os. Each ADC also supports six internal connections for diagnostic and monitoring purposes. The number of ADC channels (per ADC and package type) are listed in [Table 1-1](#).

Each ADC has a sequencer, which autonomously cycles through the configured channels (sequencer scan) with zero-switching overhead (that is, the aggregate sampling bandwidth, when clocked at 26.67 MHz, is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is controlled through a state machine or firmware. The sequencer prioritizes trigger requests, enables the appropriate analog channel, controls ADC sampling, initiates ADC data conversion, manages results, and initiates subsequent conversions for repetitive or group conversions without CPU intervention.

Each SAR ADC has an analog multiplexer used to connect the signals to be measured to the ADC. It has 32 GPIO\_STD inputs, one special GPIO\_STD input for motor-sense, and six additional inputs to measure internal signals such as a band-gap reference, a temperature sensor, and power supplies. The device supports synchronous sampling of one motor-sense channel on each of the three ADCs.

CYT3BB/4BB has one temperature sensor that is shared by all three ADCs. The temperature sensor must only be sampled by one ADC at a time. Software post-processing is required to convert the temperature sensor reading into kelvin or Celsius values.

To accommodate signals with varying source impedances and frequencies, it is possible to have different sample times programmed for each channel. Each ADC also supports range comparison, which allows fast detection of out-of-range values without having to wait for a sequencer scan to complete and for the CPU firmware to evaluate the measurement for out-of-range values. The ADCs are not usable in DeepSleep and Hibernate modes as they require a high-speed clock. The ADC input reference voltage VREFH range is 2.7 V to  $V_{DDA}$  and VREFL is  $V_{SSA}$ .

#### Note

12.VREF\_L prevents IR drops in the VSSIO and VSSA paths from impacting the measurements. VREF\_L, when properly connected, reduces or removes the impact of IR drops in the VSSIO and VSSA paths from measurements.

### 3.3.4 Timer/counter/PWM block (TCPWM)

The TCPWM block consists of 16-bit (75 channels) and 32-bit (8 channels) counters with user-programmable period. Twelve of the 16-bit counters are optimized for motor-control operations. Each TCPWM counter contains a capture register to record the count at the time of an event, a period register (used to either stop or auto-reload the counter when its count is equal to the period register), and compare registers to generate signals that are used as PWM duty-cycle outputs.

Each counter within the TCPWM block supports several functional modes such as timer, capture, quadrature, PWM, PWM with dead-time insertion (PWM\_DT, 8-bit), pseudo-random PWM (PWM\_PR), and shift-register.

In motor-control applications, the counter within the TCPWM block supports enhanced quadrature mode with features such as asymmetric PWM generation, dead-time insertion (16-bit), and association of different dead times for PWM output signals.

The TCPWM block also provides true and complement outputs, with programmable offset between them, to allow their use as deadband complementary PWM outputs. The TCPWM block also has a kill input (only for the PWM mode) to force outputs to a predetermined state; for example, this may be used in motor-drive systems when an overcurrent state is detected and the PWMs driving the FETs need to be shut off immediately (no time for software intervention).

### 3.3.5 Serial communication blocks (SCB)

CYT3BB/4BB contains up to 11 serial communication blocks, each configurable to support I<sup>2</sup>C, UART, or SPI.

#### 3.3.5.1 I<sup>2</sup>C interface

An SCB can be configured to implement a full I<sup>2</sup>C master (capable of multi-master arbitration) or slave interface. Each SCB configured for I<sup>2</sup>C can operate at speeds of up to 1 Mbps (Fast-mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency of the CPU. In addition, each SCB supports FIFO buffering for receive and transmit data, which, by increasing the time for the CPU to read the data, reduces the need for clock stretching. The I<sup>2</sup>C interface is compatible with Standard, Fast-mode, and Fast-mode Plus devices as specified in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C-bus I/O is implemented with GPIO in open-drain modes<sup>[13, 14]</sup>.

#### 3.3.5.2 UART interface

When configured as a UART, each SCB provides a full-featured UART with maximum signalling rate determined by the configured peripheral-clock frequency and over-sampling rate. It supports infrared interface (IrDA) and SmartCard (ISO 7816) protocols, which are minor variants of the UART protocol. It also supports the 9-bit multi-processor mode that allows the addressing of peripherals connected over common Rx and Tx lines. Common UART functions such as parity, number of stop bits, break detect, and frame error are supported. FIFO buffering of transmit and receive data allows greater CPU service latencies to be tolerated.

The LIN protocol is supported by the UART. LIN is based on a single-master multi-slave topology. There is one master node and multiple slave nodes on the LIN bus. The SCB UART supports only LIN slave functionality. Compared to the dedicated LIN blocks, an SCB/UART used for LIN requires a higher level of software interaction and increased CPU load.

#### Notes

13. This is not 100% compliant with the I<sup>2</sup>C-bus specification; I/Os are not over-voltage tolerant, do not support the 20-mA sink requirement of Fast-mode Plus, and violate the leakage specification when no power is applied.

14. Only Port 0 with the slew rate control enabled meets the minimum fall time requirement.

### 3.3.5.3 SPI interface

The SPI configuration supports full Motorola SPI, TI Synchronous Serial Protocol (SSP, essentially adds a start pulse that is used to synchronize SPI-based Codecs), and National Microwire (a half-duplex form of SPI). The SPI interface can use the FIFO. The SPI interface operates with up to a 12.5-MHz SPI Clock. SCB also supports EZSPI<sup>[15]</sup> mode.

SCB0 supports the following additional features:

- Operable as a slave in DeepSleep mode
- I<sup>2</sup>C slave EZ (EZI<sup>2</sup>C<sup>[16]</sup>) mode with up to 256-B data buffer for multi-byte communication without CPU intervention
- I<sup>2</sup>C slave externally-clocked operations
- Command/response mode with a 512-B data buffer for multi-byte communication without CPU intervention

### 3.3.6 CAN FD

CYT3BB/4BB contains two CAN FD controller blocks, each supporting four CAN FD channel. All CAN FD controllers are compliant with the ISO 11898-1:2015 standard; an ISO 16845:2015 certificate is available. It also implements the time-triggered CAN (TTCAN) protocol specified in ISO 11898-4 (TTCAN protocol levels 1 and 2) completely in hardware. All functions concerning the handling of messages are implemented by the Rx and Tx handlers. The Rx handler manages message acceptance filtering, transfer of received messages from the CAN core to a message RAM, and provides receive-message status. The Tx handler is responsible for the transfer of transmit messages from the message RAM to the CAN core, and provides transmit-message status.

### 3.3.7 Local interconnect network (LIN)

CYT3BB/4BB contains up to 16 LIN blocks. Each block supports transmission/reception of data following the LIN protocol according to ISO standard 17987. Each LIN block connects to an external transceiver through a 3-pin interface (including an enable function) and supports master and slave functionality. Each block also supports classic and enhanced checksum, along with break detection during message reception and wake-up signaling. Break detection, sync field, checksum calculations, and error interrupts are handled in hardware.

### 3.3.8 Ethernet MAC

CYT3BB/4BB supports one Ethernet channel with transfer rates of 10, or 100 Mbps. The input/output frames and flow control are compliant to the Ethernet/IEEE 802.3bw standard and also IEEE-1588 precision-time protocol (PTP). CYT3BB/4BB supports half/full-duplex data transport using external PHY devices. The MAC supports glue-free connection to PHYs through IEEE standard MII, and RMII interfaces. The device also supports Audio-Video Bridging (AVB). The MAC supports standard 6-byte programmable addresses.

### 3.3.9 External memory interface

In addition to the internal flash memory, CYT3BB/4BB supports direct connection to as much as 128 MB of external flash or RAM memory. This connection is made through either a HYPERBUS™ or serial peripheral interface (SPI). HYPERBUS™ allows connection to HYPERFLASH™ and HYPERRAM™ devices, while SPI (single, dual, quad, or octal SPI) can connect with serial flash memory. Code stored in memory connected through this interface allows execute-in-place (XIP) operation, which does not require the instructions to be first copied to internal memory, and on-the-fly encryption and decryption for environments requiring secure external data and code.

#### Notes

15. The Easy SPI (EZSPI) protocol is based on the Motorola SPI protocol operating in any mode (0, 1, 2, or 3). It allows communication between master and slave while reducing the need for CPU intervention.

16. The Easy I<sup>2</sup>C (EZI<sup>2</sup>C) protocol is a unique communication scheme built on top of the I<sup>2</sup>C protocol by Cypress. It uses a meta protocol around the standard I<sup>2</sup>C protocol to communicate to an I<sup>2</sup>C slave using indexed memory transfers. This reduces the need for CPU intervention.

### 3.3.10 SDHC interface

CYT3BB/4BB supports one Secure Digital High Capacity (SDHC) interface, which conforms to Secure Digital (SD) 6.0, Secure Digital Input Output (SDIO) 4.10, and Embedded Multimedia Card (eMMC) 5.1 specifications, along with Host Control Interface (HCI) 4.2 specification. The interface supports System DMA (SDMA), Advance DMA (ADMA2, ADMA3), and command queuing (CQ) features. This interface supports data rates of SD DS (Default Speed, 4-bits at 25 MHz), SD HS (High Speed, 4-bits at 50 MHz), and eMMC 52-MHz DDR (8-bits at 52-MHz card clock).

### 3.3.11 Audio interface

CYT3BB/4BB supports three instances of Inter-IC Sound Bus (I<sup>2</sup>S) interface to connect to digital audio devices: Supports I<sup>2</sup>S Left Justified (LJ), and eight-channel Time Division Multiplexed (TDM) digital audio interface formats in both master and slave modes with independent operations in receive and transmit directions.

### 3.3.12 One-time-programmable (OTP) eFuse

CYT3BB/4BB contains a 1024-bit OTP eFuse memory that can be used to store and access a unique and unalterable identifier or serial number for each device. eFuses are also used to control the device life-cycle (manufacturing, programming, normal operation, end-of-life, and so on) and the security state. Of the 1024 bits, 192 are available for user purposes.

### 3.3.13 Event generator

The event generator supports generation of interrupts and triggers in Active mode and interrupts in DeepSleep mode. The event generators are used to trigger a specific device operation (execution of an interrupt handler, a SAR ADC conversion, and so on) and to provide a cyclic wakeup mechanism from DeepSleep mode. They provide CPU-free triggers for device functions, and reduce CPU involvement in triggering device functions, thus reducing overall power consumption and processing overhead.

### 3.3.14 Trigger multiplexer

CYT3BB/4BB supports connection of various peripherals using trigger signals. Triggers are used to inform a peripheral of the occurrence of an event or change of state. These triggers are used to affect or initiate some action in other peripherals. The trigger multiplexer is used to route triggers from a source peripheral to a destination. Triggers provide active logic functionality and are typically supported in Active mode.

## 3.4 I/Os

CYT3BB/4BB has up to 220 programmable I/Os.

The I/Os are organized as logical entities called ports, which are a maximum of 8 bits wide. During power-on, and reset, the I/Os are forced to the High-Z state. During the Hibernate mode, I/Os are frozen.

Every I/O can generate an interrupt (if enabled) and each port has an interrupt request (IRQ) and interrupt service routine (ISR) associated with it.

I/O port power source mapping is listed in [Table 3-4](#). The associated supply determines the  $V_{OH}$ ,  $V_{OL}$ ,  $V_{IH}$ , and  $V_{IL}$  levels when configured for CMOS and Automotive thresholds.

**Table 3-4 I/O port power source**

| Supply pins | Ports                                                                              |
|-------------|------------------------------------------------------------------------------------|
| VDDD        | P0, P1, P2, P3, P4, P5, P16, P17, P18, P19, P20, P21, P22, P23, P28, P29, P30, P31 |
| VDDIO_1     | P6, P7, P8, P9, P32                                                                |
| VDDIO_2     | P10, P11, P12, P13, P14, P15, P26, P27                                             |
| VDDIO_3     | P24, P25                                                                           |

### 3.4.1 Port nomenclature

Px.y describes a particular bit “y” available within an I/O port “x.”

For example, P4.2 reads “port 4, bit 2”.

Each I/O implements the following:

- Programmable drive mode
  - High impedance
  - Resistive pull-up
  - Resistive pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up or pull-down
  - Weak pull-up or pull-down

CYT3BB/4BB has three types of programmable I/Os: GPIO Standard, GPIO Enhanced, and HSIO Standard.

### 3.4.2 GPIO Standard (GPIO\_STD)

Supports standard automotive signaling across the 2.7-V to 5.5-V  $V_{DDIO}$  range. GPIO Standard I/Os have multiple configurable drive levels, drive modes, and selectable input levels.

### 3.4.3 GPIO Enhanced (GPIO\_ENH)

Supports extended functionality automotive signaling across the 2.7-V to 5.5-V  $V_{DDIO}$  range with higher currents at lower voltages (full I<sup>2</sup>C timing support, slew-rate control).

Both GPIO\_STD and GPIO\_ENH implement the following:

- Configurable input threshold (CMOS, TTL, or Automotive)
- Hold mode for latching previous state (used for retaining the I/O state in DeepSleep mode)
- Analog input mode (input and output buffers disabled)

### 3.4.4 HSIO Standard (HSIO\_STD)

These I/Os are optimized exclusively for high-speed signaling and do not support slew-rate control, DeepSleep operation, POR mode control, analog connections, or non-CMOS signaling levels. HSIO\_STD supports high-speed peripherals such as QSPI, HYPERBUS™, Ethernet, and SDHC controller. HSIO\_STD also supports programmable drive strength. These I/Os are available only in Active mode and retain state in DeepSleep mode.

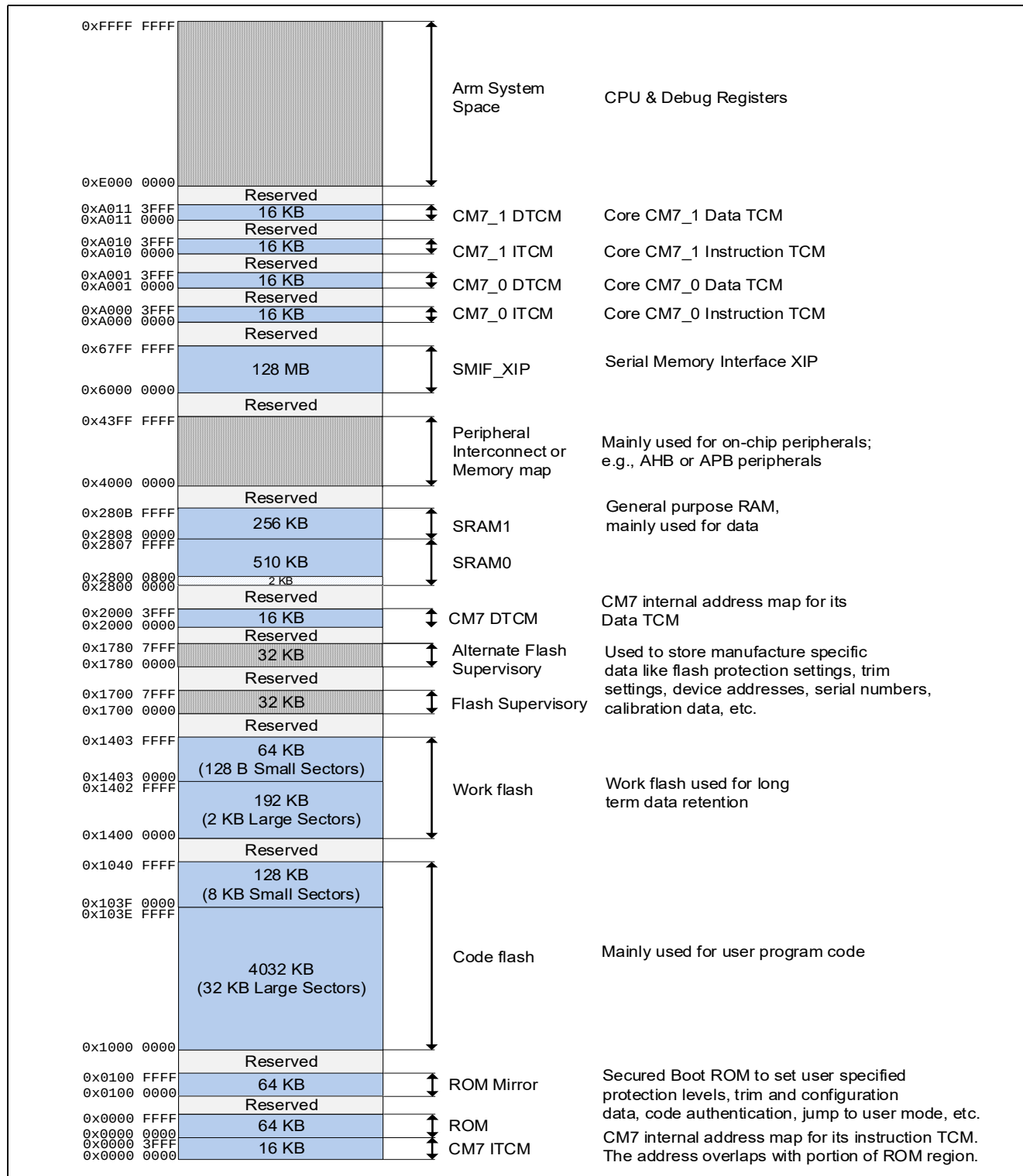
### 3.4.5 Smart I/O

Smart I/O allows Boolean operations on signals going to the I/O from the subsystems of the chip or on signals coming into the chip. CYT3BB/4BB has five Smart I/O blocks. Operation can be synchronous or asynchronous and the blocks operate in all device power modes except for Hibernate.

## **4 CYT3BB/4BB address map**

The CYT3BB/4BB microcontroller supports the memory spaces shown in [Figure 4-1](#).

- 4160 KB (4032 KB + 128 KB) of code-flash, used in the single- or dual-bank mode based on the associated bit in the flash control register
  - Single-bank mode: 4160 KB
  - Dual-bank mode: 2080 KB per bank
- 256 KB (192 KB + 64 KB) of work-flash, used in the single- or dual-bank mode based on the associated bit in the flash control register
  - Single-bank mode: 256 KB
  - Dual-bank mode: 128 KB per bank
- 64 KB of secure ROM
- 768 KB of SRAM (First 2 KB is reserved for internal usage)
- 16 KB of Instruction TCM for each Cortex-M7 CPU
- 16 KB of Data TCM for each Cortex-M7 CPU
- 128 MB SMIF XIP



**Figure 4-1** CYT3BB/4BB address map<sup>[17, 18]</sup>

#### Notes

17. The size representation is not up to scale.

18. First 2KB of SRAM is reserved, not available for users. User must keep the power of first 32KB block of SRAM0 in enabled or retained in all Active, LP Active, Sleep, LP Sleep, DeepSleep modes.

## 5 Flash base address map

**Table 5-1** through **Table 5-6** give information about the sector mapping of the code- and work-flash regions along with their respective base addresses.

**Table 5-1 Code-flash Address Mapping in Single-Bank Mode**

| Code-flash Size (KB) | Large Sectors (LS) | Small Sectors (SS) | Large Sector Base Address | Small Sector Base Address |
|----------------------|--------------------|--------------------|---------------------------|---------------------------|
| 4160                 | 32 KB × 126        | 8 KB × 16          | 0x1000 0000               | 0x103F 0000               |

**Table 5-2 Work-flash Address Mapping in Single-Bank Mode**

| Work-flash Size (KB) | Large Sectors | Small Sectors | Large Sector Base Address | Small Sector Base Address |
|----------------------|---------------|---------------|---------------------------|---------------------------|
| 256                  | 2 KB × 96     | 128 B × 512   | 0x1400 0000               | 0x1403 0000               |

**Table 5-3 Code-flash Address Mapping in Dual-Bank Mode (Mapping A)**

| Code-flash Size (KB) | First Half LS | First Half SS | Second Half LS | Second Half SS | First Half LS Base Address | First Half SS Base Address | Second Half LS Base Address | Second Half SS Base Address |
|----------------------|---------------|---------------|----------------|----------------|----------------------------|----------------------------|-----------------------------|-----------------------------|
| 4160                 | 32 KB × 63    | 8 KB × 8      | 32 KB × 63     | 8 KB × 8       | 0x1000 0000                | 0x101F 8000                | 0x1200 0000                 | 0x121F 8000                 |

**Table 5-4 Code-flash Address Mapping in Dual-Bank Mode (Mapping B)**

| Code-flash Size (KB) | First Half LS | First Half SS | Second Half LS | Second Half SS | First Half LS Base Address | First Half SS Base Address | Second Half LS Base Address | Second Half SS Base Address |
|----------------------|---------------|---------------|----------------|----------------|----------------------------|----------------------------|-----------------------------|-----------------------------|
| 4160                 | 32 KB × 63    | 8 KB × 8      | 32 KB × 63     | 8 KB × 8       | 0x1200 0000                | 0x121F 8000                | 0x1000 0000                 | 0x101F 8000                 |

**Table 5-5 Work-flash Address Mapping in Dual-Bank Mode (Mapping A)**

| Work-flash Size (KB) | First Half LS | First Half SS | Second Half LS | Second Half SS | First Half LS Base Address | First Half SS Base Address | Second Half LS Base Address | Second Half SS Base Address |
|----------------------|---------------|---------------|----------------|----------------|----------------------------|----------------------------|-----------------------------|-----------------------------|
| 256                  | 2 KB × 48     | 128 B × 256   | 2 KB × 48      | 128 B × 256    | 0x1400 0000                | 0x1401 8000                | 0x1500 0000                 | 0x1501 8000                 |

**Table 5-6 Work-flash Address Mapping in Dual-Bank Mode (Mapping B)**

| Work-flash Size (KB) | First Half LS | First Half SS | Second Half LS | Second Half SS | First Half LS Base Address | First Half SS Base Address | Second Half LS Base Address | Second Half SS Base Address |
|----------------------|---------------|---------------|----------------|----------------|----------------------------|----------------------------|-----------------------------|-----------------------------|
| 256                  | 2 KB × 48     | 128 B × 256   | 2 KB × 48      | 128 B × 256    | 0x1500 0000                | 0x1501 8000                | 0x1400 0000                 | 0x1401 8000                 |

## 6 Peripheral I/O map

**Table 6-1 CYT3BB/4BB peripheral I/O map**

| Section   | Description                                  | Base Address | Instances          | Instance Size | Group | Slave |
|-----------|----------------------------------------------|--------------|--------------------|---------------|-------|-------|
| PERI      | Peripheral interconnect                      | 0x4000 0000  |                    |               | 0     | 0     |
|           | Peripheral group (0, 1, 2, 3, 4, 5, 6, 8, 9) | 0x4000 4000  | 9                  | 0x40          |       |       |
|           | Peripheral trigger group                     | 0x4000 8000  | 11                 | 0x400         |       |       |
|           | Peripheral 1:1 trigger group                 | 0x4000 C000  | 11                 | 0x400         |       |       |
| PERI_MS   | Peripheral interconnect, master interface    | 0x4002 0000  |                    |               | 0     | 1     |
|           | PERI Programmable PPU                        | 0x4002 0000  | 10 <sup>[19]</sup> | 0x40          |       |       |
|           | PERI Fixed PPU                               | 0x4002 0800  | 700                | 0x40          |       |       |
| PERI_PCLK | Peripheral Clock Groups                      | 0x4004 0000  | 2                  | 0x2000        | 0     | 2     |
| CRYPTO    | Cryptography component                       | 0x4010 0000  |                    |               | 1     | 0     |
| CPUSS     | CPU subsystem (CPUSS)                        | 0x4020 0000  |                    |               | 2     | 0     |
| FAULT     | Fault structure subsystem                    | 0x4021 0000  |                    |               | 2     | 1     |
|           | Fault structures                             | 0x4021 0000  | 4                  | 0x100         |       |       |
| IPC       | Inter process communication                  | 0x4022 0000  |                    |               | 2     | 2     |
|           | IPC structures                               | 0x4022 0000  | 8                  | 0x20          |       |       |
|           | IPC interrupt structures                     | 0x4022 1000  | 8                  | 0x20          |       |       |
| PROT      | Protection                                   | 0x4023 0000  |                    |               | 2     | 3     |
|           | Shared memory protection unit structures     | 0x4023 2000  | 16                 | 0x40          |       |       |
|           | Memory protection unit structures            | 0x4023 4000  | 16                 | 0x400         |       |       |
| FLASHC    | Flash controller                             | 0x4024 0000  |                    |               | 2     | 4     |
| SRSS      | System Resources Sub-System Core Registers   | 0x4026 0000  |                    |               | 2     | 5     |
|           | Clock Supervision High Frequency             | 0x4026 1400  | 8                  | 0x10          |       |       |
|           | Clock Supervision Reference Frequency        | 0x4026 1710  | 1                  |               |       |       |
|           | Clock Supervision Low Frequency              | 0x4026 1720  | 1                  |               |       |       |
|           | Clock Supervision Internal Low Frequency     | 0x4026 1730  | 1                  |               |       |       |
|           | Clock PLL 400 MHz                            | 0x4026 1900  | 2                  | 0x10          |       |       |
|           | Multi Counter WDT                            | 0x4026 8000  | 3                  | 0x100         |       |       |
|           | Free Running WDT                             | 0x4026 C000  | 1                  |               |       |       |
| BACKUP    | SRSS Backup Domain/RTC                       | 0x4027 0000  |                    |               | 2     | 6     |
|           | Backup Register                              | 0x4027 1000  | 4                  | 0x04          |       |       |
| P-DMA     | P-DMA0 Controller                            | 0x4028 0000  |                    |               | 2     | 7     |
|           | P-DMA0 channel structures                    | 0x4028 8000  | 100                | 0x40          |       |       |
|           | P-DMA1 Controller                            | 0x4029 0000  |                    |               | 2     | 8     |
|           | P-DMA1 channel structures                    | 0x4029 8000  | 58                 | 0x40          |       |       |
| M-DMA     | M-DMA0 Controller                            | 0x402A 0000  |                    |               | 2     | 9     |
|           | M-DMA0 channels                              | 0x402A 1000  | 8                  | 0x100         |       |       |

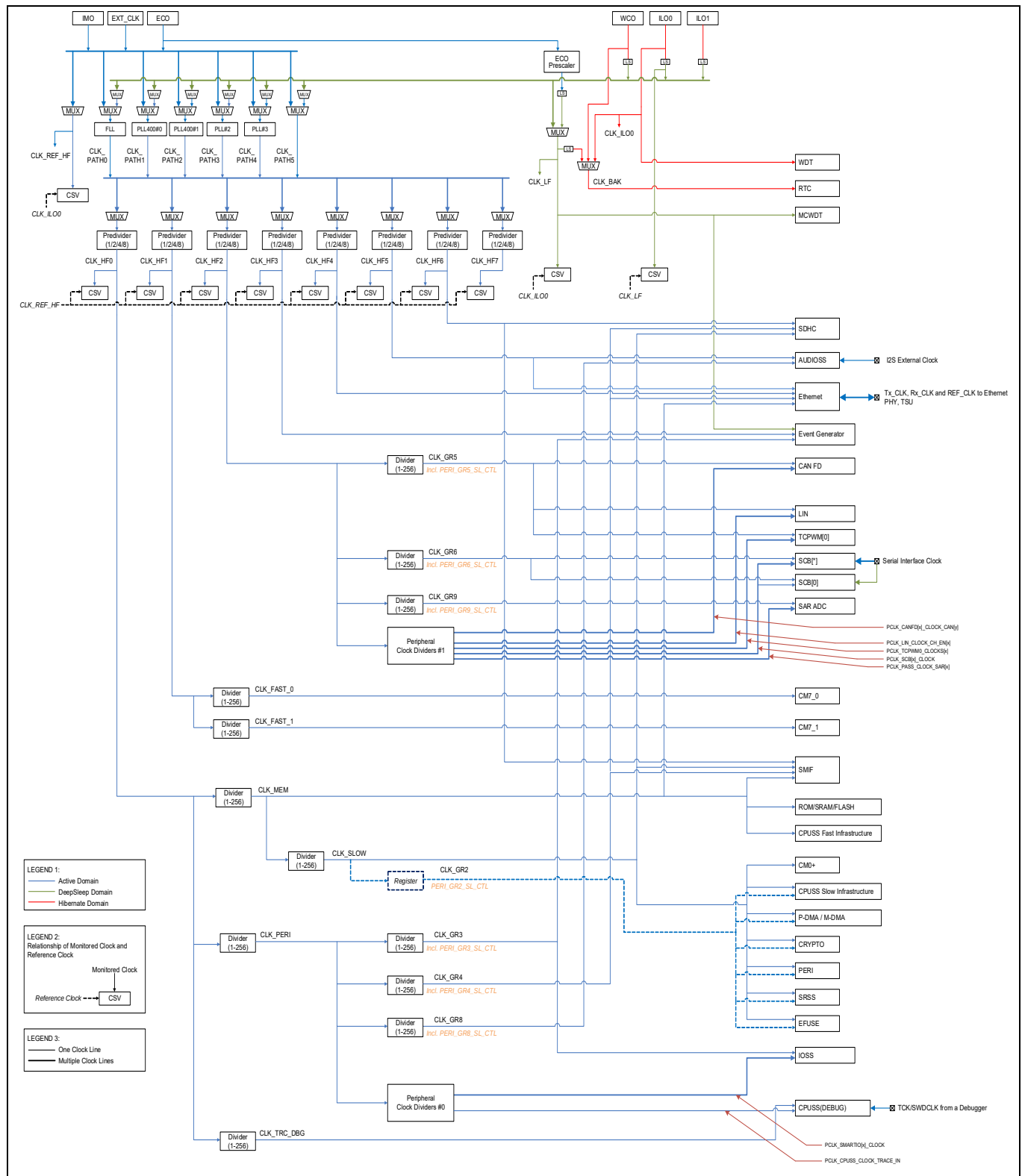
**Note**

19. These Programmable PPU's are configured by the Boot ROM and are available for the user based on the access rights. Refer to the device-specific TRM to know more about the configuration of these programmable PPU's.

**Table 6-1**      **CYT3BB/4BB peripheral I/O map** (continued)

| Section          | Description                                             | Base Address | Instances | Instance Size | Group | Slave |
|------------------|---------------------------------------------------------|--------------|-----------|---------------|-------|-------|
| eFUSE            | eFUSE Customer Data (192 bits)                          | 0x402C 0868  | 6         | 0x04          | 2     | 10    |
| HSIOM            | High-Speed I/O Matrix (HSIOM)                           | 0x4030 0000  | 33        | 0x10          | 3     | 0     |
| GPIO             | GPIO port control/configuration                         | 0x4031 0000  | 33        | 0x80          | 3     | 1     |
| SMARTIO          | Programmable I/O configuration                          | 0x4032 0000  |           |               | 3     | 2     |
|                  | SMARTIO port configuration                              | 0x4032 0C00  | 5         | 0x100         |       |       |
| EVTGEN           | Event generator 0 (EVTGEN0)                             | 0x403F 0000  |           |               | 3     | 3     |
|                  | Event generator 0 comparator structures                 | 0x403F 0800  | 16        | 0x20          |       |       |
| SMIF             | Serial Memory Interface 0 (SMIF0)                       | 0x4042 0000  |           |               | 4     | 0     |
|                  | SMIF0 Devices                                           | 0x4042 0800  | 1         | 0x80          |       |       |
| SDHC             | Secure Digital High Capacity 0 (SDHC0)                  | 0x4046 0000  |           |               | 4     | 1     |
|                  | SDHC0 Wrap                                              | 0x4046 0000  |           |               |       |       |
|                  | SDHC0 Core                                              | 0x4046 1000  |           |               |       |       |
| ETH              | Ethernet 0 (ETH0)                                       | 0x4048 0000  | 1         | 0x10000       | 4     | 2     |
| LIN              | Local Interconnect Network 0 (LIN0)                     | 0x4050 0000  |           |               | 5     | 0     |
|                  | LIN0 Channels                                           | 0x4050 8000  | 16        | 0x100         |       |       |
| TTCANFD          | CAN0 controller                                         | 0x4052 0000  | 4         | 0x200         | 5     | 1     |
|                  | Message RAM CAN0                                        | 0x4053 0000  |           | 0x7FFF        |       |       |
|                  | CAN1 controller                                         | 0x4054 0000  | 4         | 0x200         | 5     | 2     |
|                  | Message RAM CAN1                                        | 0x4055 0000  |           | 0x7FFF        |       |       |
| TCPWM            | Timer/Counter/PWM 0 (TCPWM0)                            | 0x4058 0000  |           |               | 5     | 3     |
|                  | TCPWM0 Group #0 (16-bit)                                | 0x4058 0000  | 63        | 0x80          |       |       |
|                  | TCPWM0 Group #1 (16-bit, Motor control)                 | 0x4058 8000  | 12        | 0x80          |       |       |
|                  | TCPWM0 Group #2 (32-bit)                                | 0x4059 0000  | 8         | 0x80          |       |       |
| SCB              | Serial Communications Block (SPI/UART/I <sup>2</sup> C) | 0x4060 0000  | 11        | 0x10000       | 6     | 0-10  |
| I <sup>2</sup> S | I <sup>2</sup> S Audio Subsystem                        | 0x4080 0000  | 3         | 0x1000        | 8     | 0-2   |
| SAR PASS         | Programmable Analog Subsystem (PASS0)                   | 0x4090 0000  |           |               | 9     | 0     |
|                  | SAR0 channel controller                                 | 0x4090 0000  |           |               |       |       |
|                  | SAR1 channel controller                                 | 0x4090 1000  |           |               |       |       |
|                  | SAR2 channel controller                                 | 0x4090 2000  |           |               |       |       |
|                  | SAR0 channel structures                                 | 0x4090 0800  | 32        | 0x40          |       |       |
|                  | SAR1 channel structures                                 | 0x4090 1800  | 32        | 0x40          |       |       |
|                  | SAR2 channel structures                                 | 0x4090 2800  | 8         | 0x40          |       |       |

## 7 CYT3BB/4BB clock diagram



**Figure 7-1** CYT3BB/4BB clock diagram

## 8 CYT3BB/4BB CPU start-up sequence

The start-up sequence is described in the following steps:

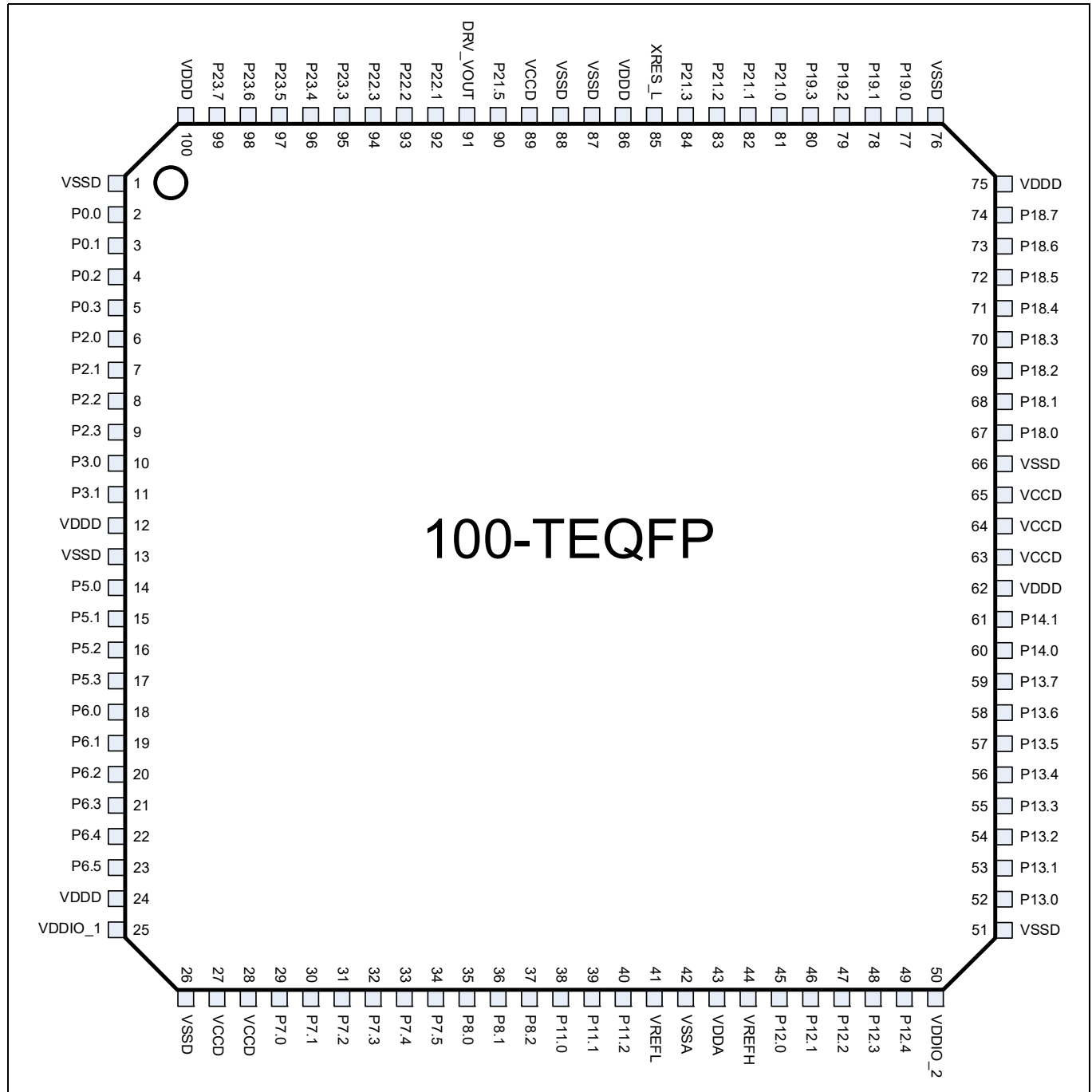
1. System Reset (@0x0000 0000)
2. CM0+ executes ROM boot (@0x0000 0004)
  - i. Applies trims
  - ii. Applies Debug Access port (DAP) access restrictions and system protection from eFuse and supervisory flash
  - iii. Authenticates flash boot (only in SECURE life-cycle stage) and transfers control to it
3. CM0+ executes flash boot (from Supervisory flash @0x1700 2000)
  - i. Debug pins are configured based on the SWD/JTAG spec<sup>[20]</sup>
  - ii. Sets CM0+ vector offset register (CM0\_VTOR part of the Arm® system space) to the beginning of flash (@0x1000 0000)
  - iii. CM0+ branches to its Reset handler
4. CM0+ starts execution of application
  - i. Moves CM0+ vector table to SRAM (updates CM0+ vector table base)
  - i. Sets clocks for CM7\_0 (CLK\_HF1) and CM7\_1 (CLK\_HF2)
  - ii. Sets CM7\_0 (CM7\_0\_VECTOR\_TABLE\_BASE @0x4020 0200) and CM7\_1 (CM7\_1\_VECTOR\_TABLE\_BASE @0x4020 0600) vector tables to the respective locations, also and mentioned in flash (specified in the linker definition file)
  - iii. Enables the power for both the CPU cores CM7\_0 and CM7\_1
  - iv. Disables CPU\_WAIT to allow accesses from the debugger
  - v. Releases CM7\_0 and/or CM7\_1 from reset
  - vi. Continues execution of CM0+ user application
5. CM7\_0 and/or CM7\_1 executes directly from either code-flash or SRAM
  - i. CM7\_0/CM7\_1 branches to its Reset handler
  - ii. Continues execution of the user application

### Note

20. Port configuration of SWD/JTAG pins will be changed from the default GPIO mode to support debugging after the boot process, refer to [Table 11-1](#) for pin assignments.

## 9 Pin assignment

**Note:** For all TEQFP packages, the thermal pad needs to be connected to VSSD.



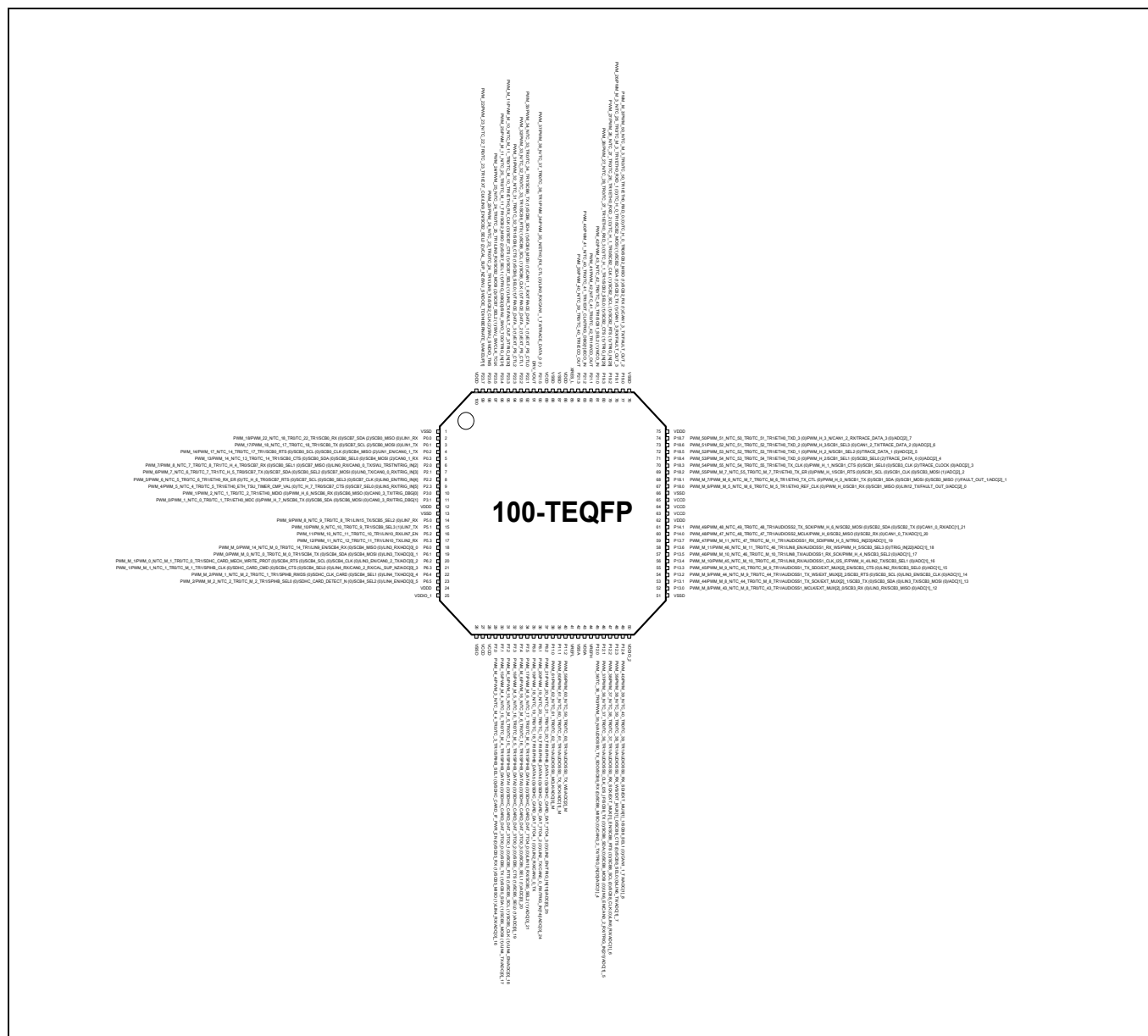
**Figure 9-1 100-TEQFP pin assignment**

# TRAVEO™ T2G 32-bit Automotive MCU

## Based on Arm® Cortex®-M7 single/dual



### Pin assignment



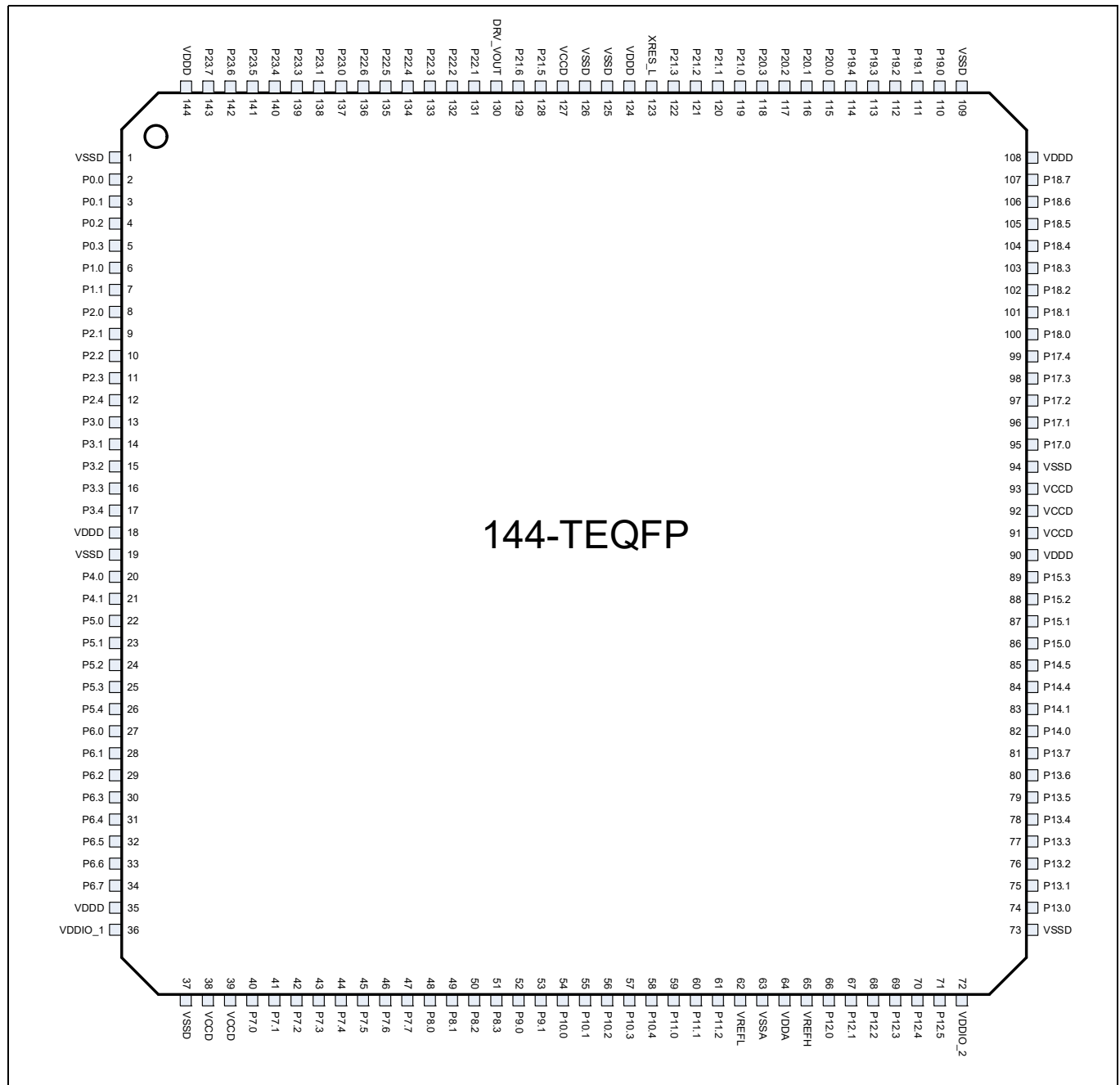
**Figure 9-2 100-TEQFP pin assignment with alternate functions**

# TRAVEO™ T2G 32-bit Automotive MCU

## Based on Arm® Cortex®-M7 single/dual



### Pin assignment



**Figure 9-3 144-TEQFP pin assignment**

# TRAVEO™ T2G 32-bit Automotive MCU

## Based on Arm® Cortex®-M7 single/dual



### Pin assignment

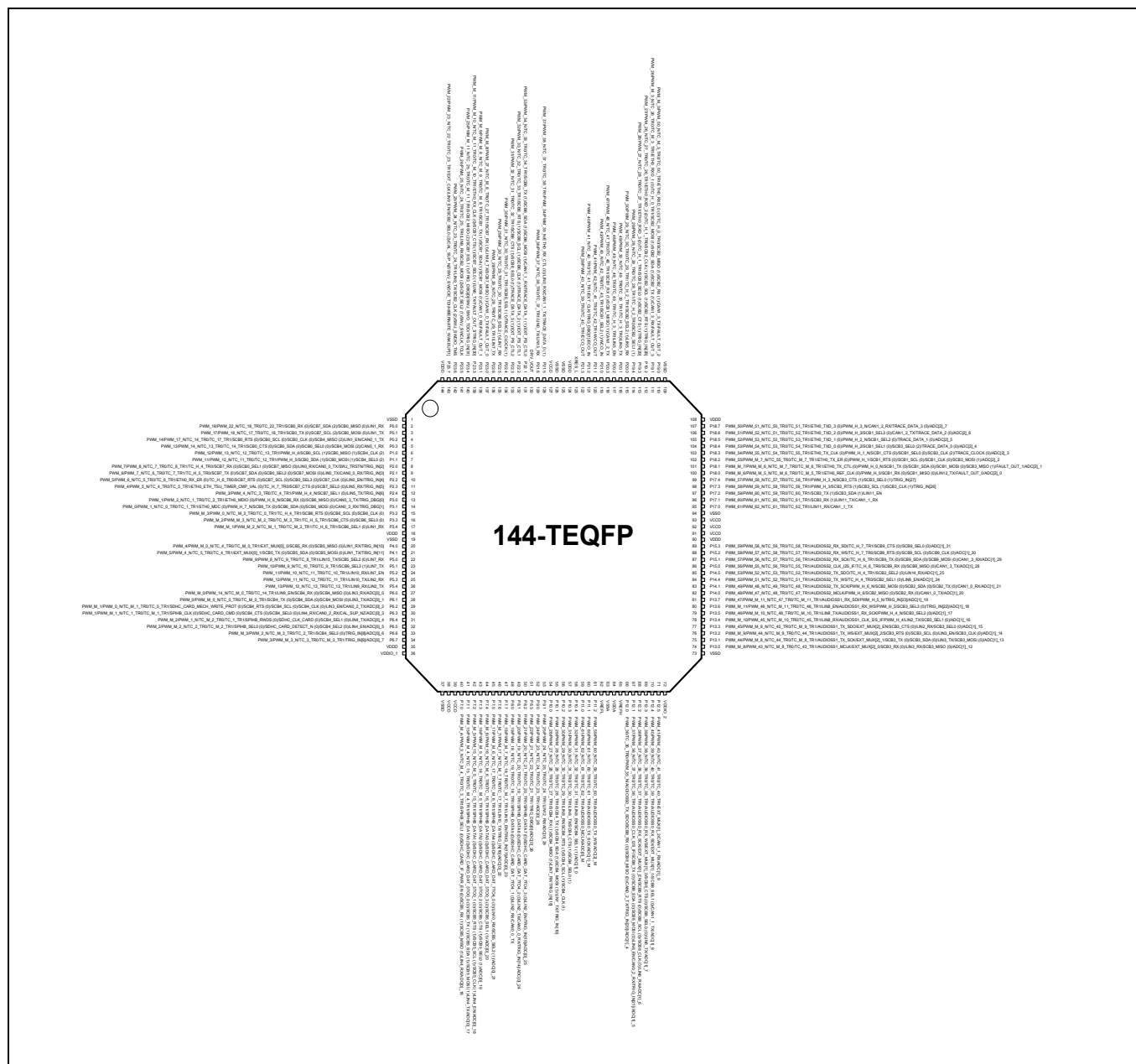
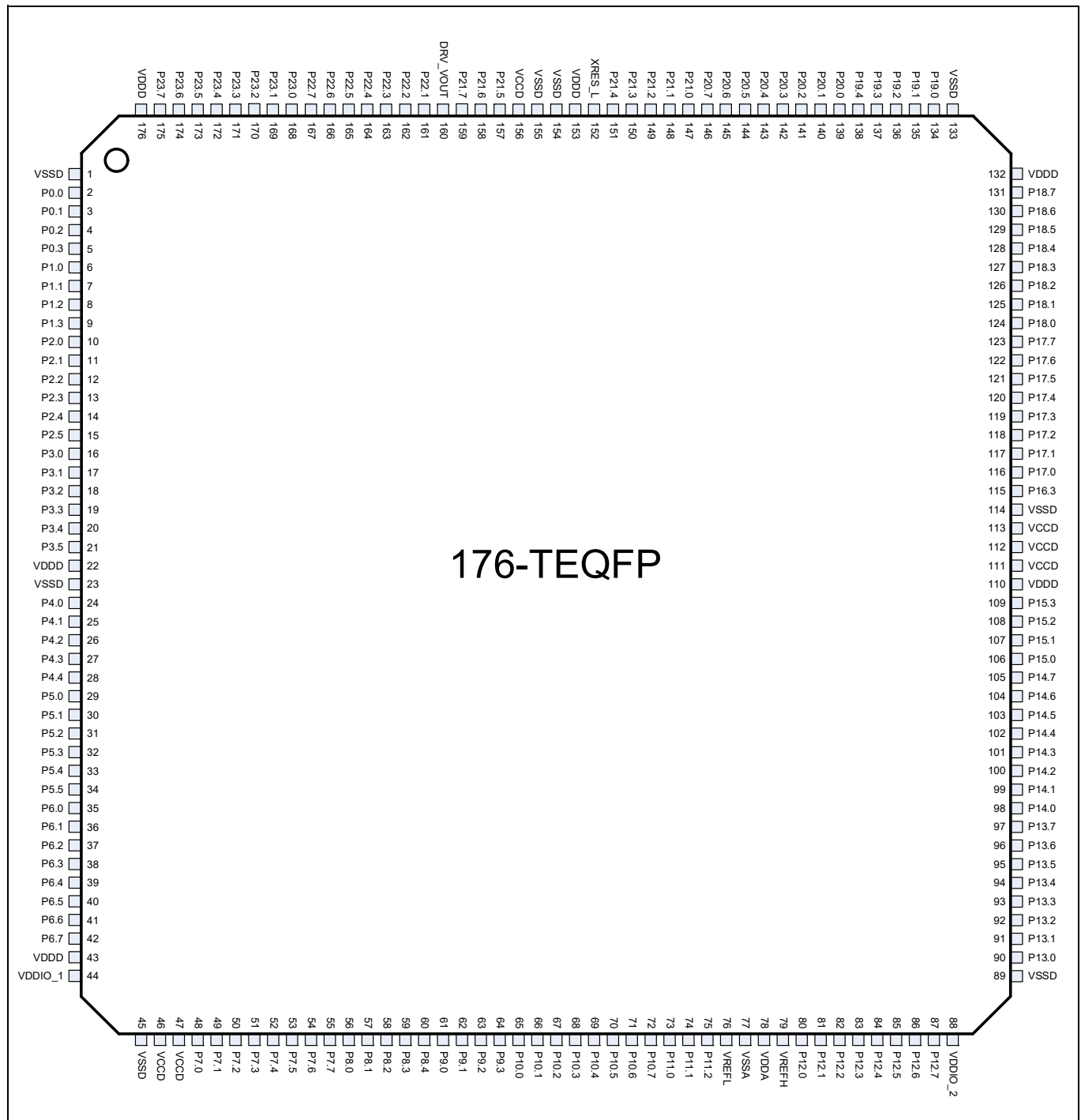


Figure 9-4 144-TQFP pin assignment with alternate functions

Pin assignment



**Figure 9-5 176-TEQFP pin assignment**

# TRAVEO™ T2G 32-bit Automotive MCU

## Based on Arm® Cortex®-M7 single/dual



### Pin assignment

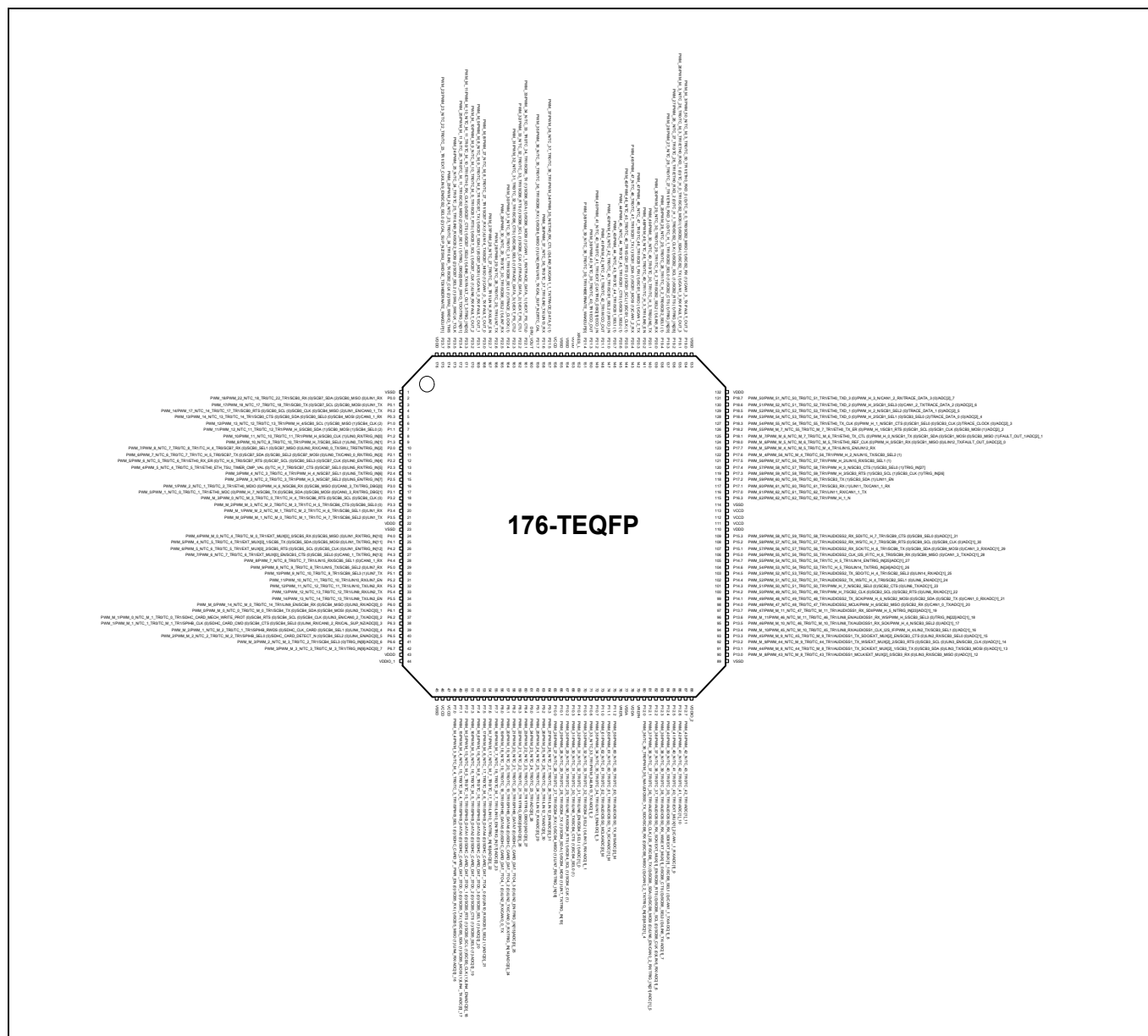
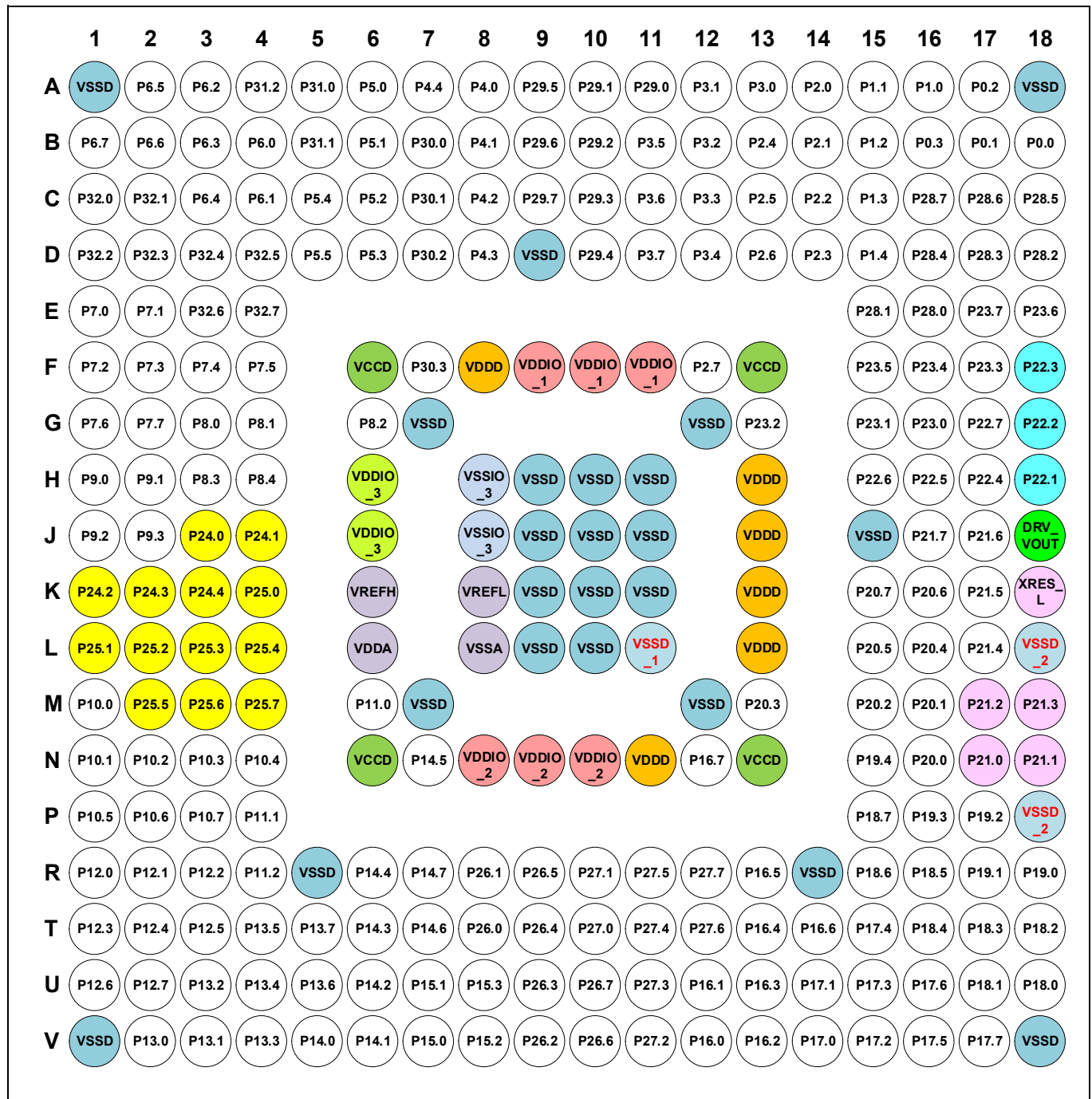


Figure 9-6 176-TEQFP pin assignment with alternate functions

Pin assignment



**Figure 9-7 272-BGA ball map**

## 10 High-speed I/O matrix connections

**Table 10-1 HSIOM connections reference**

| Name                | Number | Description               |
|---------------------|--------|---------------------------|
| HSIOM_SEL_GPIO      | 0      | GPIO controls 'out'       |
| HSIOM_SEL_GPIO_DSI  | 1      | Reserved                  |
| HSIOM_SEL_DSI_DSI   | 2      |                           |
| HSIOM_SEL_DSI_GPIO  | 3      |                           |
| HSIOM_SEL_AMUXA     | 4      |                           |
| HSIOM_SEL_AMUXB     | 5      |                           |
| HSIOM_SEL_AMUXA_DSI | 6      |                           |
| HSIOM_SEL_AMUXB_DSI | 7      |                           |
| HSIOM_SEL_ACT_0     | 8      | Active functionality 0    |
| HSIOM_SEL_ACT_1     | 9      | Active functionality 1    |
| HSIOM_SEL_ACT_2     | 10     | Active functionality 2    |
| HSIOM_SEL_ACT_3     | 11     | Active functionality 3    |
| HSIOM_SEL_DS_0      | 12     | DeepSleep functionality 0 |
| HSIOM_SEL_DS_1      | 13     | DeepSleep functionality 1 |
| HSIOM_SEL_DS_2      | 14     | DeepSleep functionality 2 |
| HSIOM_SEL_DS_3      | 15     | DeepSleep functionality 3 |
| HSIOM_SEL_ACT_4     | 16     | Active functionality 4    |
| HSIOM_SEL_ACT_5     | 17     | Active functionality 5    |
| HSIOM_SEL_ACT_6     | 18     | Active functionality 6    |
| HSIOM_SEL_ACT_7     | 19     | Active functionality 7    |
| HSIOM_SEL_ACT_8     | 20     | Active functionality 8    |
| HSIOM_SEL_ACT_9     | 21     | Active functionality 9    |
| HSIOM_SEL_ACT_10    | 22     | Active functionality 10   |
| HSIOM_SEL_ACT_11    | 23     | Active functionality 11   |
| HSIOM_SEL_ACT_12    | 24     | Active functionality 12   |
| HSIOM_SEL_ACT_13    | 25     | Active functionality 13   |
| HSIOM_SEL_ACT_14    | 26     | Active functionality 14   |
| HSIOM_SEL_ACT_15    | 27     | Active functionality 15   |
| HSIOM_SEL_DS_4      | 28     | DeepSleep functionality 4 |
| HSIOM_SEL_DS_5      | 29     | DeepSleep functionality 5 |
| HSIOM_SEL_DS_6      | 30     | DeepSleep functionality 6 |
| HSIOM_SEL_DS_7      | 31     | DeepSleep functionality 7 |

# 11 Package pin list and alternate functions

Most pins have alternate functionality, as specified in [Table 11-1](#).

Port 11 has the following additional features,

- Ability to pass full-level analog signals to the SAR without clipping to  $V_{DDIO}$  in cases where  $V_{DDIO} < V_{DDA}$
- Ability to simultaneously capture all three ADC signals with highest priority (ADC[0:2]\_M)
- Lower noise, for the most sensitive sensors

**Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) mode, Analog, Smart I/O** <sup>[24, 25]</sup>

| Name | I/O type               | Package |           |           |           | DeepSleep mapping         |           |               | Analog | SMART I/O |
|------|------------------------|---------|-----------|-----------|-----------|---------------------------|-----------|---------------|--------|-----------|
|      | HCon#0 <sup>[21]</sup> | 272-BGA | 176-TEQFP | 144-TEQFP | 100-TEQFP | HCon#14                   | HCon#29   | HCon#30       |        |           |
|      |                        | Pin     | Pin       | Pin       | Pin       | DS #0 <sup>[22, 23]</sup> | DS #1     | DS #2         |        |           |
| P0.0 | GPIO_ENH               | B18     | 2         | 2         | 2         |                           |           | SCB0_MISO (0) |        |           |
| P0.1 | GPIO_ENH               | B17     | 3         | 3         | 3         |                           |           | SCB0_MOSI (0) |        |           |
| P0.2 | GPIO_ENH               | A17     | 4         | 4         | 4         | SCB0_SCL (0)              |           | SCB0_CLK (0)  |        |           |
| P0.3 | GPIO_ENH               | B16     | 5         | 5         | 5         | SCB0_SDA (0)              |           | SCB0_SEL0 (0) |        |           |
| P1.0 | GPIO_STD               | A16     | 6         | 6         | NA        | SCB0_SCL (1)              |           | SCB0_MISO (1) |        |           |
| P1.1 | GPIO_STD               | A15     | 7         | 7         | NA        | SCB0_SDA (1)              |           | SCB0_MOSI (1) |        |           |
| P1.2 | GPIO_STD               | B15     | 8         | NA        | NA        |                           |           | SCB0_CLK (1)  |        |           |
| P1.3 | GPIO_STD               | C15     | 9         | NA        | NA        |                           |           | SCB0_SEL0 (1) |        |           |
| P1.4 | GPIO_STD               | D15     | NA        | NA        | NA        |                           |           |               |        |           |
| P2.0 | GPIO_STD               | A14     | 10        | 8         | 6         |                           | SWJ_TRSTN | SCB0_SEL1 (0) |        |           |
| P2.1 | GPIO_STD               | B14     | 11        | 9         | 7         |                           |           | SCB0_SEL2 (0) |        |           |
| P2.2 | GPIO_STD               | C14     | 12        | 10        | 8         |                           |           | SCB0_SEL3 (0) |        |           |
| P2.3 | GPIO_STD               | D14     | 13        | 11        | 9         |                           |           |               |        |           |
| P2.4 | GPIO_STD               | B13     | 14        | 12        | NA        |                           |           |               |        |           |
| P2.5 | GPIO_STD               | C13     | 15        | NA        | NA        |                           |           |               |        |           |
| P2.6 | GPIO_STD               | D13     | NA        | NA        | NA        |                           |           |               |        |           |
| P2.7 | GPIO_STD               | F12     | NA        | NA        | NA        |                           |           |               |        |           |

## Notes

- 21.HCon refers to High Speed I/O matrix connection reference as per [Table 10-1](#).  
22.DeepSleep ordering (DS #0, DS #1, DS #2) does not have any impact on choosing any alternate functions; the HSIOM module handles the individual alternate function assignment.  
23.All port pin functions available in DeepSleep mode are also available in Active mode.  
24.Refer to [Table 13-2](#) for more information on pin multiplexer abbreviations used.  
25.For any function marked with an identifier (n), the AC timing is only guaranteed within the respective group "n".

**Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) mode, Analog, Smart I/O** (continued)<sup>[24, 25]</sup>

| Name | I/O type               | Package |           |           |           | DeepSleep mapping         |         |         | Analog    | SMART I/O |
|------|------------------------|---------|-----------|-----------|-----------|---------------------------|---------|---------|-----------|-----------|
|      | HCon#0 <sup>[21]</sup> | 272-BGA | 176-TEQFP | 144-TEQFP | 100-TEQFP | HCon#14                   | HCon#29 | HCon#30 |           |           |
|      |                        | Pin     | Pin       | Pin       | Pin       | DS #0 <sup>[22, 23]</sup> | DS #1   | DS #2   |           |           |
| P3.0 | GPIO_STD               | A13     | 16        | 13        | 10        |                           |         |         |           |           |
| P3.1 | GPIO_STD               | A12     | 17        | 14        | 11        |                           |         |         |           |           |
| P3.2 | GPIO_STD               | B12     | 18        | 15        | NA        |                           |         |         |           |           |
| P3.3 | GPIO_STD               | C12     | 19        | 16        | NA        |                           |         |         |           |           |
| P3.4 | GPIO_STD               | D12     | 20        | 17        | NA        |                           |         |         |           |           |
| P3.5 | GPIO_STD               | B11     | 21        | NA        | NA        |                           |         |         |           |           |
| P3.6 | GPIO_STD               | C11     | NA        | NA        | NA        |                           |         |         |           |           |
| P3.7 | GPIO_STD               | D11     | NA        | NA        | NA        |                           |         |         |           |           |
| P4.0 | GPIO_STD               | A8      | 24        | 20        | NA        |                           |         |         |           |           |
| P4.1 | GPIO_STD               | B8      | 25        | 21        | NA        |                           |         |         |           |           |
| P4.2 | GPIO_STD               | C8      | 26        | NA        | NA        |                           |         |         |           |           |
| P4.3 | GPIO_STD               | D8      | 27        | NA        | NA        |                           |         |         |           |           |
| P4.4 | GPIO_STD               | A7      | 28        | NA        | NA        |                           |         |         |           |           |
| P5.0 | GPIO_STD               | A6      | 29        | 22        | 14        |                           |         |         |           |           |
| P5.1 | GPIO_STD               | B6      | 30        | 23        | 15        |                           |         |         |           |           |
| P5.2 | GPIO_STD               | C6      | 31        | 24        | 16        |                           |         |         |           |           |
| P5.3 | GPIO_STD               | D6      | 32        | 25        | 17        |                           |         |         |           |           |
| P5.4 | GPIO_STD               | C5      | 33        | 26        | NA        |                           |         |         |           |           |
| P5.5 | GPIO_STD               | D5      | 34        | NA        | NA        |                           |         |         |           |           |
| P6.0 | GPIO_STD               | B4      | 35        | 27        | 18        |                           |         |         | ADC[0]_0  |           |
| P6.1 | GPIO_STD               | C4      | 36        | 28        | 19        |                           |         |         | ADC[0]_1  |           |
| P6.2 | GPIO_STD               | A3      | 37        | 29        | 20        |                           |         |         | ADC[0]_2  |           |
| P6.3 | GPIO_STD               | B3      | 38        | 30        | 21        |                           |         |         | ADC[0]_3  |           |
| P6.4 | GPIO_STD               | C3      | 39        | 31        | 22        |                           |         |         | ADC[0]_4  |           |
| P6.5 | GPIO_STD               | A2      | 40        | 32        | 23        |                           |         |         | ADC[0]_5  |           |
| P6.6 | GPIO_STD               | B2      | 41        | 33        | NA        |                           |         |         | ADC[0]_6  |           |
| P6.7 | GPIO_STD               | B1      | 42        | 34        | NA        |                           |         |         | ADC[0]_7  |           |
| P7.0 | GPIO_STD               | E1      | 48        | 40        | 29        |                           |         |         | ADC[0]_16 |           |
| P7.1 | GPIO_STD               | E2      | 49        | 41        | 30        |                           |         |         | ADC[0]_17 |           |
| P7.2 | GPIO_STD               | F1      | 50        | 42        | 31        |                           |         |         | ADC[0]_18 |           |
| P7.3 | GPIO_STD               | F2      | 51        | 43        | 32        |                           |         |         | ADC[0]_19 |           |

**Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) mode, Analog, Smart I/O** (continued)<sup>[24, 25]</sup>

| Name  | I/O type               | Package |           |           |           | DeepSleep mapping         |         |         | Analog    | SMART I/O   |
|-------|------------------------|---------|-----------|-----------|-----------|---------------------------|---------|---------|-----------|-------------|
|       | HCon#0 <sup>[21]</sup> | 272-BGA | 176-TEQFP | 144-TEQFP | 100-TEQFP | HCon#14                   | HCon#29 | HCon#30 |           |             |
|       |                        | Pin     | Pin       | Pin       | Pin       | DS #0 <sup>[22, 23]</sup> | DS #1   | DS #2   |           |             |
| P7.4  | GPIO_STD               | F3      | 52        | 44        | 33        |                           |         |         | ADC[0]_20 |             |
| P7.5  | GPIO_STD               | F4      | 53        | 45        | 34        |                           |         |         | ADC[0]_21 |             |
| P7.6  | GPIO_STD               | G1      | 54        | 46        | NA        |                           |         |         | ADC[0]_22 |             |
| P7.7  | GPIO_STD               | G2      | 55        | 47        | NA        |                           |         |         | ADC[0]_23 |             |
| P8.0  | GPIO_STD               | G3      | 56        | 48        | 35        |                           |         |         |           |             |
| P8.1  | GPIO_STD               | G4      | 57        | 49        | 36        |                           |         |         | ADC[0]_24 |             |
| P8.2  | GPIO_STD               | G6      | 58        | 50        | 37        |                           |         |         | ADC[0]_25 |             |
| P8.3  | GPIO_STD               | H3      | 59        | 51        | NA        |                           |         |         | ADC[0]_26 |             |
| P8.4  | GPIO_STD               | H4      | 60        | NA        | NA        |                           |         |         | ADC[0]_27 |             |
| P9.0  | GPIO_STD               | H1      | 61        | 52        | NA        |                           |         |         | ADC[0]_28 |             |
| P9.1  | GPIO_STD               | H2      | 62        | 53        | NA        |                           |         |         | ADC[0]_29 |             |
| P9.2  | GPIO_STD               | J1      | 63        | NA        | NA        |                           |         |         | ADC[0]_30 |             |
| P9.3  | GPIO_STD               | J2      | 64        | NA        | NA        |                           |         |         | ADC[0]_31 |             |
| P10.0 | GPIO_STD               | M1      | 65        | 54        | NA        |                           |         |         |           |             |
| P10.1 | GPIO_STD               | N1      | 66        | 55        | NA        |                           |         |         |           |             |
| P10.2 | GPIO_STD               | N2      | 67        | 56        | NA        |                           |         |         |           |             |
| P10.3 | GPIO_STD               | N3      | 68        | 57        | NA        |                           |         |         |           |             |
| P10.4 | GPIO_STD               | N4      | 69        | 58        | NA        |                           |         |         | ADC[1]_0  |             |
| P10.5 | GPIO_STD               | P1      | 70        | NA        | NA        |                           |         |         | ADC[1]_1  |             |
| P10.6 | GPIO_STD               | P2      | 71        | NA        | NA        |                           |         |         | ADC[1]_2  |             |
| P10.7 | GPIO_STD               | P3      | 72        | NA        | NA        |                           |         |         | ADC[1]_3  |             |
| P11.0 | GPIO_STD               | M6      | 73        | 59        | 38        |                           |         |         | ADC[0]_M  |             |
| P11.1 | GPIO_STD               | P4      | 74        | 60        | 39        |                           |         |         | ADC[1]_M  |             |
| P11.2 | GPIO_STD               | R4      | 75        | 61        | 40        |                           |         |         | ADC[2]_M  |             |
| P12.0 | GPIO_STD               | R1      | 80        | 66        | 45        |                           |         |         | ADC[1]_4  | SMARTIO12_0 |
| P12.1 | GPIO_STD               | R2      | 81        | 67        | 46        |                           |         |         | ADC[1]_5  | SMARTIO12_1 |
| P12.2 | GPIO_STD               | R3      | 82        | 68        | 47        |                           |         |         | ADC[1]_6  | SMARTIO12_2 |
| P12.3 | GPIO_STD               | T1      | 83        | 69        | 48        |                           |         |         | ADC[1]_7  | SMARTIO12_3 |
| P12.4 | GPIO_STD               | T2      | 84        | 70        | 49        |                           |         |         | ADC[1]_8  | SMARTIO12_4 |
| P12.5 | GPIO_STD               | T3      | 85        | 71        | NA        |                           |         |         | ADC[1]_9  | SMARTIO12_5 |
| P12.6 | GPIO_STD               | U1      | 86        | NA        | NA        |                           |         |         | ADC[1]_10 | SMARTIO12_6 |

**Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) mode, Analog, Smart I/O** (continued)<sup>[24, 25]</sup>

| Name  | I/O type               | Package |           |           |           | DeepSleep mapping         |         |         | Analog    | SMART I/O   |
|-------|------------------------|---------|-----------|-----------|-----------|---------------------------|---------|---------|-----------|-------------|
|       | HCon#0 <sup>[21]</sup> | 272-BGA | 176-TEQFP | 144-TEQFP | 100-TEQFP | HCon#14                   | HCon#29 | HCon#30 |           |             |
|       |                        | Pin     | Pin       | Pin       | Pin       | DS #0 <sup>[22, 23]</sup> | DS #1   | DS #2   |           |             |
| P12.7 | GPIO_STD               | U2      | 87        | NA        | NA        |                           |         |         | ADC[1]_11 | SMARTIO12_7 |
| P13.0 | GPIO_STD               | V2      | 90        | 74        | 52        |                           |         |         | ADC[1]_12 | SMARTIO13_0 |
| P13.1 | GPIO_STD               | V3      | 91        | 75        | 53        |                           |         |         | ADC[1]_13 | SMARTIO13_1 |
| P13.2 | GPIO_STD               | U3      | 92        | 76        | 54        |                           |         |         | ADC[1]_14 | SMARTIO13_2 |
| P13.3 | GPIO_STD               | V4      | 93        | 77        | 55        |                           |         |         | ADC[1]_15 | SMARTIO13_3 |
| P13.4 | GPIO_STD               | U4      | 94        | 78        | 56        |                           |         |         | ADC[1]_16 | SMARTIO13_4 |
| P13.5 | GPIO_STD               | T4      | 95        | 79        | 57        |                           |         |         | ADC[1]_17 | SMARTIO13_5 |
| P13.6 | GPIO_STD               | U5      | 96        | 80        | 58        |                           |         |         | ADC[1]_18 | SMARTIO13_6 |
| P13.7 | GPIO_STD               | T5      | 97        | 81        | 59        |                           |         |         | ADC[1]_19 | SMARTIO13_7 |
| P14.0 | GPIO_STD               | V5      | 98        | 82        | 60        |                           |         |         | ADC[1]_20 | SMARTIO14_0 |
| P14.1 | GPIO_STD               | V6      | 99        | 83        | 61        |                           |         |         | ADC[1]_21 | SMARTIO14_1 |
| P14.2 | GPIO_STD               | U6      | 100       | NA        | NA        |                           |         |         | ADC[1]_22 | SMARTIO14_2 |
| P14.3 | GPIO_STD               | T6      | 101       | NA        | NA        |                           |         |         | ADC[1]_23 | SMARTIO14_3 |
| P14.4 | GPIO_STD               | R6      | 102       | 84        | NA        |                           |         |         | ADC[1]_24 | SMARTIO14_4 |
| P14.5 | GPIO_STD               | N7      | 103       | 85        | NA        |                           |         |         | ADC[1]_25 | SMARTIO14_5 |
| P14.6 | GPIO_STD               | T7      | 104       | NA        | NA        |                           |         |         | ADC[1]_26 | SMARTIO14_6 |
| P14.7 | GPIO_STD               | R7      | 105       | NA        | NA        |                           |         |         | ADC[1]_27 | SMARTIO14_7 |
| P15.0 | GPIO_STD               | V7      | 106       | 86        | NA        |                           |         |         | ADC[1]_28 | SMARTIO15_0 |
| P15.1 | GPIO_STD               | U7      | 107       | 87        | NA        |                           |         |         | ADC[1]_29 | SMARTIO15_1 |
| P15.2 | GPIO_STD               | V8      | 108       | 88        | NA        |                           |         |         | ADC[1]_30 | SMARTIO15_2 |
| P15.3 | GPIO_STD               | U8      | 109       | 89        | NA        |                           |         |         | ADC[1]_31 | SMARTIO15_3 |
| P16.0 | GPIO_STD               | V12     | NA        | NA        | NA        |                           |         |         |           |             |
| P16.1 | GPIO_STD               | U12     | NA        | NA        | NA        |                           |         |         |           |             |
| P16.2 | GPIO_STD               | V13     | NA        | NA        | NA        |                           |         |         |           |             |
| P16.3 | GPIO_STD               | U13     | 115       | NA        | NA        |                           |         |         |           |             |
| P16.4 | GPIO_STD               | T13     | NA        | NA        | NA        |                           |         |         |           |             |
| P16.5 | GPIO_STD               | R13     | NA        | NA        | NA        |                           |         |         |           |             |
| P16.6 | GPIO_STD               | T14     | NA        | NA        | NA        |                           |         |         |           |             |
| P16.7 | GPIO_STD               | N12     | NA        | NA        | NA        |                           |         |         |           |             |
| P17.0 | GPIO_STD               | V14     | 116       | 95        | NA        |                           |         |         |           | SMARTIO17_0 |
| P17.1 | GPIO_STD               | U14     | 117       | 96        | NA        |                           |         |         |           | SMARTIO17_1 |

**Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) mode, Analog, Smart I/O** (continued)<sup>[24, 25]</sup>

| Name  | I/O type               | Package |           |           |           | DeepSleep mapping         |         |         | Analog                  | SMART I/O   |
|-------|------------------------|---------|-----------|-----------|-----------|---------------------------|---------|---------|-------------------------|-------------|
|       | HCon#0 <sup>[21]</sup> | 272-BGA | 176-TEQFP | 144-TEQFP | 100-TEQFP | HCon#14                   | HCon#29 | HCon#30 |                         |             |
|       |                        | Pin     | Pin       | Pin       | Pin       | DS #0 <sup>[22, 23]</sup> | DS #1   | DS #2   |                         |             |
| P17.2 | GPIO_STD               | V15     | 118       | 97        | NA        |                           |         |         |                         | SMARTIO17_2 |
| P17.3 | GPIO_STD               | U15     | 119       | 98        | NA        |                           |         |         |                         | SMARTIO17_3 |
| P17.4 | GPIO_STD               | T15     | 120       | 99        | NA        |                           |         |         |                         | SMARTIO17_4 |
| P17.5 | GPIO_STD               | V16     | 121       | NA        | NA        |                           |         |         |                         | SMARTIO17_5 |
| P17.6 | GPIO_STD               | U16     | 122       | NA        | NA        |                           |         |         |                         | SMARTIO17_6 |
| P17.7 | GPIO_STD               | V17     | 123       | NA        | NA        |                           |         |         |                         | SMARTIO17_7 |
| P18.0 | GPIO_STD               | U18     | 124       | 100       | 67        |                           |         |         | ADC[2]_0                |             |
| P18.1 | GPIO_STD               | U17     | 125       | 101       | 68        |                           |         |         | ADC[2]_1                |             |
| P18.2 | GPIO_STD               | T18     | 126       | 102       | 69        |                           |         |         | ADC[2]_2                |             |
| P18.3 | GPIO_STD               | T17     | 127       | 103       | 70        |                           |         |         | ADC[2]_3                |             |
| P18.4 | GPIO_STD               | T16     | 128       | 104       | 71        |                           |         |         | ADC[2]_4                |             |
| P18.5 | GPIO_STD               | R16     | 129       | 105       | 72        |                           |         |         | ADC[2]_5                |             |
| P18.6 | GPIO_STD               | R15     | 130       | 106       | 73        |                           |         |         | ADC[2]_6                |             |
| P18.7 | GPIO_STD               | P15     | 131       | 107       | 74        |                           |         |         | ADC[2]_7                |             |
| P19.0 | GPIO_STD               | R18     | 134       | 110       | 77        |                           |         |         |                         |             |
| P19.1 | GPIO_STD               | R17     | 135       | 111       | 78        |                           |         |         |                         |             |
| P19.2 | GPIO_STD               | P17     | 136       | 112       | 79        |                           |         |         |                         |             |
| P19.3 | GPIO_STD               | P16     | 137       | 113       | 80        |                           |         |         |                         |             |
| P19.4 | GPIO_STD               | N15     | 138       | 114       | NA        |                           |         |         |                         |             |
| P20.0 | GPIO_STD               | N16     | 139       | 115       | NA        |                           |         |         |                         |             |
| P20.1 | GPIO_STD               | M16     | 140       | 116       | NA        |                           |         |         |                         |             |
| P20.2 | GPIO_STD               | M15     | 141       | 117       | NA        |                           |         |         |                         |             |
| P20.3 | GPIO_STD               | M13     | 142       | 118       | NA        |                           |         |         |                         |             |
| P20.4 | GPIO_STD               | L16     | 143       | NA        | NA        |                           |         |         |                         |             |
| P20.5 | GPIO_STD               | L15     | 144       | NA        | NA        |                           |         |         |                         |             |
| P20.6 | GPIO_STD               | K16     | 145       | NA        | NA        |                           |         |         |                         |             |
| P20.7 | GPIO_STD               | K15     | 146       | NA        | NA        |                           |         |         |                         |             |
| P21.0 | GPIO_STD               | N17     | 147       | 119       | 81        |                           |         |         | WCO_IN <sup>[26]</sup>  |             |
| P21.1 | GPIO_STD               | N18     | 148       | 120       | 82        |                           |         |         | WCO_OUT <sup>[26]</sup> |             |
| P21.2 | GPIO_STD               | M17     | 149       | 121       | 83        |                           |         |         | ECO_IN <sup>[26]</sup>  |             |
| P21.3 | GPIO_STD               | M18     | 150       | 122       | 84        |                           |         |         | ECO_OUT <sup>[26]</sup> |             |

**Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) mode, Analog, Smart I/O** (continued)<sup>[24, 25]</sup>

| Name                  | I/O type               | Package |           |           |           | DeepSleep mapping         |                |         | Analog              | SMART I/O |
|-----------------------|------------------------|---------|-----------|-----------|-----------|---------------------------|----------------|---------|---------------------|-----------|
|                       | HCon#0 <sup>[21]</sup> | 272-BGA | 176-TEQFP | 144-TEQFP | 100-TEQFP | HCon#14                   | HCon#29        | HCon#30 |                     |           |
|                       |                        | Pin     | Pin       | Pin       | Pin       | DS #0 <sup>[22, 23]</sup> | DS #1          | DS #2   |                     |           |
| P21.4 <sup>[27]</sup> | GPIO_STD               | L17     | 151       | NA        | NA        |                           |                |         | HIBERNATE_WAKEUP[0] |           |
| P21.5                 | GPIO_STD               | K17     | 157       | 128       | 90        |                           |                |         |                     |           |
| P21.6                 | GPIO_STD               | J17     | 158       | 129       | NA        |                           |                |         |                     |           |
| P21.7                 | GPIO_STD               | J16     | 159       | NA        | NA        |                           | RTC_CAL        |         |                     |           |
| P22.1                 | GPIO_STD               | H18     | 161       | 131       | 92        |                           |                |         | EXT_PS_CTL0         |           |
| P22.2                 | GPIO_STD               | G18     | 162       | 132       | 93        |                           |                |         | EXT_PS_CTL1         |           |
| P22.3                 | GPIO_STD               | F18     | 163       | 133       | 94        |                           |                |         | EXT_PS_CTL2         |           |
| P22.4                 | GPIO_STD               | H17     | 164       | 134       | NA        |                           |                |         |                     |           |
| P22.5                 | GPIO_STD               | H16     | 165       | 135       | NA        |                           |                |         |                     |           |
| P22.6                 | GPIO_STD               | H15     | 166       | 136       | NA        |                           |                |         |                     |           |
| P22.7                 | GPIO_STD               | G17     | 167       | NA        | NA        |                           |                |         |                     |           |
| P23.0                 | GPIO_STD               | G16     | 168       | 137       | NA        |                           |                |         |                     |           |
| P23.1                 | GPIO_STD               | G15     | 169       | 138       | NA        |                           |                |         |                     |           |
| P23.2                 | GPIO_STD               | G13     | 170       | NA        | NA        |                           |                |         |                     |           |
| P23.3                 | GPIO_STD               | F17     | 171       | 139       | 95        |                           |                |         |                     |           |
| P23.4                 | GPIO_STD               | F16     | 172       | 140       | 96        |                           | SWJ_SWO_TDO    |         |                     |           |
| P23.5                 | GPIO_STD               | F15     | 173       | 141       | 97        |                           | SWJ_SWCLK_TCLK |         |                     |           |
| P23.6                 | GPIO_STD               | E18     | 174       | 142       | 98        |                           | SWJ_SWDIO_TMS  |         |                     |           |
| P23.7                 | GPIO_STD               | E17     | 175       | 143       | 99        |                           | SWJ_SWDOE_TDI  |         | HIBERNATE_WAKEUP[1] |           |
| P24.0                 | HSIO_STD               | J3      | NA        | NA        | NA        |                           |                |         |                     |           |
| P24.1                 | HSIO_STD               | J4      | NA        | NA        | NA        |                           |                |         |                     |           |
| P24.2                 | HSIO_STD               | K1      | NA        | NA        | NA        |                           |                |         |                     |           |
| P24.3                 | HSIO_STD               | K2      | NA        | NA        | NA        |                           |                |         |                     |           |
| P24.4                 | HSIO_STD               | K3      | NA        | NA        | NA        |                           |                |         |                     |           |
| P25.0                 | HSIO_STD               | K4      | NA        | NA        | NA        |                           |                |         |                     |           |
| P25.1                 | HSIO_STD               | L1      | NA        | NA        | NA        |                           |                |         |                     |           |
| P25.2                 | HSIO_STD               | L2      | NA        | NA        | NA        |                           |                |         |                     |           |
| P25.3                 | HSIO_STD               | L3      | NA        | NA        | NA        |                           |                |         |                     |           |

**Notes**

26.I/O pins that support an oscillator function (WCO or ECO) must be configured for high-impedance if the oscillator is enabled.

27.This I/O has increased leakage to ground when the V<sub>DD</sub> supply is below the POR threshold.

**Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) mode, Analog, Smart I/O** (continued)<sup>[24, 25]</sup>

| Name  | I/O type               | Package |           |           |           | DeepSleep mapping         |         |         | Analog | SMART I/O |
|-------|------------------------|---------|-----------|-----------|-----------|---------------------------|---------|---------|--------|-----------|
|       | HCon#0 <sup>[21]</sup> | 272-BGA | 176-TEQFP | 144-TEQFP | 100-TEQFP | HCon#14                   | HCon#29 | HCon#30 |        |           |
|       |                        | Pin     | Pin       | Pin       | Pin       | DS #0 <sup>[22, 23]</sup> | DS #1   | DS #2   |        |           |
| P25.4 | HSIO_STD               | L4      | NA        | NA        | NA        |                           |         |         |        |           |
| P25.5 | HSIO_STD               | M2      | NA        | NA        | NA        |                           |         |         |        |           |
| P25.6 | HSIO_STD               | M3      | NA        | NA        | NA        |                           |         |         |        |           |
| P25.7 | HSIO_STD               | M4      | NA        | NA        | NA        |                           |         |         |        |           |
| P26.0 | GPIO_STD               | T8      | NA        | NA        | NA        |                           |         |         |        |           |
| P26.1 | GPIO_STD               | R8      | NA        | NA        | NA        |                           |         |         |        |           |
| P26.2 | GPIO_STD               | V9      | NA        | NA        | NA        |                           |         |         |        |           |
| P26.3 | GPIO_STD               | U9      | NA        | NA        | NA        |                           |         |         |        |           |
| P26.4 | GPIO_STD               | T9      | NA        | NA        | NA        |                           |         |         |        |           |
| P26.5 | GPIO_STD               | R9      | NA        | NA        | NA        |                           |         |         |        |           |
| P26.6 | GPIO_STD               | V10     | NA        | NA        | NA        |                           |         |         |        |           |
| P26.7 | GPIO_STD               | U10     | NA        | NA        | NA        |                           |         |         |        |           |
| P27.0 | GPIO_STD               | T10     | NA        | NA        | NA        |                           |         |         |        |           |
| P27.1 | GPIO_STD               | R10     | NA        | NA        | NA        |                           |         |         |        |           |
| P27.2 | GPIO_STD               | V11     | NA        | NA        | NA        |                           |         |         |        |           |
| P27.3 | GPIO_STD               | U11     | NA        | NA        | NA        |                           |         |         |        |           |
| P27.4 | GPIO_STD               | T11     | NA        | NA        | NA        |                           |         |         |        |           |
| P27.5 | GPIO_STD               | R11     | NA        | NA        | NA        |                           |         |         |        |           |
| P27.6 | GPIO_STD               | T12     | NA        | NA        | NA        |                           |         |         |        |           |
| P27.7 | GPIO_STD               | R12     | NA        | NA        | NA        |                           |         |         |        |           |
| P28.0 | GPIO_STD               | E16     | NA        | NA        | NA        |                           |         |         |        |           |
| P28.1 | GPIO_STD               | E15     | NA        | NA        | NA        |                           |         |         |        |           |
| P28.2 | GPIO_STD               | D18     | NA        | NA        | NA        |                           |         |         |        |           |
| P28.3 | GPIO_STD               | D17     | NA        | NA        | NA        |                           |         |         |        |           |
| P28.4 | GPIO_STD               | D16     | NA        | NA        | NA        |                           |         |         |        |           |
| P28.5 | GPIO_STD               | C18     | NA        | NA        | NA        |                           |         |         |        |           |
| P28.6 | GPIO_STD               | C17     | NA        | NA        | NA        |                           |         |         |        |           |
| P28.7 | GPIO_STD               | C16     | NA        | NA        | NA        |                           |         |         |        |           |
| P29.0 | GPIO_STD               | A11     | NA        | NA        | NA        |                           |         |         |        |           |
| P29.1 | GPIO_STD               | A10     | NA        | NA        | NA        |                           |         |         |        |           |
| P29.2 | GPIO_STD               | B10     | NA        | NA        | NA        |                           |         |         |        |           |

**Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) mode, Analog, Smart I/O** (continued)<sup>[24, 25]</sup>

| Name  | I/O type               | Package |           |           |           | DeepSleep mapping         |         |         | Analog    | SMART I/O |
|-------|------------------------|---------|-----------|-----------|-----------|---------------------------|---------|---------|-----------|-----------|
|       | HCon#0 <sup>[21]</sup> | 272-BGA | 176-TEQFP | 144-TEQFP | 100-TEQFP | HCon#14                   | HCon#29 | HCon#30 |           |           |
|       |                        | Pin     | Pin       | Pin       | Pin       | DS #0 <sup>[22, 23]</sup> | DS #1   | DS #2   |           |           |
| P29.3 | GPIO_STD               | C10     | NA        | NA        | NA        |                           |         |         |           |           |
| P29.4 | GPIO_STD               | D10     | NA        | NA        | NA        |                           |         |         |           |           |
| P29.5 | GPIO_STD               | A9      | NA        | NA        | NA        |                           |         |         |           |           |
| P29.6 | GPIO_STD               | B9      | NA        | NA        | NA        |                           |         |         |           |           |
| P29.7 | GPIO_STD               | C9      | NA        | NA        | NA        |                           |         |         |           |           |
| P30.0 | GPIO_STD               | B7      | NA        | NA        | NA        |                           |         |         |           |           |
| P30.1 | GPIO_STD               | C7      | NA        | NA        | NA        |                           |         |         |           |           |
| P30.2 | GPIO_STD               | D7      | NA        | NA        | NA        |                           |         |         |           |           |
| P30.3 | GPIO_STD               | F7      | NA        | NA        | NA        |                           |         |         |           |           |
| P31.0 | GPIO_STD               | A5      | NA        | NA        | NA        |                           |         |         |           |           |
| P31.1 | GPIO_STD               | B5      | NA        | NA        | NA        |                           |         |         |           |           |
| P31.2 | GPIO_STD               | A4      | NA        | NA        | NA        |                           |         |         |           |           |
| P32.0 | GPIO_STD               | C1      | NA        | NA        | NA        |                           |         |         | ADC[0]_8  |           |
| P32.1 | GPIO_STD               | C2      | NA        | NA        | NA        |                           |         |         | ADC[0]_9  |           |
| P32.2 | GPIO_STD               | D1      | NA        | NA        | NA        |                           |         |         | ADC[0]_10 |           |
| P32.3 | GPIO_STD               | D2      | NA        | NA        | NA        |                           |         |         | ADC[0]_11 |           |
| P32.4 | GPIO_STD               | D3      | NA        | NA        | NA        |                           |         |         | ADC[0]_12 |           |
| P32.5 | GPIO_STD               | D4      | NA        | NA        | NA        |                           |         |         | ADC[0]_13 |           |
| P32.6 | GPIO_STD               | E3      | NA        | NA        | NA        |                           |         |         | ADC[0]_14 |           |
| P32.7 | GPIO_STD               | E4      | NA        | NA        | NA        |                           |         |         | ADC[0]_15 |           |

## 12 Power pin assignments

**Table 12-1** Power pin assignments

| Power pin name       | Package                                                                                                 |                                   |                                  |                               | Remarks                                                                                   |
|----------------------|---------------------------------------------------------------------------------------------------------|-----------------------------------|----------------------------------|-------------------------------|-------------------------------------------------------------------------------------------|
|                      | 272-BGA                                                                                                 | 176-TEQFP                         | 144-TEQFP                        | 100-TEQFP                     |                                                                                           |
| VDDD                 | F8, H13, J13, K13, L13, N11                                                                             | 22, 43, 110, 132, 153, 176        | 18, 35, 90, 108, 124, 144        | 12, 24, 62, 75, 86, 100       | Main digital supply                                                                       |
| VSSD                 | A1, A18, D9, G7, G12, H9, H10, H11, J9, J10, J11, J15, K9, K10, K11, M7, M12, R5, R14, V1, V18, L9, L10 | 1, 23, 45, 89, 114, 133, 154, 155 | 1, 19, 37, 73, 94, 109, 125, 126 | 1, 13, 26, 51, 66, 76, 87, 88 | Main digital ground                                                                       |
| VSSD_1               | L11                                                                                                     | NA                                | NA                               | NA                            | Digital ground                                                                            |
| VSSD_2               | L18, P18                                                                                                | NA                                | NA                               | NA                            | Noise guard for ECO inputs                                                                |
| VDDIO_1              | F9, F10, F11                                                                                            | 44                                | 36                               | 25                            | I/O supply (except analog I/Os on VDDA)                                                   |
| VDDIO_2              | N8, N9, N10                                                                                             | 88                                | 72                               | 50                            | I/O supply (except analog I/Os on VDDA)                                                   |
| VDDIO_3              | H6, J6                                                                                                  | NA                                | NA                               | NA                            | I/O supply for high speed domain#0 (HSIO_STD), P24, P25                                   |
| VSSIO_3              | H8, J8                                                                                                  | NA                                | NA                               | NA                            | HSIO ground                                                                               |
| VCCD <sup>[28]</sup> | F6, F13, N6, N13                                                                                        | 46, 47, 111, 112, 113, 156        | 38, 39, 91, 92, 93, 127          | 27, 28, 63, 64, 65, 89        | Main regulated supply. Driven by LDO regulator (either internal LDO or external LDO/PMIC) |
| VREFH                | K6                                                                                                      | 79                                | 65                               | 44                            | High-reference voltage for SAR ADCs                                                       |
| VREFL                | K8                                                                                                      | 76                                | 62                               | 41                            | Low-reference voltage for SAR ADCs                                                        |
| VDDA                 | L6                                                                                                      | 78                                | 64                               | 43                            | Main analog supply for SAR ADCs                                                           |
| VSSA                 | L8                                                                                                      | 77                                | 63                               | 42                            | Main analog ground                                                                        |
| XRES_L               | K18                                                                                                     | 152                               | 123                              | 85                            | Active LOW external reset input                                                           |
| DRV_VOUT             | J18                                                                                                     | 160                               | 130                              | 91                            | Dedicated external supply control pin                                                     |

### Note

28. The V<sub>CCD</sub> pins must be connected together to ensure a low-impedance connection. (see the requirement in [Figure 26-2](#))

# 13 Alternate function pin assignments

**Table 13-1** Alternate pin functions in active mode<sup>[23, 31, 32]</sup>

| Port<br>pin | Active mapping         |            |             |             |             |              |              |               |          |           |         |         |                                        |         |            |             |
|-------------|------------------------|------------|-------------|-------------|-------------|--------------|--------------|---------------|----------|-----------|---------|---------|----------------------------------------|---------|------------|-------------|
|             | HCon#8 <sup>[29]</sup> | HCon#9     | HCon#10     | HCon#11     | HCon#16     | HCon#17      | HCon#18      | HCon#19       | HCon#20  | HCon#21   | HCon#22 | HCon#23 | HCon#24                                | HCon#25 | HCon#26    | HCon#27     |
|             | ACT #0 <sup>[30]</sup> | ACT #1     | ACT #2      | ACT #3      | ACT #4      | ACT #5       | ACT #6       | ACT #7        | ACT #8   | ACT #9    | ACT #10 | ACT #11 | ACT #12                                | ACT #13 | ACT #14    | ACT #15     |
| P0.0        | PWM0_18                | PWM0_22_N  | TC0_18_TR0  | TC0_22_TR1  |             | SCB0_RX (0)  | SCB7_SDA (2) |               | LIN1_RX  |           |         |         |                                        |         |            |             |
| P0.1        | PWM0_17                | PWM0_18_N  | TC0_17_TR0  | TC0_18_TR1  |             | SCB0_TX (0)  | SCB7_SCL (2) |               | LIN1_TX  |           |         |         |                                        |         |            |             |
| P0.2        | PWM0_14                | PWM0_17_N  | TC0_14_TR0  | TC0_17_TR1  |             | SCB0_RTS (0) |              | SCB4_MISO (2) | LIN1_EN  | CAN0_1_TX |         |         |                                        |         |            |             |
| P0.3        | PWM0_13                | PWM0_14_N  | TC0_13_TR0  | TC0_14_TR1  |             | SCB0_CTS (0) |              | SCB4_MOSI (2) |          | CAN0_1_RX |         |         |                                        |         |            |             |
| P1.0        | PWM0_12                | PWM0_13_N  | TC0_12_TR0  | TC0_13_TR1  | PWM0_H_4    |              |              | SCB4_CLK (2)  |          |           |         |         |                                        |         |            |             |
| P1.1        | PWM0_11                | PWM0_12_N  | TC0_11_TR0  | TC0_12_TR1  | PWM0_H_5    |              |              | SCB4_SEL0 (2) |          |           |         |         |                                        |         |            |             |
| P1.2        | PWM0_10                | PWM0_11_N  | TC0_10_TR0  | TC0_11_TR1  | PWM0_H_6    |              |              |               | LIN0_RX  |           |         |         |                                        |         | TRIG_IN[0] |             |
| P1.3        | PWM0_8                 | PWM0_10_N  | TC0_8_TR0   | TC0_10_TR1  | PWM0_H_7    |              |              |               | LIN0_TX  |           |         |         |                                        |         | TRIG_IN[1] |             |
| P1.4        |                        |            |             |             |             |              |              |               |          |           | LIN8_RX |         |                                        |         |            |             |
| P2.0        | PWM0_7                 | PWM0_8_N   | TC0_7_TR0   | TC0_8_TR1   | TC0_H_4_TR0 | SCB7_RX (0)  |              | SCB7_MISO (0) | LIN0_RX  | CAN0_0_TX |         |         |                                        |         | TRIG_IN[2] |             |
| P2.1        | PWM0_6                 | PWM0_7_N   | TC0_6_TR0   | TC0_7_TR1   | TC0_H_5_TR0 | SCB7_TX (0)  | SCB7_SDA (0) | SCB7_MOSI (0) | LIN0_TX  | CAN0_0_RX |         |         |                                        |         | TRIG_IN[3] |             |
| P2.2        | PWM0_5                 | PWM0_6_N   | TC0_5_TR0   | TC0_6_TR1   | TC0_H_6_TR0 | SCB7_RTS (0) | SCB7_SCL (0) | SCB7_CLK (0)  | LIN0_EN  |           |         |         | ETH0_RX_ER (0)                         |         | TRIG_IN[4] |             |
| P2.3        | PWM0_4                 | PWM0_5_N   | TC0_4_TR0   | TC0_5_TR1   | TC0_H_7_TR0 | SCB7_CTS (0) |              | SCB7_SEL0 (0) | LIN5_RX  |           |         |         | ETH0_ETH_TSU -<br>TIMER_CMP_VAL<br>(0) |         | TRIG_IN[5] |             |
| P2.4        | PWM0_3                 | PWM0_4_N   | TC0_3_TR0   | TC0_4_TR1   | PWM0_H_4_N  |              |              | SCB7_SEL1 (0) | LIN5_TX  |           |         |         |                                        |         | TRIG_IN[6] |             |
| P2.5        | PWM0_2                 | PWM0_3_N   | TC0_2_TR0   | TC0_3_TR1   | PWM0_H_5_N  |              |              | SCB7_SEL2 (0) | LIN5_EN  |           |         |         |                                        |         | TRIG_IN[7] |             |
| P2.6        |                        |            |             |             |             |              |              |               |          |           |         |         |                                        |         |            |             |
| P2.7        |                        |            |             |             |             |              |              |               | LIN11_RX |           |         |         |                                        |         |            |             |
| P3.0        | PWM0_1                 | PWM0_2_N   | TC0_1_TR0   | TC0_2_TR1   | PWM0_H_6_N  | SCB6_RX (0)  |              | SCB6_MISO (0) |          | CAN0_3_TX |         |         | ETH0_MDIO (0)                          |         |            | TRIG_DBG[0] |
| P3.1        | PWM0_0                 | PWM0_1_N   | TC0_0_TR0   | TC0_1_TR1   | PWM0_H_7_N  | SCB6_TX (0)  | SCB6_SDA (0) | SCB6_MOSI (0) |          | CAN0_3_RX |         |         | ETH0_MDC (0)                           |         |            | TRIG_DBG[1] |
| P3.2        | PWM0_M_3               | PWM0_0_N   | TC0_M_3_TR0 | TC0_0_TR1   | TC0_H_4_TR1 | SCB6_RTS (0) | SCB6_SCL (0) | SCB6_CLK (0)  |          |           |         |         |                                        |         |            |             |
| P3.3        | PWM0_M_2               | PWM0_M_3_N | TC0_M_2_TR0 | TC0_M_3_TR1 | TC0_H_5_TR1 | SCB6_CTS (0) |              | SCB6_SEL0 (0) |          |           |         |         |                                        |         |            |             |
| P3.4        | PWM0_M_1               | PWM0_M_2_N | TC0_M_1_TR0 | TC0_M_2_TR1 | TC0_H_6_TR1 |              |              | SCB6_SEL1 (0) | LIN1_RX  |           |         |         |                                        |         |            |             |
| P3.5        | PWM0_M_0               | PWM0_M_1_N | TC0_M_0_TR0 | TC0_M_1_TR1 | TC0_H_7_TR1 |              |              | SCB6_SEL2 (0) | LIN1_TX  |           |         |         |                                        |         |            |             |

## Notes

29.High Speed I/O matrix connection (HCon) reference as per [Table 10-1](#).

30.Active Mode ordering (ACT #0, ACT #1, and so on) does not have any impact on configuring alternate functions; the HSIOM module handles the alternate function assignments.

31.Refer to [Table 13-2](#) for more information on pin multiplexer abbreviations used.

32.For any function marked with an identifier (n), the AC timing is only guaranteed within the respective group "n".

**Table 13-1** Alternate pin functions in active mode (continued)<sup>[23, 31, 32]</sup>

| Port<br>pin | Active mapping         |            |             |             |               |              |              |               |          |           |         |                      |         |                                        |             |            |
|-------------|------------------------|------------|-------------|-------------|---------------|--------------|--------------|---------------|----------|-----------|---------|----------------------|---------|----------------------------------------|-------------|------------|
|             | HCon#8 <sup>[29]</sup> | HCon#9     | HCon#10     | HCon#11     | HCon#16       | HCon#17      | HCon#18      | HCon#19       | HCon#20  | HCon#21   | HCon#22 | HCon#23              | HCon#24 | HCon#25                                | HCon#26     | HCon#27    |
|             | ACT #0 <sup>[30]</sup> | ACT #1     | ACT #2      | ACT #3      | ACT #4        | ACT #5       | ACT #6       | ACT #7        | ACT #8   | ACT #9    | ACT #10 | ACT #11              | ACT #12 | ACT #13                                | ACT #14     | ACT #15    |
| P3.6        |                        |            |             |             |               |              |              | SCB8_SEL2 (0) | LIN11_TX | CAN1_2_TX |         |                      |         |                                        |             |            |
| P3.7        |                        |            |             |             |               |              |              |               | LIN11_EN | CAN1_2_RX |         |                      |         |                                        |             |            |
| P4.0        | PWM0_4                 | PWM0_M_0_N | TC0_4_TR0   | TC0_M_0_TR1 | EXT_MUX[0]_0  | SCB5_RX (0)  |              | SCB5_MISO (0) | LIN1_RX  |           |         |                      |         |                                        | TRIG_IN[10] |            |
| P4.1        | PWM0_5                 | PWM0_4_N   | TC0_5_TR0   | TC0_4_TR1   | EXT_MUX[0]_1  | SCB5_TX (0)  | SCB5_SDA (0) | SCB5_MOSI (0) | LIN1_TX  |           |         |                      |         |                                        | TRIG_IN[11] |            |
| P4.2        | PWM0_6                 | PWM0_5_N   | TC0_6_TR0   | TC0_5_TR1   | EXT_MUX[0]_2  | SCB5_RTS (0) | SCB5_SCL (0) | SCB5_CLK (0)  | LIN1_EN  |           |         |                      |         |                                        | TRIG_IN[12] |            |
| P4.3        | PWM0_7                 | PWM0_6_N   | TC0_7_TR0   | TC0_6_TR1   | EXT_MUX[0]_EN | SCB5_CTS (0) |              | SCB5_SEL0 (0) |          | CAN0_1_TX |         |                      |         |                                        | TRIG_IN[13] |            |
| P4.4        | PWM0_8                 | PWM0_7_N   | TC0_8_TR0   | TC0_7_TR1   |               |              | LIN15_RX     | SCB5_SEL1 (0) |          | CAN0_1_RX |         |                      |         |                                        |             |            |
| P5.0        | PWM0_9                 | PWM0_8_N   | TC0_9_TR0   | TC0_8_TR1   |               |              | LIN15_TX     | SCB5_SEL2 (0) | LIN7_RX  |           |         |                      |         |                                        |             |            |
| P5.1        | PWM0_10                | PWM0_9_N   | TC0_10_TR0  | TC0_9_TR1   |               |              |              | SCB9_SEL3 (1) | LIN7_TX  |           |         |                      |         |                                        |             |            |
| P5.2        | PWM0_11                | PWM0_10_N  | TC0_11_TR0  | TC0_10_TR1  |               |              | LIN10_RX     |               | LIN7_EN  |           |         |                      |         |                                        |             |            |
| P5.3        | PWM0_12                | PWM0_11_N  | TC0_12_TR0  | TC0_11_TR1  |               |              | LIN10_TX     |               | LIN2_RX  |           |         |                      |         |                                        |             |            |
| P5.4        | PWM0_13                | PWM0_12_N  | TC0_13_TR0  | TC0_12_TR1  |               |              |              |               | LIN2_TX  |           |         | LIN9_RX              |         |                                        |             |            |
| P5.5        | PWM0_14                | PWM0_13_N  | TC0_14_TR0  | TC0_13_TR1  |               |              |              |               | LIN2_EN  |           |         | LIN9_TX              |         |                                        |             |            |
| P6.0        | PWM0_M_0               | PWM0_14_N  | TC0_M_0_TR0 | TC0_14_TR1  |               | SCB4_RX (0)  |              | SCB4_MISO (0) | LIN3_RX  |           |         | LIN9_EN              |         |                                        |             |            |
| P6.1        | PWM0_0                 | PWM0_M_0_N | TC0_0_TR0   | TC0_M_0_TR1 |               | SCB4_TX (0)  | SCB4_SDA (0) | SCB4_MOSI (0) | LIN3_TX  |           |         |                      |         |                                        |             |            |
| P6.2        | PWM0_M_1               | PWM0_0_N   | TC0_M_1_TR0 | TC0_0_TR1   |               | SCB4_RTS (0) | SCB4_SCL (0) | SCB4_CLK (0)  | LIN3_EN  | CAN0_2_TX |         |                      |         | SDHC_CARD -<br>MECH_WRITE_P<br>ROT (0) |             |            |
| P6.3        | PWM0_1                 | PWM0_M_1_N | TC0_1_TR0   | TC0_M_1_TR1 |               | SCB4_CTS (0) |              | SCB4_SEL0 (0) | LIN4_RX  | CAN0_2_RX |         | SPIHB_CLK<br>(0)     |         | SDHC_CARD -<br>CARD_CMD (0)            |             | CAL_SUP_NZ |
| P6.4        | PWM0_M_2               | PWM0_1_N   | TC0_M_2_TR0 | TC0_1_TR1   |               |              |              | SCB4_SEL1 (0) | LIN4_TX  |           |         | SPIHB_RWD<br>S (0)   |         | SDHC_CARD -<br>CLK_CARD (0)            |             |            |
| P6.5        | PWM0_2                 | PWM0_M_2_N | TC0_2_TR0   | TC0_M_2_TR1 |               |              |              | SCB4_SEL2 (0) | LIN4_EN  |           |         | SPIHB_SEL0<br>(0)    |         | SDHC_CARD -<br>DETECT_N (0)            |             |            |
| P6.6        | PWM0_M_3               | PWM0_2_N   | TC0_M_3_TR0 | TC0_2_TR1   |               |              |              | SCB4_SEL3 (0) |          |           |         |                      |         |                                        | TRIG_IN[8]  |            |
| P6.7        | PWM0_3                 | PWM0_M_3_N | TC0_3_TR0   | TC0_M_3_TR1 |               |              |              |               |          |           |         |                      |         |                                        | TRIG_IN[9]  |            |
| P7.0        | PWM0_M_4               | PWM0_3_N   | TC0_M_4_TR0 | TC0_3_TR1   |               | SCB5_RX (1)  |              | SCB5_MISO (1) | LIN4_RX  |           |         | SPIHB_SEL1<br>(0)    |         | SDHC_CARD -<br>CARD_IF_P-<br>WR_EN (0) |             |            |
| P7.1        | PWM0_15                | PWM0_M_4_N | TC0_15_TR0  | TC0_M_4_TR1 |               | SCB5_TX (1)  | SCB5_SDA (1) | SCB5_MOSI (1) | LIN4_TX  |           |         | SPIHB -<br>DATA0 (0) |         | SDHC_CARD -<br>DAT_3TO0_0 (0)          |             |            |
| P7.2        | PWM0_M_5               | PWM0_15_N  | TC0_M_5_TR0 | TC0_15_TR1  |               | SCB5_RTS (1) | SCB5_SCL (1) | SCB5_CLK (1)  | LIN4_EN  |           |         | SPIHB -<br>DATA1 (0) |         | SDHC_CARD -<br>DAT_3TO0_1 (0)          |             |            |
| P7.3        | PWM0_16                | PWM0_M_5_N | TC0_16_TR0  | TC0_M_5_TR1 |               | SCB5_CTS (1) |              | SCB5_SEL0 (1) |          |           |         | SPIHB -<br>DATA2 (0) |         | SDHC_CARD -<br>DAT_3TO0_2 (0)          |             |            |
| P7.4        | PWM0_M_6               | PWM0_16_N  | TC0_M_6_TR0 | TC0_16_TR1  |               |              |              | SCB5_SEL1 (1) |          |           |         | SPIHB -<br>DATA3 (0) |         | SDHC_CARD -<br>DAT_3TO0_3 (0)          |             |            |
| P7.5        | PWM0_17                | PWM0_M_6_N | TC0_17_TR0  | TC0_M_6_TR1 |               |              | LIN10_RX     | SCB5_SEL2 (1) |          |           |         | SPIHB -<br>DATA4 (0) |         | SDHC_CARD -<br>DAT_7TO4_0 (0)          |             |            |
| P7.6        | PWM0_M_7               | PWM0_17_N  | TC0_M_7_TR0 | TC0_17_TR1  |               |              | LIN10_TX     |               |          |           |         |                      |         |                                        | TRIG_IN[16] |            |

**Table 13-1** Alternate pin functions in active mode (continued)<sup>[23, 31, 32]</sup>

| Port<br>pin | Active mapping         |            |            |             |               |              |              |               |         |           |         |                      |         |                               |             |             |
|-------------|------------------------|------------|------------|-------------|---------------|--------------|--------------|---------------|---------|-----------|---------|----------------------|---------|-------------------------------|-------------|-------------|
|             | HCon#8 <sup>[29]</sup> | HCon#9     | HCon#10    | HCon#11     | HCon#16       | HCon#17      | HCon#18      | HCon#19       | HCon#20 | HCon#21   | HCon#22 | HCon#23              | HCon#24 | HCon#25                       | HCon#26     | HCon#27     |
|             | ACT #0 <sup>[30]</sup> | ACT #1     | ACT #2     | ACT #3      | ACT #4        | ACT #5       | ACT #6       | ACT #7        | ACT #8  | ACT #9    | ACT #10 | ACT #11              | ACT #12 | ACT #13                       | ACT #14     | ACT #15     |
| P7.7        | PWM0_18                | PWM0_M_7_N | TC0_18_TR0 | TC0_M_7_TR1 |               |              | LIN10_EN     |               |         |           |         |                      |         |                               | TRIG_IN[17] |             |
| P8.0        | PWM0_19                | PWM0_18_N  | TC0_19_TR0 | TC0_18_TR1  |               |              |              |               | LIN2_RX | CAN0_0_TX |         | SPIHB -<br>DATA5 (0) |         | SDHC_CARD -<br>DAT_7TO4_1 (0) |             |             |
| P8.1        | PWM0_20                | PWM0_19_N  | TC0_20_TR0 | TC0_19_TR1  |               |              |              |               | LIN2_TX | CAN0_0_RX |         | SPIHB -<br>DATA6 (0) |         | SDHC_CARD -<br>DAT_7TO4_2 (0) | TRIG_IN[14] |             |
| P8.2        | PWM0_21                | PWM0_20_N  | TC0_21_TR0 | TC0_20_TR1  |               |              |              |               | LIN2_EN |           |         | SPIHB -<br>DATA7 (0) |         | SDHC_CARD -<br>DAT_7TO4_3 (0) | TRIG_IN[15] |             |
| P8.3        | PWM0_22                | PWM0_21_N  | TC0_22_TR0 | TC0_21_TR1  |               |              |              |               |         |           |         |                      |         |                               |             | TRIG_DBG[0] |
| P8.4        | PWM0_23                | PWM0_22_N  | TC0_23_TR0 | TC0_22_TR1  |               |              |              |               |         |           |         |                      |         |                               |             | TRIG_DBG[1] |
| P9.0        | PWM0_24                | PWM0_23_N  | TC0_24_TR0 | TC0_23_TR1  |               |              |              |               |         |           |         |                      |         |                               |             |             |
| P9.1        | PWM0_25                | PWM0_24_N  | TC0_25_TR0 | TC0_24_TR1  |               |              |              |               |         | LIN12_RX  |         |                      |         |                               |             |             |
| P9.2        | PWM0_26                | PWM0_25_N  | TC0_26_TR0 | TC0_25_TR1  |               |              |              |               |         | LIN12_TX  |         |                      |         |                               |             |             |
| P9.3        | PWM0_27                | PWM0_26_N  | TC0_27_TR0 | TC0_26_TR1  |               |              |              |               |         | LIN12_EN  |         |                      |         |                               |             |             |
| P10.0       | PWM0_28                | PWM0_27_N  | TC0_28_TR0 | TC0_27_TR1  |               | SCB4_RX (1)  |              | SCB4_MISO (1) | LIN7_RX |           |         |                      |         |                               | TRIG_IN[18] |             |
| P10.1       | PWM0_29                | PWM0_28_N  | TC0_29_TR0 | TC0_28_TR1  |               | SCB4_TX (1)  | SCB4_SDA (1) | SCB4_MOSI (1) | LIN7_TX |           |         |                      |         |                               | TRIG_IN[19] |             |
| P10.2       | PWM0_30                | PWM0_29_N  | TC0_30_TR0 | TC0_29_TR1  |               | SCB4_RTS (1) | SCB4_SCL (1) | SCB4_CLK (1)  |         |           | LIN8_RX |                      |         |                               |             |             |
| P10.3       | PWM0_31                | PWM0_30_N  | TC0_31_TR0 | TC0_30_TR1  |               | SCB4_CTS (1) |              | SCB4_SEL0 (1) |         |           | LIN8_TX |                      |         |                               |             |             |
| P10.4       | PWM0_32                | PWM0_31_N  | TC0_32_TR0 | TC0_31_TR1  |               |              |              | SCB4_SEL1 (1) |         |           | LIN8_EN |                      |         |                               |             |             |
| P10.5       | PWM0_33                | PWM0_32_N  | TC0_33_TR0 | TC0_32_TR1  |               |              |              | SCB4_SEL2 (1) |         | LIN13_RX  |         |                      |         |                               |             |             |
| P10.6       |                        | PWM0_33_N  |            | TC0_33_TR1  |               |              |              |               |         | LIN13_TX  | PWM0_34 |                      |         |                               |             |             |
| P10.7       | PWM0_35                | PWM0_34_N  | TC0_35_TR0 | TC0_34_TR1  |               |              |              |               |         | LIN13_EN  |         |                      |         |                               |             |             |
| P11.0       | PWM0_61                | PWM0_62_N  | TC0_61_TR0 | TC0_62_TR1  |               |              |              |               |         |           |         |                      |         | AUDIOSS0_MCLK                 |             |             |
| P11.1       | PWM0_60                | PWM0_61_N  | TC0_60_TR0 | TC0_61_TR1  |               |              |              |               |         |           |         |                      |         | AUDIOSS0_TX_SCK               |             |             |
| P11.2       | PWM0_59                | PWM0_60_N  | TC0_59_TR0 | TC0_60_TR1  |               |              |              |               |         |           |         |                      |         | AUDIOSS0_TX_WS                |             |             |
| P12.0       | PWM0_36                |            | TC0_36_TR0 |             |               | SCB8_RX (0)  |              | SCB8_MISO (0) |         | CAN0_2_TX |         | PWM0_35_N            |         | AUDIOSS0_TX_SDO               | TRIG_IN[20] |             |
| P12.1       | PWM0_37                | PWM0_36_N  | TC0_37_TR0 | TC0_36_TR1  |               | SCB8_TX (0)  | SCB8_SDA (0) | SCB8_MOSI (0) | LIN6_EN | CAN0_2_RX |         |                      |         | AUDIOSS0_CLK_I2S_IF           | TRIG_IN[21] |             |
| P12.2       | PWM0_38                | PWM0_37_N  | TC0_38_TR0 | TC0_37_TR1  | EXT_MUX[1]_EN | SCB8_RTS (0) | SCB8_SCL (0) | SCB8_CLK (0)  | LIN6_RX |           |         |                      |         | AUDIOSS0_RX_SCK               |             |             |
| P12.3       | PWM0_39                | PWM0_38_N  | TC0_39_TR0 | TC0_38_TR1  | EXT_MUX[1]_0  | SCB8_CTS (0) |              | SCB8_SEL0 (0) | LIN6_TX |           |         |                      |         | AUDIOSS0_RX_WS                |             |             |
| P12.4       | PWM0_40                | PWM0_39_N  | TC0_40_TR0 | TC0_39_TR1  | EXT_MUX[1]_1  |              |              | SCB8_SEL1 (0) |         | CAN1_1_TX |         |                      |         | AUDIOSS0_RX_SDI               |             |             |
| P12.5       | PWM0_41                | PWM0_40_N  | TC0_41_TR0 | TC0_40_TR1  | EXT_MUX[1]_2  |              |              |               |         | CAN1_1_RX |         |                      |         |                               |             |             |
| P12.6       | PWM0_42                | PWM0_41_N  | TC0_42_TR0 | TC0_41_TR1  |               |              |              |               |         |           |         |                      |         |                               |             |             |
| P12.7       | PWM0_43                | PWM0_42_N  | TC0_43_TR0 | TC0_42_TR1  |               |              |              |               |         |           |         |                      |         |                               |             |             |

**Table 13-1** Alternate pin functions in active mode (continued)<sup>[23, 31, 32]</sup>

| Port<br>pin | Active mapping         |             |              |              |               |               |              |               |          |               |         |         |         |                     |             |         |
|-------------|------------------------|-------------|--------------|--------------|---------------|---------------|--------------|---------------|----------|---------------|---------|---------|---------|---------------------|-------------|---------|
|             | HCon#8 <sup>[29]</sup> | HCon#9      | HCon#10      | HCon#11      | HCon#16       | HCon#17       | HCon#18      | HCon#19       | HCon#20  | HCon#21       | HCon#22 | HCon#23 | HCon#24 | HCon#25             | HCon#26     | HCon#27 |
|             | ACT #0 <sup>[30]</sup> | ACT #1      | ACT #2       | ACT #3       | ACT #4        | ACT #5        | ACT #6       | ACT #7        | ACT #8   | ACT #9        | ACT #10 | ACT #11 | ACT #12 | ACT #13             | ACT #14     | ACT #15 |
| P13.0       | PWM0_M_8               | PWM0_43_N   | TC0_M_8_TR0  | TC0_43_TR1   | EXT_MUX[2]_0  | SCB3_RX (0)   |              |               | LIN3_RX  | SCB3_MISO (0) |         |         |         | AUDIOSS1_MCLK       |             |         |
| P13.1       | PWM0_44                | PWM0_M_8_N  | TC0_44_TR0   | TC0_M_8_TR1  | EXT_MUX[2]_1  | SCB3_TX (0)   | SCB3_SDA (0) |               | LIN3_TX  | SCB3_MOSI (0) |         |         |         | AUDIOSS1_TX_SCK     |             |         |
| P13.2       | PWM0_M_9               | PWM0_44_N   | TC0_M_9_TR0  | TC0_44_TR1   | EXT_MUX[2]_2  | SCB3_RTS (0)  | SCB3_SCL (0) |               | LIN3_EN  | SCB3_CLK (0)  |         |         |         | AUDIOSS1_TX_WS      |             |         |
| P13.3       | PWM0_45                | PWM0_M_9_N  | TC0_45_TR0   | TC0_M_9_TR1  | EXT_MUX[2]_EN | SCB3_CTS (0)  |              |               | LIN2_RX  | SCB3_SEL0 (0) |         |         |         | AUDIOSS1_TX_SDO     |             |         |
| P13.4       | PWM0_M_10              | PWM0_45_N   | TC0_M_10_TR0 | TC0_45_TR1   | PWM0_H_4      |               |              |               | LIN2_TX  | SCB3_SEL1 (0) | LIN8_RX |         |         | AUDIOSS1_CLK_I2S_IF |             |         |
| P13.5       | PWM0_46                | PWM0_M_10_N | TC0_46_TR0   | TC0_M_10_TR1 | PWM0_H_4_N    |               |              |               |          | SCB3_SEL2 (0) | LIN8_TX |         |         | AUDIOSS1_RX_SCK     |             |         |
| P13.6       | PWM0_M_11              | PWM0_46_N   | TC0_M_11_TR0 | TC0_46_TR1   | PWM0_H_5      |               |              |               |          | SCB3_SEL3 (0) | LIN8_EN |         |         | AUDIOSS1_RX_WS      | TRIG_IN[22] |         |
| P13.7       | PWM0_47                | PWM0_M_11_N | TC0_47_TR0   | TC0_M_11_TR1 | PWM0_H_5_N    |               |              |               |          |               |         |         |         | AUDIOSS1_RX_SDI     | TRIG_IN[23] |         |
| P14.0       | PWM0_48                | PWM0_47_N   | TC0_48_TR0   | TC0_47_TR1   | PWM0_H_6      | SCB2_MISO (0) |              | SCB2_RX (0)   |          | CAN1_0_TX     |         |         |         | AUDIOSS2_MCLK       |             |         |
| P14.1       | PWM0_49                | PWM0_48_N   | TC0_49_TR0   | TC0_48_TR1   | PWM0_H_6_N    | SCB2_MOSI (0) | SCB2_SDA (0) | SCB2_TX (0)   |          | CAN1_0_RX     |         |         |         | AUDIOSS2_TX_SCK     |             |         |
| P14.2       | PWM0_50                | PWM0_49_N   | TC0_50_TR0   | TC0_49_TR1   | PWM0_H_7      | SCB2_CLK (0)  | SCB2_SCL (0) | SCB2_RTS (0)  | LIN6_RX  |               |         |         |         |                     |             |         |
| P14.3       | PWM0_51                | PWM0_50_N   | TC0_51_TR0   | TC0_50_TR1   | PWM0_H_7_N    | SCB2_SEL0 (0) |              | SCB2_CTS (0)  | LIN6_TX  |               |         |         |         |                     |             |         |
| P14.4       | PWM0_52                | PWM0_51_N   | TC0_52_TR0   | TC0_51_TR1   | TC0_H_4_TR0   | SCB2_SEL1 (0) |              |               | LIN6_EN  |               |         |         |         | AUDIOSS2_TX_WS      |             |         |
| P14.5       | PWM0_53                | PWM0_52_N   | TC0_53_TR0   | TC0_52_TR1   | TC0_H_4_TR1   | SCB2_SEL2 (0) | LIN14_RX     |               |          |               |         |         |         | AUDIOSS2_TX_SDO     |             |         |
| P14.6       | PWM0_54                | PWM0_53_N   | TC0_54_TR0   | TC0_53_TR1   | TC0_H_5_TR0   |               | LIN14_TX     |               |          |               |         |         |         |                     | TRIG_IN[24] |         |
| P14.7       | PWM0_55                | PWM0_54_N   | TC0_55_TR0   | TC0_54_TR1   | TC0_H_5_TR1   |               | LIN14_EN     |               |          |               |         |         |         |                     | TRIG_IN[25] |         |
| P15.0       | PWM0_56                | PWM0_55_N   | TC0_56_TR0   | TC0_55_TR1   | TC0_H_6_TR0   | SCB9_RX (0)   |              | SCB9_MISO (0) |          | CAN1_3_TX     |         |         |         | AUDIOSS2_CLK_I2S_IF |             |         |
| P15.1       | PWM0_57                | PWM0_56_N   | TC0_57_TR0   | TC0_56_TR1   | TC0_H_6_TR1   | SCB9_TX (0)   | SCB9_SDA (0) | SCB9_MOSI (0) |          | CAN1_3_RX     |         |         |         | AUDIOSS2_RX_SCK     |             |         |
| P15.2       | PWM0_58                | PWM0_57_N   | TC0_58_TR0   | TC0_57_TR1   | TC0_H_7_TR0   | SCB9_RTS (0)  | SCB9_SCL (0) | SCB9_CLK (0)  |          |               |         |         |         | AUDIOSS2_RX_WS      |             |         |
| P15.3       | PWM0_59                | PWM0_58_N   | TC0_59_TR0   | TC0_58_TR1   | TC0_H_7_TR1   | SCB9_CTS (0)  |              | SCB9_SEL0 (0) |          |               |         |         |         | AUDIOSS2_RX_SDI     |             |         |
| P16.0       | PWM0_60                | PWM0_59_N   | TC0_60_TR0   | TC0_59_TR1   | PWM0_H_0      |               |              | SCB9_SEL1 (0) | LIN11_RX |               |         |         |         |                     |             |         |
| P16.1       | PWM0_61                | PWM0_60_N   | TC0_61_TR0   | TC0_60_TR1   | PWM0_H_0_N    |               |              | SCB9_SEL2 (0) | LIN11_TX |               |         |         |         |                     |             |         |
| P16.2       | PWM0_62                | PWM0_61_N   | TC0_62_TR0   | TC0_61_TR1   | PWM0_H_1      |               |              | SCB9_SEL3 (0) | LIN11_EN |               |         |         |         |                     |             |         |
| P16.3       | PWM0_62                | PWM0_62_N   | TC0_62_TR0   | TC0_62_TR1   | PWM0_H_1_N    |               |              |               |          |               |         |         |         |                     |             |         |
| P16.4       |                        |             |              |              |               |               |              |               |          |               |         |         |         |                     |             |         |
| P16.5       |                        |             |              |              |               |               |              |               |          |               |         |         |         |                     |             |         |
| P16.6       |                        |             |              |              |               |               |              |               |          |               |         |         |         |                     |             |         |
| P16.7       |                        |             |              |              |               |               |              |               |          |               |         |         |         |                     |             |         |

Alternate function pin assignments

**Table 13-1** Alternate pin functions in active mode (continued)<sup>[23, 31, 32]</sup>

| Port<br>pin | Active mapping         |            |             |             |             |               |              |               |          |               |         |         |                  |         |             |                   |
|-------------|------------------------|------------|-------------|-------------|-------------|---------------|--------------|---------------|----------|---------------|---------|---------|------------------|---------|-------------|-------------------|
|             | HCon#8 <sup>[29]</sup> | HCon#9     | HCon#10     | HCon#11     | HCon#16     | HCon#17       | HCon#18      | HCon#19       | HCon#20  | HCon#21       | HCon#22 | HCon#23 | HCon#24          | HCon#25 | HCon#26     | HCon#27           |
|             | ACT #0 <sup>[30]</sup> | ACT #1     | ACT #2      | ACT #3      | ACT #4      | ACT #5        | ACT #6       | ACT #7        | ACT #8   | ACT #9        | ACT #10 | ACT #11 | ACT #12          | ACT #13 | ACT #14     | ACT #15           |
| P17.0       | PWM0_61                | PWM0_62_N  | TC0_61_TR0  | TC0_62_TR1  |             |               |              |               | LIN11_RX | CAN1_1_TX     |         |         |                  |         |             |                   |
| P17.1       | PWM0_60                | PWM0_61_N  | TC0_60_TR0  | TC0_61_TR1  |             | SCB3_RX (1)   |              |               | LIN11_TX | CAN1_1_RX     |         |         |                  |         |             |                   |
| P17.2       | PWM0_59                | PWM0_60_N  | TC0_59_TR0  | TC0_60_TR1  |             | SCB3_TX (1)   | SCB3_SDA (1) |               | LIN11_EN |               |         |         |                  |         |             |                   |
| P17.3       | PWM0_58                | PWM0_59_N  | TC0_58_TR0  | TC0_59_TR1  | PWM0_H_3    | SCB3_RTS (1)  | SCB3_SCL (1) |               |          | SCB3_CLK (1)  |         |         |                  |         | TRIG_IN[26] |                   |
| P17.4       | PWM0_57                | PWM0_58_N  | TC0_57_TR0  | TC0_58_TR1  | PWM0_H_3_N  | SCB3_CTS (1)  |              |               |          | SCB3_SEL0 (1) |         |         |                  |         | TRIG_IN[27] |                   |
| P17.5       | PWM0_56                | PWM0_57_N  | TC0_56_TR0  | TC0_57_TR1  | PWM0_H_2    |               | LIN15_RX     |               |          | SCB3_SEL1 (1) |         |         |                  |         |             |                   |
| P17.6       | PWM0_M_4               | PWM0_56_N  | TC0_M_4_TR0 | TC0_56_TR1  | PWM0_H_2_N  |               | LIN15_TX     |               |          | SCB3_SEL2 (1) |         |         |                  |         |             |                   |
| P17.7       | PWM0_M_5               | PWM0_M_4_N | TC0_M_5_TR0 | TC0_M_4_TR1 |             |               | LIN15_EN     |               |          | LIN12_RX      |         |         |                  |         |             |                   |
| P18.0       | PWM0_M_6               | PWM0_M_5_N | TC0_M_6_TR0 | TC0_M_5_TR1 | PWM0_H_0    | SCB1_RX (0)   |              | SCB1_MISO (0) |          | LIN12_TX      |         |         | ETH0_REF_CLK (0) |         |             | FAULT_OUT_0       |
| P18.1       | PWM0_M_7               | PWM0_M_6_N | TC0_M_7_TR0 | TC0_M_6_TR1 | PWM0_H_0_N  | SCB1_TX (0)   | SCB1_SDA (0) | SCB1_MOSI (0) |          | SCB3_MISO (1) |         |         | ETH0_TX_CTL (0)  |         |             | FAULT_OUT_1       |
| P18.2       | PWM0_55                | PWM0_M_7_N | TC0_55_TR0  | TC0_M_7_TR1 | PWM0_H_1    | SCB1_RTS (0)  | SCB1_SCL (0) | SCB1_CLK (0)  |          | SCB3_MOSI (1) |         |         | ETH0_TX_ER (0)   |         |             |                   |
| P18.3       | PWM0_54                | PWM0_55_N  | TC0_54_TR0  | TC0_55_TR1  | PWM0_H_1_N  | SCB1_CTS (0)  |              | SCB1_SEL0 (0) |          | SCB3_CLK (2)  |         |         | ETH0_TX_CLK (0)  |         |             | TRACE_CLOCK (0)   |
| P18.4       | PWM0_53                | PWM0_54_N  | TC0_53_TR0  | TC0_54_TR1  | PWM0_H_2    |               |              | SCB1_SEL1 (0) |          | SCB3_SEL0 (2) |         |         | ETH0_TXD_0 (0)   |         |             | TRACE_-DATA_0 (0) |
| P18.5       | PWM0_52                | PWM0_53_N  | TC0_52_TR0  | TC0_53_TR1  | PWM0_H_2_N  |               |              | SCB1_SEL2 (0) |          |               |         |         | ETH0_TXD_1 (0)   |         |             | TRACE_-DATA_1 (0) |
| P18.6       | PWM0_51                | PWM0_52_N  | TC0_51_TR0  | TC0_52_TR1  | PWM0_H_3    |               |              | SCB1_SEL3 (0) |          | CAN1_2_TX     |         |         | ETH0_TXD_2 (0)   |         |             | TRACE_-DATA_2 (0) |
| P18.7       | PWM0_50                | PWM0_51_N  | TC0_50_TR0  | TC0_51_TR1  | PWM0_H_3_N  |               |              |               |          | CAN1_2_RX     |         |         | ETH0_TXD_3 (0)   |         |             | TRACE_-DATA_3 (0) |
| P19.0       | PWM0_M_3               | PWM0_50_N  | TC0_M_3_TR0 | TC0_50_TR1  | TC0_H_0_TR0 | SCB2_MISO (1) |              | SCB2_RX (1)   |          | CAN1_3_TX     |         |         | ETH0_RXD_0 (0)   |         |             | FAULT_OUT_2       |
| P19.1       | PWM0_26                | PWM0_M_3_N | TC0_26_TR0  | TC0_M_3_TR1 | TC0_H_0_TR1 | SCB2_MOSI (1) | SCB2_SDA (1) | SCB2_TX (1)   |          | CAN1_3_RX     |         |         | ETH0_RXD_1 (0)   |         |             | FAULT_OUT_3       |
| P19.2       | PWM0_27                | PWM0_26_N  | TC0_27_TR0  | TC0_26_TR1  | TC0_H_1_TR0 | SCB2_CLK (1)  | SCB2_SCL (1) | SCB2_RTS (1)  |          |               |         |         | ETH0_RXD_2 (0)   |         | TRIG_IN[28] |                   |
| P19.3       | PWM0_28                | PWM0_27_N  | TC0_28_TR0  | TC0_27_TR1  | TC0_H_1_TR1 | SCB2_SEL0 (1) |              | SCB2_CTS (1)  |          |               |         |         | ETH0_RXD_3 (0)   |         | TRIG_IN[29] |                   |
| P19.4       | PWM0_29                | PWM0_28_N  | TC0_29_TR0  | TC0_28_TR1  | TC0_H_2_TR0 | SCB2_SEL1 (1) |              |               |          |               |         |         |                  |         |             |                   |
| P20.0       | PWM0_30                | PWM0_29_N  | TC0_30_TR0  | TC0_29_TR1  | TC0_H_2_TR1 | SCB2_SEL2 (1) |              |               | LIN5_RX  |               |         |         |                  |         |             |                   |
| P20.1       | PWM0_49                | PWM0_30_N  | TC0_49_TR0  | TC0_30_TR1  | TC0_H_3_TR0 |               |              |               | LIN5_TX  |               |         |         |                  |         |             |                   |
| P20.2       | PWM0_48                | PWM0_49_N  | TC0_48_TR0  | TC0_49_TR1  | TC0_H_3_TR1 |               |              |               | LIN5_EN  |               |         |         |                  |         |             |                   |
| P20.3       | PWM0_47                | PWM0_48_N  | TC0_47_TR0  | TC0_48_TR1  |             | SCB1_RX (1)   |              | SCB1_MISO (1) |          | CAN1_2_TX     |         |         |                  |         |             |                   |
| P20.4       | PWM0_46                | PWM0_47_N  | TC0_46_TR0  | TC0_47_TR1  |             | SCB1_TX (1)   | SCB1_SDA (1) | SCB1_MOSI (1) |          | CAN1_2_RX     |         |         |                  |         |             |                   |
| P20.5       | PWM0_45                | PWM0_46_N  | TC0_45_TR0  | TC0_46_TR1  |             | SCB1_RTS (1)  | SCB1_SCL (1) | SCB1_CLK (1)  |          |               |         |         |                  |         |             |                   |
| P20.6       | PWM0_44                | PWM0_45_N  | TC0_44_TR0  | TC0_45_TR1  |             | SCB1_CTS (1)  |              | SCB1_SEL0 (1) |          |               |         |         |                  |         |             |                   |
| P20.7       | PWM0_43                | PWM0_44_N  | TC0_43_TR0  | TC0_44_TR1  |             |               |              | SCB1_SEL1 (1) |          |               |         |         |                  |         |             |                   |

**Table 13-1** Alternate pin functions in active mode *(continued)*<sup>[23, 31, 32]</sup>

| Port<br>pin | Active mapping         |             |              |              |         |               |              |               |         |           |         |                    |                 |                                        |             |                       |
|-------------|------------------------|-------------|--------------|--------------|---------|---------------|--------------|---------------|---------|-----------|---------|--------------------|-----------------|----------------------------------------|-------------|-----------------------|
|             | HCon#8 <sup>[29]</sup> | HCon#9      | HCon#10      | HCon#11      | HCon#16 | HCon#17       | HCon#18      | HCon#19       | HCon#20 | HCon#21   | HCon#22 | HCon#23            | HCon#24         | HCon#25                                | HCon#26     | HCon#27               |
|             | ACT #0 <sup>[30]</sup> | ACT #1      | ACT #2       | ACT #3       | ACT #4  | ACT #5        | ACT #6       | ACT #7        | ACT #8  | ACT #9    | ACT #10 | ACT #11            | ACT #12         | ACT #13                                | ACT #14     | ACT #15               |
| P21.0       | PWM0_42                | PWM0_43_N   | TC0_42_TR0   | TC0_43_TR1   |         |               |              | SCB1_SEL2 (1) |         |           |         |                    |                 |                                        |             |                       |
| P21.1       | PWM0_41                | PWM0_42_N   | TC0_41_TR0   | TC0_42_TR1   |         |               |              |               |         |           |         |                    |                 |                                        |             |                       |
| P21.2       | PWM0_40                | PWM0_41_N   | TC0_40_TR0   | TC0_41_TR1   |         |               |              |               |         |           | EXT_CLK |                    |                 |                                        |             | TRIG_DBG[1]           |
| P21.3       | PWM0_39                | PWM0_40_N   | TC0_39_TR0   | TC0_40_TR1   |         |               |              |               |         |           |         |                    |                 |                                        |             |                       |
| P21.4       | PWM0_38                | PWM0_39_N   | TC0_38_TR0   | TC0_39_TR1   |         |               |              |               |         |           |         |                    |                 |                                        |             |                       |
| P21.5       | PWM0_37                | PWM0_38_N   | TC0_37_TR0   | TC0_38_TR1   |         |               |              |               | LIN0_RX | CAN1_1_TX | PWM0_34 | PWM0_35_N          | ETH0_RX_CTL (0) |                                        |             | TRACE_-<br>DATA_0 (1) |
| P21.6       | PWM0_36                | PWM0_37_N   | TC0_36_TR0   | TC0_37_TR1   |         |               |              |               | LIN0_TX | LIN13_RX  |         |                    |                 |                                        |             |                       |
| P21.7       | PWM0_35                | PWM0_36_N   | TC0_35_TR0   | TC0_36_TR1   |         | SCB6_RX (1)   |              | SCB6_MISO (1) | LIN0_EN | LIN13_TX  |         |                    |                 |                                        |             | CAL_SUP_NZ            |
| P22.1       | PWM0_33                | PWM0_34_N   | TC0_33_TR0   | TC0_34_TR1   |         | SCB6_TX (1)   | SCB6_SDA (1) | SCB6_MOSI (1) |         | CAN1_1_RX |         |                    |                 |                                        |             | TRACE_-<br>DATA_1 (1) |
| P22.2       | PWM0_32                | PWM0_33_N   | TC0_32_TR0   | TC0_33_TR1   |         | SCB6_RTS (1)  | SCB6_SCL (1) | SCB6_CLK (1)  |         |           |         |                    |                 |                                        |             | TRACE_-<br>DATA_2 (1) |
| P22.3       | PWM0_31                | PWM0_32_N   | TC0_31_TR0   | TC0_32_TR1   |         | SCB6_CTS (1)  |              | SCB6_SEL0 (1) |         |           |         |                    |                 |                                        |             | TRACE_-<br>DATA_3 (1) |
| P22.4       | PWM0_30                | PWM0_31_N   | TC0_30_TR0   | TC0_31_TR1   |         |               |              | SCB6_SEL1 (1) |         |           |         |                    |                 |                                        |             | TRACE_CLOCK<br>(1)    |
| P22.5       | PWM0_29                | PWM0_30_N   | TC0_29_TR0   | TC0_30_TR1   |         |               |              | SCB6_SEL2 (1) | LIN7_RX |           |         |                    |                 |                                        |             |                       |
| P22.6       | PWM0_28                | PWM0_29_N   | TC0_28_TR0   | TC0_29_TR1   |         |               |              |               | LIN7_TX |           |         |                    |                 |                                        |             |                       |
| P22.7       | PWM0_27                | PWM0_28_N   | TC0_27_TR0   | TC0_28_TR1   |         |               | LIN14_RX     |               | LIN7_EN |           |         |                    |                 |                                        |             |                       |
| P23.0       | PWM0_M_8               | PWM0_27_N   | TC0_M_8_TR0  | TC0_27_TR1   |         | SCB7_RX (1)   | LIN14_TX     | SCB7_MISO (1) |         | CAN1_0_TX |         |                    |                 |                                        |             | FAULT_OUT_0           |
| P23.1       | PWM0_M_9               | PWM0_M_8_N  | TC0_M_9_TR0  | TC0_M_8_TR1  |         | SCB7_TX (1)   | SCB7_SDA (1) | SCB7_MOSI (1) |         | CAN1_0_RX |         |                    |                 |                                        |             | FAULT_OUT_1           |
| P23.2       | PWM0_M_10              | PWM0_M_9_N  | TC0_M_10_TR0 | TC0_M_9_TR1  |         | SCB7_RTS (1)  | SCB7_SCL (1) | SCB7_CLK (1)  | LIN6_RX |           |         |                    |                 |                                        |             | FAULT_OUT_2           |
| P23.3       | PWM0_M_11              | PWM0_M_10_N | TC0_M_11_TR0 | TC0_M_10_TR1 |         | SCB7_CTS (1)  |              | SCB7_SEL0 (1) | LIN6_TX |           |         |                    | ETH0_RX_CLK (0) |                                        | TRIG_IN[30] | FAULT_OUT_3           |
| P23.4       | PWM0_25                | PWM0_M_11_N | TC0_25_TR0   | TC0_M_11_TR1 |         | SCB2_MISO (2) |              | SCB7_SEL1 (1) |         |           |         |                    |                 |                                        | TRIG_IN[31] | TRIG_DBG[0]           |
| P23.5       | PWM0_24                | PWM0_25_N   | TC0_24_TR0   | TC0_25_TR1   |         | SCB2_MOSI (2) |              | SCB7_SEL2 (1) |         |           |         | LIN9_RX            |                 |                                        |             |                       |
| P23.6       | PWM0_23                | PWM0_24_N   | TC0_23_TR0   | TC0_24_TR1   |         | SCB2_CLK (2)  |              |               |         |           |         | LIN9_TX            |                 |                                        |             |                       |
| P23.7       | PWM0_22                | PWM0_23_N   | TC0_22_TR0   | TC0_23_TR1   |         | SCB2_SEL0 (2) |              |               |         |           | EXT_CLK | LIN9_EN            |                 |                                        |             | CAL_SUP_NZ            |
| P24.0       |                        |             |              |              |         |               |              |               |         |           | EXT_CLK |                    |                 | SDHC_CARD_-<br>DETECT_N (1)            |             |                       |
| P24.1       |                        |             |              |              |         |               |              |               |         |           |         | SPIHB_CLK<br>(1)   |                 | SDHC_CARD_-<br>MECH_WRITE_P<br>ROT (1) |             |                       |
| P24.2       |                        |             |              |              |         |               |              |               |         |           |         | SPIHB_RWD<br>S (1) |                 | SDHC_-<br>CLK_CARD (1)                 |             |                       |
| P24.3       |                        |             |              |              |         |               |              |               |         |           |         | SPIHB_SEL0<br>(1)  |                 | SDHC_-<br>CARD_CMD (1)                 |             |                       |
| P24.4       |                        |             |              |              |         |               |              |               |         |           |         | SPIHB_SEL1<br>(1)  |                 | SDHC_-<br>CARD_IF_P-<br>WR_EN (1)      |             |                       |

**Table 13-1** Alternate pin functions in active mode *(continued)*<sup>[23, 31, 32]</sup>

| Port<br>pin | Active mapping         |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
|-------------|------------------------|--------|---------|---------|---------|---------------|---------------|----------------|---------|---------|---------|----------------------|---------|-------------------------------|---------|---------|
|             | HCon#8 <sup>[29]</sup> | HCon#9 | HCon#10 | HCon#11 | HCon#16 | HCon#17       | HCon#18       | HCon#19        | HCon#20 | HCon#21 | HCon#22 | HCon#23              | HCon#24 | HCon#25                       | HCon#26 | HCon#27 |
|             | ACT #0 <sup>[30]</sup> | ACT #1 | ACT #2  | ACT #3  | ACT #4  | ACT #5        | ACT #6        | ACT #7         | ACT #8  | ACT #9  | ACT #10 | ACT #11              | ACT #12 | ACT #13                       | ACT #14 | ACT #15 |
| P25.0       |                        |        |         |         |         |               |               |                |         |         |         | SPIHB -<br>DATA0 (1) |         | SDHC_CARD -<br>DAT_3TO0_0 (1) |         |         |
| P25.1       |                        |        |         |         |         |               |               |                |         |         |         | SPIHB -<br>DATA1 (1) |         | SDHC_CARD -<br>DAT_3TO0_1 (1) |         |         |
| P25.2       |                        |        |         |         |         |               |               |                |         |         |         | SPIHB -<br>DATA2 (1) |         | SDHC_CARD -<br>DAT_3TO0_2 (1) |         |         |
| P25.3       |                        |        |         |         |         |               |               |                |         |         |         | SPIHB -<br>DATA3 (1) |         | SDHC_CARD -<br>DAT_3TO0_3 (1) |         |         |
| P25.4       |                        |        |         |         |         |               |               |                |         |         |         | SPIHB -<br>DATA4 (1) |         | SDHC_CARD -<br>DAT_7TO4_0 (1) |         |         |
| P25.5       |                        |        |         |         |         |               |               |                |         |         |         | SPIHB -<br>DATA5 (1) |         | SDHC_CARD -<br>DAT_7TO4_1 (1) |         |         |
| P25.6       |                        |        |         |         |         |               |               |                |         |         |         | SPIHB -<br>DATA6 (1) |         | SDHC_CARD -<br>DAT_7TO4_2 (1) |         |         |
| P25.7       |                        |        |         |         |         |               |               |                |         |         |         | SPIHB -<br>DATA7 (1) |         | SDHC_CARD -<br>DAT_7TO4_3 (1) |         |         |
| P26.0       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P26.1       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P26.2       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P26.3       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P26.4       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P26.5       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P26.6       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P26.7       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P27.0       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P27.1       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P27.2       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P27.3       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P27.4       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P27.5       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P27.6       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P27.7       |                        |        |         |         |         |               |               |                |         |         |         |                      |         |                               |         |         |
| P28.0       |                        |        |         |         |         | SCB10_RX (0)  |               | SCB10_MISO (0) |         |         |         |                      |         |                               |         |         |
| P28.1       |                        |        |         |         |         | SCB10_TX (0)  | SCB10_SDA (0) | SCB10_MOSI (0) |         |         |         |                      |         |                               |         |         |
| P28.2       |                        |        |         |         |         | SCB10_RTS (0) | SCB10_SCL (0) | SCB10_CLK (0)  |         |         |         |                      |         |                               |         |         |
| P28.3       |                        |        |         |         |         | SCB10_CTS (0) |               | SCB10_SEL0 (0) |         |         |         |                      |         |                               |         |         |
| P28.4       |                        |        |         |         |         |               |               | SCB10_SEL1 (0) |         |         |         |                      |         |                               |         |         |

**Table 13-1** Alternate pin functions in active mode *(continued)*<sup>[23, 31, 32]</sup>

| Port<br>pin | Active mapping         |        |         |         |         |               |               |                |         |           |         |         |         |         |         |         |
|-------------|------------------------|--------|---------|---------|---------|---------------|---------------|----------------|---------|-----------|---------|---------|---------|---------|---------|---------|
|             | HCon#8 <sup>[29]</sup> | HCon#9 | HCon#10 | HCon#11 | HCon#16 | HCon#17       | HCon#18       | HCon#19        | HCon#20 | HCon#21   | HCon#22 | HCon#23 | HCon#24 | HCon#25 | HCon#26 | HCon#27 |
|             | ACT #0 <sup>[30]</sup> | ACT #1 | ACT #2  | ACT #3  | ACT #4  | ACT #5        | ACT #6        | ACT #7         | ACT #8  | ACT #9    | ACT #10 | ACT #11 | ACT #12 | ACT #13 | ACT #14 | ACT #15 |
| P28.5       |                        |        |         |         |         |               |               | SCB10_SEL2 (0) |         |           |         |         |         |         |         |         |
| P28.6       |                        |        |         |         |         |               |               | SCB10_SEL3 (0) |         |           |         |         |         |         |         |         |
| P28.7       |                        |        |         |         |         |               |               |                |         |           |         |         |         |         |         |         |
| P29.0       |                        |        |         |         |         |               |               |                |         |           |         |         |         |         |         |         |
| P29.1       |                        |        |         |         |         |               |               |                |         |           |         |         |         |         |         |         |
| P29.2       |                        |        |         |         |         |               |               |                |         |           |         |         |         |         |         |         |
| P29.3       |                        |        |         |         |         |               |               |                |         |           |         |         |         |         |         |         |
| P29.4       |                        |        |         |         |         |               |               |                |         |           |         |         |         |         |         |         |
| P29.5       |                        |        |         |         |         |               |               |                |         |           |         |         |         |         |         |         |
| P29.6       |                        |        |         |         |         |               |               |                |         |           |         |         |         |         |         |         |
| P29.7       |                        |        |         |         |         |               |               |                |         |           |         |         |         |         |         |         |
| P30.0       |                        |        |         |         |         | SCB9_RTS (1)  |               | SCB9_CLK (1)   |         |           |         |         |         |         |         |         |
| P30.1       |                        |        |         |         |         | SCB9_CTS (1)  |               | SCB9_SEL0 (1)  |         |           |         |         |         |         |         |         |
| P30.2       |                        |        |         |         |         |               |               | SCB9_SEL1 (1)  |         | CAN1_3_TX |         |         |         |         |         |         |
| P30.3       |                        |        |         |         |         |               |               | SCB9_SEL2 (1)  |         | CAN1_3_RX |         |         |         |         |         |         |
| P31.0       |                        |        |         |         |         |               |               |                |         |           |         |         |         |         |         |         |
| P31.1       |                        |        |         |         |         |               |               |                |         |           |         |         |         |         |         |         |
| P31.2       |                        |        |         |         |         |               |               |                |         |           |         |         |         |         |         |         |
| P32.0       |                        |        |         |         |         | SCB10_RX (1)  |               | SCB10_MISO (1) |         |           |         |         |         |         |         |         |
| P32.1       |                        |        |         |         |         | SCB10_TX (1)  | SCB10_SDA (1) | SCB10_MOSI (1) |         |           |         |         |         |         |         |         |
| P32.2       |                        |        |         |         |         | SCB10_RTS (1) | SCB10_SCL (1) | SCB10_CLK (1)  |         |           |         |         |         |         |         |         |
| P32.3       |                        |        |         |         |         | SCB10_CTS (1) |               | SCB10_SEL0 (1) |         |           |         |         |         |         |         |         |
| P32.4       |                        |        |         |         |         |               | LIN10_RX      | SCB10_SEL1 (1) |         |           |         |         |         |         |         |         |
| P32.5       |                        |        |         |         |         |               | LIN10_TX      | SCB10_SEL2 (1) |         |           |         |         |         |         |         |         |
| P32.6       |                        |        |         |         |         |               | LIN10_EN      | SCB10_SEL3 (1) |         |           |         |         |         |         |         |         |
| P32.7       |                        |        |         |         |         |               |               |                |         |           |         |         |         |         |         |         |

## 13.1 Pin function description

**Table 13-2 Pin function description**

| Sl. No. | Pin                         | Module   | Description                                                                                                         |
|---------|-----------------------------|----------|---------------------------------------------------------------------------------------------------------------------|
| 1       | PWMx_y                      | TCPWM    | TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number                    |
| 2       | PWMx_y_N                    | TCPWM    | TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number  |
| 3       | PWMx_M_y                    | TCPWM    | TCPWM 16-bit PWM with motor control line out, x-TCPWM block, y-counter number                                       |
| 4       | PWMx_M_y_N                  | TCPWM    | TCPWM 16-bit PWM with motor control complementary line out (N), x-TCPWM block, y-counter number                     |
| 5       | PWMx_H_y                    | TCPWM    | TCPWM 32-bit PWM, PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number                                       |
| 6       | PWMx_H_y_N                  | TCPWM    | TCPWM 32-bit PWM, PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number                     |
| 7       | TCx_y_TRz                   | TCPWM    | TCPWM 16-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number                    |
| 8       | TCx_M_y_TRz                 | TCPWM    | TCPWM 16-bit dedicated counter input triggers with motor control, x-TCPWM block, y-counter number, z-trigger number |
| 9       | TCx_H_y_TRz                 | TCPWM    | TCPWM 32-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number                    |
| 10      | SCBx_RX                     | SCB      | UART Receive, x-SCB block                                                                                           |
| 11      | SCBx_TX                     | SCB      | UART Transmit, x-SCB block                                                                                          |
| 12      | SCBx_RTS                    | SCB      | UART Request to Send (Handshake), x-SCB block                                                                       |
| 13      | SCBx_CTS                    | SCB      | UART Clear to Send (Handshake), x-SCB block                                                                         |
| 14      | SCBx_SDA                    | SCB      | I <sup>2</sup> C Data line, x-SCB block                                                                             |
| 15      | SCBx_SCL                    | SCB      | I <sup>2</sup> C Clock line, x-SCB block                                                                            |
| 16      | SCBx_MISO                   | SCB      | SPI Master Input Slave Output, x-SCB block                                                                          |
| 17      | SCBx_MOSI                   | SCB      | SPI Master Output Slave Input, x-SCB block                                                                          |
| 18      | SCBx_CLK                    | SCB      | SPI Serial Clock, x-SCB block                                                                                       |
| 19      | SCBx_SELy                   | SCB      | SPI Slave Select, x-SCB block, y-select line                                                                        |
| 20      | LINx_RX                     | LIN      | LIN Receive line, x-LIN block                                                                                       |
| 21      | LINx_TX                     | LIN      | LIN Transmit line, x-LIN block                                                                                      |
| 22      | LINx_EN                     | LIN      | LIN Enable line, x-LIN block                                                                                        |
| 23      | CANx_y_TX                   | CANFD    | CAN Transmit line, x-CAN block, y-channel number                                                                    |
| 24      | CANx_y_RX                   | CANFD    | CAN Receive line, x-CAN block, y-channel number                                                                     |
| 25      | SPIHB_CLK                   | SMIF     | SMIF interface clock                                                                                                |
| 26      | SPIHB_RWDS                  | SMIF     | SMIF (SPI/HYPERBUS™) read-write-data-strobe line                                                                    |
| 27      | SPIHB_SELx                  | SMIF     | SMIF (SPI/HYPERBUS™) memory select line, x-select line number                                                       |
| 28      | SPIHB_DATAx                 | SMIF     | SMIF (SPI/HYPERBUS™) memory data read and write line, x-0 to 7 data lines                                           |
| 29      | ETHx_RX_ER                  | Ethernet | Ethernet receive error indication line, x-ETH module number                                                         |
| 30      | ETHx_ETH_TSU_TIMER_C-MP_VAL | Ethernet | Ethernet time stamp unit timer compare indication line, x-ETH module number                                         |
| 31      | ETHx_MDIO                   | Ethernet | Ethernet management data input/output (MDIO) interface to PHY, x-ETH module number                                  |
| 32      | ETHx_MDC                    | Ethernet | Ethernet management data clock (MDC) line, x-ETH module number                                                      |
| 33      | ETHx_REF_CLK                | Ethernet | Ethernet reference clock line, x-ETH module number                                                                  |
| 34      | ETHx_TX_CTL                 | Ethernet | Ethernet transmit control line, x-ETH module number                                                                 |
| 35      | ETHx_TX_ER                  | Ethernet | Ethernet transmit error indication line, x-ETH module number                                                        |
| 36      | ETHx_TX_CLK                 | Ethernet | Ethernet transmit clock line, x-ETH module number                                                                   |
| 37      | ETHx_TXD_y                  | Ethernet | Ethernet transmit data line, , x-ETH module number, y-transmit channel number                                       |
| 38      | ETHx_RXD_y                  | Ethernet | Ethernet receive data line, , x-ETH module number, y-receive channel number                                         |
| 39      | ETHx_RX_CTL                 | Ethernet | Ethernet receive control line, x-ETH module number                                                                  |
| 40      | ETHx_RX_CLK                 | Ethernet | Ethernet receive clock line, x-ETH module number                                                                    |

## Alternate function pin assignments

**Table 13-2 Pin function description** *(continued)*

| Sl. No. | Pin                      | Module     | Description                                                                                                               |
|---------|--------------------------|------------|---------------------------------------------------------------------------------------------------------------------------|
| 41      | SDHC_CARD_MEC_WRITE_PROT | SDHC       | SDHC mechanical write protect                                                                                             |
| 42      | SDHC_CARD_CMD            | SDHC       | SDHC command line                                                                                                         |
| 43      | SDHC_CLK_CARD            | SDHC       | SDHC clock line                                                                                                           |
| 44      | SDHC_CARD_DETECT_N       | SDHC       | SDHC interface insertion or removal detection line                                                                        |
| 45      | SDHC_CARD_IF_PWR_EN      | SDHC       | SDHC interface power cycle line                                                                                           |
| 46      | SDHC_CARD_DAT_3TO0_x     | SDHC       | SDHC lower 4-bits of the data                                                                                             |
| 47      | SDHC_CARD_DAT_7TO4_x     | SDHC       | SDHC upper 4-bits of the data in 8-bit mode                                                                               |
| 48      | AUDIOSSx_MCLK            | AUDIOSS    | AudioSS master clock out, x-AudioSS block                                                                                 |
| 49      | AUDIOSSx_TX_SCK          | AUDIOSS    | I <sup>2</sup> S serial clock for transmitter, x-AudioSS block                                                            |
| 50      | AUDIOSSx_TX_WS           | AUDIOSS    | I <sup>2</sup> S word select for transmitter, x-AudioSS block                                                             |
| 51      | AUDIOSSx_TX_SDO          | AUDIOSS    | I <sup>2</sup> S serial data output for transmitter, x-AudioSS block                                                      |
| 52      | AUDIOSSx_CLK_I2S_IF      | AUDIOSS    | I <sup>2</sup> S clock supplied from external I2S bus host, x-AudioSS block                                               |
| 53      | AUDIOSSx_RX_SCK          | AUDIOSS    | I <sup>2</sup> S serial clock for receiver, x-AudioSS block                                                               |
| 54      | AUDIOSSx_RX_WS           | AUDIOSS    | I <sup>2</sup> S word select for receiver, x-AudioSS block                                                                |
| 55      | AUDIOSSx_RX_SDI          | AUDIOSS    | I <sup>2</sup> S serial data input for receiver, x-AudioSS block                                                          |
| 56      | CAL_SUP_NZ               | System     | ETAS Calibration support line                                                                                             |
| 57      | FAULT_OUT_x              | SRSS       | Fault output line x-0 to 3                                                                                                |
| 58      | TRACE_DATA_x             | SRSS       | Trace data out line x-0 to 3                                                                                              |
| 59      | TRACE_CLOCK              | SRSS       | Trace clock line                                                                                                          |
| 60      | RTC_CAL                  | SRSS RTC   | RTC calibration clock input                                                                                               |
| 61      | SWJ_TRSTN                | SRSS       | JTAG Test reset line (Active low)                                                                                         |
| 62      | SWJ_SWO_TDO              | SRSS       | JTAG Test data output/SWO (Serial Wire Output)                                                                            |
| 63      | SWJ_SWCLK_TCLK           | SRSS       | JTAG Test clock/SWD clock (Serial Wire Clock)                                                                             |
| 64      | SWJ_SWDIO_TMS            | SRSS       | JTAG Test mode select/SWD data (Serial Wire Data Input/Output)                                                            |
| 65      | SWJ_SWDOE_TDI            | SRSS       | JTAG Test data input                                                                                                      |
| 66      | HIBERNATE_WAKEUP[x]      | SRSS       | Hibernate wakeup line x-0 to 3                                                                                            |
| 67      | EXT_CLK                  | SRSS       | External clock input                                                                                                      |
| 68      | EXT_PS_CTL0              | SRSS REGHC | REGHC control line, Transistor mode/Positive terminal of the current sense resistor, PMIC mode/Power good input from PMIC |
| 69      | EXT_PS_CTL1              | SRSS REGHC | REGHC control line, Transistor mode/Negative terminal of the current sense resistor, PMIC mode/Enable output for PMIC     |
| 70      | EXT_PS_CTL2              | SRSS REGHC | REGHC control line, Transistor mode/unused, PMIC mode/Reset threshold adjustment for some PMICs                           |
| 71      | ADC[x]_y                 | PASS SAR   | SAR, channel, x-SAR number, y-channel number                                                                              |
| 72      | ADC[x]_M                 | PASS SAR   | SAR motor control input, x-SAR number                                                                                     |
| 73      | EXT_MUX[x]_y             | PASS SAR   | External SAR MUX inputs, x-MUX number, y-MUX input 0 to 2                                                                 |
| 74      | EXT_MUX[x]_EN            | PASS SAR   | External SAR MUX enable line                                                                                              |

## 14 Interrupts and wake-up assignments

**Table 14-1 Peripheral interrupt assignments and wake-up sources**

| Interrupt | Source                             | Power Mode | Description                                                             |
|-----------|------------------------------------|------------|-------------------------------------------------------------------------|
| 0         | cpuss_interrupts_ipc_0_IRQn        | DeepSleep  | CPUSS Inter Process Communication Interrupt #0                          |
| 1         | cpuss_interrupts_ipc_1_IRQn        | DeepSleep  | CPUSS Inter Process Communication Interrupt #1                          |
| 2         | cpuss_interrupts_ipc_2_IRQn        | DeepSleep  | CPUSS Inter Process Communication Interrupt #2                          |
| 3         | cpuss_interrupts_ipc_3_IRQn        | DeepSleep  | CPUSS Inter Process Communication Interrupt #3                          |
| 4         | cpuss_interrupts_ipc_4_IRQn        | DeepSleep  | CPUSS Inter Process Communication Interrupt #4                          |
| 5         | cpuss_interrupts_ipc_5_IRQn        | DeepSleep  | CPUSS Inter Process Communication Interrupt #5                          |
| 6         | cpuss_interrupts_ipc_6_IRQn        | DeepSleep  | CPUSS Inter Process Communication Interrupt #6                          |
| 7         | cpuss_interrupts_ipc_7_IRQn        | DeepSleep  | CPUSS Inter Process Communication Interrupt #7                          |
| 8         | cpuss_interrupts_fault_0_IRQn      | DeepSleep  | CPUSS Fault Structure #0 Interrupt                                      |
| 9         | cpuss_interrupts_fault_1_IRQn      | DeepSleep  | CPUSS Fault Structure #1 Interrupt                                      |
| 10        | cpuss_interrupts_fault_2_IRQn      | DeepSleep  | CPUSS Fault Structure #2 Interrupt                                      |
| 11        | cpuss_interrupts_fault_3_IRQn      | DeepSleep  | CPUSS Fault Structure #3 Interrupt                                      |
| 12        | srss_interrupt_backup_IRQn         | DeepSleep  | BACKUP domain Interrupt                                                 |
| 13        | srss_interrupt_mcwdt_0_IRQn        | DeepSleep  | Multi Counter Watchdog Timer #0 interrupt                               |
| 14        | srss_interrupt_mcwdt_1_IRQn        | DeepSleep  | Multi Counter Watchdog Timer #1 interrupt                               |
| 15        | srss_interrupt_mcwdt_2_IRQn        | DeepSleep  | Multi Counter Watchdog Timer #2 interrupt                               |
| 16        | srss_interrupt_wdt_IRQn            | DeepSleep  | Hardware Watchdog Timer interrupt                                       |
| 17        | srss_interrupt_IRQn                | DeepSleep  | Other combined Interrupts for SRSS (LVD, CLKCAL)                        |
| 18        | scb_0_interrupt_IRQn               | DeepSleep  | SCB0 interrupt (DeepSleep capable)                                      |
| 19        | evtgen_0_interrupt_dpslp_IRQn      | DeepSleep  | Event gen DeepSleep domain interrupt                                    |
| 20        | ioss_interrupt_vdd_IRQn            | DeepSleep  | I/O Supply ( $V_{DDIO}$ , $V_{DDA}$ , $V_{DD}$ ) state change Interrupt |
| 21        | ioss_interrupt_gpio_dpslp_IRQn     | DeepSleep  | Consolidated Interrupt for GPIO_STD and GPIO_ENH, All Ports             |
| 22        | ioss_interrupts_gpio_dpslp_0_IRQn  | DeepSleep  | GPIO_ENH Port #0 Interrupt                                              |
| 23        | ioss_interrupts_gpio_dpslp_1_IRQn  | DeepSleep  | GPIO_STD Port #1 Interrupt                                              |
| 24        | ioss_interrupts_gpio_dpslp_2_IRQn  | DeepSleep  | GPIO_STD Port #2 Interrupt                                              |
| 25        | ioss_interrupts_gpio_dpslp_3_IRQn  | DeepSleep  | GPIO_STD Port #3 Interrupt                                              |
| 26        | ioss_interrupts_gpio_dpslp_4_IRQn  | DeepSleep  | GPIO_STD Port #4 Interrupt                                              |
| 27        | ioss_interrupts_gpio_dpslp_5_IRQn  | DeepSleep  | GPIO_STD Port #5 Interrupt                                              |
| 28        | ioss_interrupts_gpio_dpslp_6_IRQn  | DeepSleep  | GPIO_STD Port #6 Interrupt                                              |
| 29        | ioss_interrupts_gpio_dpslp_7_IRQn  | DeepSleep  | GPIO_STD Port #7 Interrupt                                              |
| 30        | ioss_interrupts_gpio_dpslp_8_IRQn  | DeepSleep  | GPIO_STD Port #8 Interrupt                                              |
| 31        | ioss_interrupts_gpio_dpslp_9_IRQn  | DeepSleep  | GPIO_STD Port #9 Interrupt                                              |
| 32        | ioss_interrupts_gpio_dpslp_10_IRQn | DeepSleep  | GPIO_STD Port #10 Interrupt                                             |
| 33        | ioss_interrupts_gpio_dpslp_11_IRQn | DeepSleep  | GPIO_STD Port #11 Interrupt                                             |
| 34        | ioss_interrupts_gpio_dpslp_12_IRQn | DeepSleep  | GPIO_STD Port #12 Interrupt                                             |
| 35        | ioss_interrupts_gpio_dpslp_13_IRQn | DeepSleep  | GPIO_STD Port #13 Interrupt                                             |
| 36        | ioss_interrupts_gpio_dpslp_14_IRQn | DeepSleep  | GPIO_STD Port #14 Interrupt                                             |
| 37        | ioss_interrupts_gpio_dpslp_15_IRQn | DeepSleep  | GPIO_STD Port #15 Interrupt                                             |
| 38        | ioss_interrupts_gpio_dpslp_16_IRQn | DeepSleep  | GPIO_STD Port #16 Interrupt                                             |
| 39        | ioss_interrupts_gpio_dpslp_17_IRQn | DeepSleep  | GPIO_STD Port #17 Interrupt                                             |
| 40        | ioss_interrupts_gpio_dpslp_18_IRQn | DeepSleep  | GPIO_STD Port #18 Interrupt                                             |
| 41        | ioss_interrupts_gpio_dpslp_19_IRQn | DeepSleep  | GPIO_STD Port #19 Interrupt                                             |
| 42        | ioss_interrupts_gpio_dpslp_20_IRQn | DeepSleep  | GPIO_STD Port #20 Interrupt                                             |

## Interrupts and wake-up assignments

**Table 14-1 Peripheral interrupt assignments and wake-up sources (continued)**

| Interrupt | Source                             | Power Mode | Description                                           |
|-----------|------------------------------------|------------|-------------------------------------------------------|
| 43        | ioss_interrupts_gpio_dpslp_21_IRQn | DeepSleep  | GPIO_STD Port #21 Interrupt                           |
| 44        | ioss_interrupts_gpio_dpslp_22_IRQn | DeepSleep  | GPIO_STD Port #22 Interrupt                           |
| 45        | ioss_interrupts_gpio_dpslp_23_IRQn | DeepSleep  | GPIO_STD Port #23 Interrupt                           |
| 46        | ioss_interrupts_gpio_dpslp_28_IRQn | DeepSleep  | GPIO_STD Port #28 Interrupt                           |
| 47        | ioss_interrupts_gpio_dpslp_29_IRQn | DeepSleep  | GPIO_STD Port #29 Interrupt                           |
| 48        | ioss_interrupts_gpio_dpslp_30_IRQn | DeepSleep  | GPIO_STD Port #30 Interrupt                           |
| 49        | ioss_interrupts_gpio_dpslp_31_IRQn | DeepSleep  | GPIO_STD Port #31 Interrupt                           |
| 50        | ioss_interrupts_gpio_dpslp_32_IRQn | DeepSleep  | GPIO_STD Port #32 Interrupt                           |
| 51        | ioss_interrupts_gpio_act_IRQn      | Active     | Consolidated Interrupt for HSIO_STD, All Ports        |
| 52        | ioss_interrupts_gpio_act_24_IRQn   | Active     | HSIO_STD Port #24 Interrupt                           |
| 53        | ioss_interrupts_gpio_act_25_IRQn   | Active     | HSIO_STD Port #25 Interrupt                           |
| 54        | ioss_interrupts_gpio_act_26_IRQn   | Active     | HSIO_STD Port #26 Interrupt                           |
| 55        | ioss_interrupts_gpio_act_27_IRQn   | Active     | HSIO_STD Port #27 Interrupt                           |
| 56        | cpuss_interrupt_crypto_IRQn        | Active     | CRYPTO Accelerator Interrupt                          |
| 57        | cpuss_interrupt_fm_IRQn            | Active     | Flash Macro Interrupt                                 |
| 58        | cpuss_interrupts_cm7_0_fp_IRQn     | Active     | CM7_0 Floating Point operation fault                  |
| 59        | cpuss_interrupts_cm7_1_fp_IRQn     | Active     | CM7_1 Floating Point operation fault                  |
| 60        | cpuss_interrupts_cm0_cti_0_IRQn    | Active     | CM0+ CTI (Cross Trigger Interface) #0                 |
| 61        | cpuss_interrupts_cm0_cti_1_IRQn    | Active     | CM0+ CTI #1                                           |
| 62        | cpuss_interrupts_cm7_0_cti_0_IRQn  | Active     | CM7_0 CTI #0                                          |
| 63        | cpuss_interrupts_cm7_0_cti_1_IRQn  | Active     | CM7_0 CTI #1                                          |
| 64        | cpuss_interrupts_cm7_1_cti_0_IRQn  | Active     | CM7_1 CTI #0                                          |
| 65        | cpuss_interrupts_cm7_1_cti_1_IRQn  | Active     | CM7_1 CTI #1                                          |
| 66        | evtgen_0_interrupt_IRQn            | Active     | Event gen Active domain Interrupt                     |
| 67        | canfd_0_interrupt0_IRQn            | Active     | CAN0, Consolidated Interrupt #0 for all four channels |
| 68        | canfd_0_interrupt1_IRQn            | Active     | CAN0, Consolidated Interrupt #1 for all four channels |
| 69        | canfd_1_interrupt0_IRQn            | Active     | CAN1, Consolidated Interrupt #0 for all four channels |
| 70        | canfd_1_interrupt1_IRQn            | Active     | CAN1, Consolidated Interrupt #1 for all four channels |
| 71        | canfd_0_interrupts0_0_IRQn         | Active     | CAN0, Interrupt #0, Channel #0                        |
| 72        | canfd_0_interrupts0_1_IRQn         | Active     | CAN0, Interrupt #0, Channel #1                        |
| 73        | canfd_0_interrupts0_2_IRQn         | Active     | CAN0, Interrupt #0, Channel #2                        |
| 74        | canfd_0_interrupts0_3_IRQn         | Active     | CAN0, Interrupt #0, Channel #3                        |
| 75        | canfd_0_interrupts1_0_IRQn         | Active     | CAN0, Interrupt #1, Channel #0                        |
| 76        | canfd_0_interrupts1_1_IRQn         | Active     | CAN0, Interrupt #1, Channel #1                        |
| 77        | canfd_0_interrupts1_2_IRQn         | Active     | CAN0, Interrupt #1, Channel #2                        |
| 78        | canfd_0_interrupts1_3_IRQn         | Active     | CAN0, Interrupt #1, Channel #3                        |
| 79        | canfd_1_interrupts0_0_IRQn         | Active     | CAN1, Interrupt #0, Channel #0                        |
| 80        | canfd_1_interrupts0_1_IRQn         | Active     | CAN1, Interrupt #0, Channel #1                        |
| 81        | canfd_1_interrupts0_2_IRQn         | Active     | CAN1, Interrupt #0, Channel #2                        |
| 82        | canfd_1_interrupts0_3_IRQn         | Active     | CAN1, Interrupt #0, Channel #3                        |
| 83        | canfd_1_interrupts1_0_IRQn         | Active     | CAN1, Interrupt #1, Channel #0                        |
| 84        | canfd_1_interrupts1_1_IRQn         | Active     | CAN1, Interrupt #1, Channel #1                        |
| 85        | canfd_1_interrupts1_2_IRQn         | Active     | CAN1, Interrupt #1, Channel #2                        |
| 86        | canfd_1_interrupts1_3_IRQn         | Active     | CAN1, Interrupt #1, Channel #3                        |
| 87        | lin_0_interrupts_0_IRQn            | Active     | LIN0, Channel #0 Interrupt                            |

## Interrupts and wake-up assignments

**Table 14-1 Peripheral interrupt assignments and wake-up sources** *(continued)*

| Interrupt | Source                        | Power Mode | Description                         |
|-----------|-------------------------------|------------|-------------------------------------|
| 88        | lin_0_interrupts_1_IRQn       | Active     | LIN0, Channel #1 Interrupt          |
| 89        | lin_0_interrupts_2_IRQn       | Active     | LIN0, Channel #2 Interrupt          |
| 90        | lin_0_interrupts_3_IRQn       | Active     | LIN0, Channel #3 Interrupt          |
| 91        | lin_0_interrupts_4_IRQn       | Active     | LIN0, Channel #4 Interrupt          |
| 92        | lin_0_interrupts_5_IRQn       | Active     | LIN0, Channel #5 Interrupt          |
| 93        | lin_0_interrupts_6_IRQn       | Active     | LIN0, Channel #6 Interrupt          |
| 94        | lin_0_interrupts_7_IRQn       | Active     | LIN0, Channel #7 Interrupt          |
| 95        | lin_0_interrupts_8_IRQn       | Active     | LIN0, Channel #8 Interrupt          |
| 96        | lin_0_interrupts_9_IRQn       | Active     | LIN0, Channel #9 Interrupt          |
| 97        | lin_0_interrupts_10_IRQn      | Active     | LIN0, Channel #10 Interrupt         |
| 98        | lin_0_interrupts_11_IRQn      | Active     | LIN0, Channel #11 Interrupt         |
| 99        | lin_0_interrupts_12_IRQn      | Active     | LIN0, Channel #12 Interrupt         |
| 100       | lin_0_interrupts_13_IRQn      | Active     | LIN0, Channel #13 Interrupt         |
| 101       | lin_0_interrupts_14_IRQn      | Active     | LIN0, Channel #14 Interrupt         |
| 102       | lin_0_interrupts_15_IRQn      | Active     | LIN0, Channel #15 Interrupt         |
| 103       | scb_1_interrupt_IRQn          | Active     | SCB1 Interrupt                      |
| 104       | scb_2_interrupt_IRQn          | Active     | SCB2 Interrupt                      |
| 105       | scb_3_interrupt_IRQn          | Active     | SCB3 Interrupt                      |
| 106       | scb_4_interrupt_IRQn          | Active     | SCB4 Interrupt                      |
| 107       | scb_5_interrupt_IRQn          | Active     | SCB5 Interrupt                      |
| 108       | scb_6_interrupt_IRQn          | Active     | SCB6 Interrupt                      |
| 109       | scb_7_interrupt_IRQn          | Active     | SCB7 Interrupt                      |
| 110       | scb_8_interrupt_IRQn          | Active     | SCB8 Interrupt                      |
| 111       | scb_9_interrupt_IRQn          | Active     | SCB9 Interrupt                      |
| 112       | scb_10_interrupt_IRQn         | Active     | SCB10 Interrupt                     |
| 113       | pass_0_interrupts_sar_0_IRQn  | Active     | SAR0, Logical Channel #0 Interrupt  |
| 114       | pass_0_interrupts_sar_1_IRQn  | Active     | SAR0, Logical Channel #1 Interrupt  |
| 115       | pass_0_interrupts_sar_2_IRQn  | Active     | SAR0, Logical Channel #2 Interrupt  |
| 116       | pass_0_interrupts_sar_3_IRQn  | Active     | SAR0, Logical Channel #3 Interrupt  |
| 117       | pass_0_interrupts_sar_4_IRQn  | Active     | SAR0, Logical Channel #4 Interrupt  |
| 118       | pass_0_interrupts_sar_5_IRQn  | Active     | SAR0, Logical Channel #5 Interrupt  |
| 119       | pass_0_interrupts_sar_6_IRQn  | Active     | SAR0, Logical Channel #6 Interrupt  |
| 120       | pass_0_interrupts_sar_7_IRQn  | Active     | SAR0, Logical Channel #7 Interrupt  |
| 121       | pass_0_interrupts_sar_8_IRQn  | Active     | SAR0, Logical Channel #8 Interrupt  |
| 122       | pass_0_interrupts_sar_9_IRQn  | Active     | SAR0, Logical Channel #9 Interrupt  |
| 123       | pass_0_interrupts_sar_10_IRQn | Active     | SAR0, Logical Channel #10 Interrupt |
| 124       | pass_0_interrupts_sar_11_IRQn | Active     | SAR0, Logical Channel #11 Interrupt |
| 125       | pass_0_interrupts_sar_12_IRQn | Active     | SAR0, Logical Channel #12 Interrupt |
| 126       | pass_0_interrupts_sar_13_IRQn | Active     | SAR0, Logical Channel #13 Interrupt |
| 127       | pass_0_interrupts_sar_14_IRQn | Active     | SAR0, Logical Channel #14 Interrupt |
| 128       | pass_0_interrupts_sar_15_IRQn | Active     | SAR0, Logical Channel #15 Interrupt |
| 129       | pass_0_interrupts_sar_16_IRQn | Active     | SAR0, Logical Channel #16 Interrupt |
| 130       | pass_0_interrupts_sar_17_IRQn | Active     | SAR0, Logical Channel #17 Interrupt |
| 131       | pass_0_interrupts_sar_18_IRQn | Active     | SAR0, Logical Channel #18 Interrupt |
| 132       | pass_0_interrupts_sar_19_IRQn | Active     | SAR0, Logical Channel #19 Interrupt |

## Interrupts and wake-up assignments

**Table 14-1 Peripheral interrupt assignments and wake-up sources (continued)**

| Interrupt | Source                        | Power Mode | Description                         |
|-----------|-------------------------------|------------|-------------------------------------|
| 133       | pass_0_interrupts_sar_20_IRQn | Active     | SAR0, Logical Channel #20 Interrupt |
| 134       | pass_0_interrupts_sar_21_IRQn | Active     | SAR0, Logical Channel #21 Interrupt |
| 135       | pass_0_interrupts_sar_22_IRQn | Active     | SAR0, Logical Channel #22 Interrupt |
| 136       | pass_0_interrupts_sar_23_IRQn | Active     | SAR0, Logical Channel #23 Interrupt |
| 137       | pass_0_interrupts_sar_24_IRQn | Active     | SAR0, Logical Channel #24 Interrupt |
| 138       | pass_0_interrupts_sar_25_IRQn | Active     | SAR0, Logical Channel #25 Interrupt |
| 139       | pass_0_interrupts_sar_26_IRQn | Active     | SAR0, Logical Channel #26 Interrupt |
| 140       | pass_0_interrupts_sar_27_IRQn | Active     | SAR0, Logical Channel #27 Interrupt |
| 141       | pass_0_interrupts_sar_28_IRQn | Active     | SAR0, Logical Channel #28 Interrupt |
| 142       | pass_0_interrupts_sar_29_IRQn | Active     | SAR0, Logical Channel #29 Interrupt |
| 143       | pass_0_interrupts_sar_30_IRQn | Active     | SAR0, Logical Channel #30 Interrupt |
| 144       | pass_0_interrupts_sar_31_IRQn | Active     | SAR0, Logical Channel #31 Interrupt |
| 145       | pass_0_interrupts_sar_32_IRQn | Active     | SAR1, Logical Channel #0 Interrupt  |
| 146       | pass_0_interrupts_sar_33_IRQn | Active     | SAR1, Logical Channel #1 Interrupt  |
| 147       | pass_0_interrupts_sar_34_IRQn | Active     | SAR1, Logical Channel #2 Interrupt  |
| 148       | pass_0_interrupts_sar_35_IRQn | Active     | SAR1, Logical Channel #3 Interrupt  |
| 149       | pass_0_interrupts_sar_36_IRQn | Active     | SAR1, Logical Channel #4 Interrupt  |
| 150       | pass_0_interrupts_sar_37_IRQn | Active     | SAR1, Logical Channel #5 Interrupt  |
| 151       | pass_0_interrupts_sar_38_IRQn | Active     | SAR1, Logical Channel #6 Interrupt  |
| 152       | pass_0_interrupts_sar_39_IRQn | Active     | SAR1, Logical Channel #7 Interrupt  |
| 153       | pass_0_interrupts_sar_40_IRQn | Active     | SAR1, Logical Channel #8 Interrupt  |
| 154       | pass_0_interrupts_sar_41_IRQn | Active     | SAR1, Logical Channel #9 Interrupt  |
| 155       | pass_0_interrupts_sar_42_IRQn | Active     | SAR1, Logical Channel #10 Interrupt |
| 156       | pass_0_interrupts_sar_43_IRQn | Active     | SAR1, Logical Channel #11 Interrupt |
| 157       | pass_0_interrupts_sar_44_IRQn | Active     | SAR1, Logical Channel #12 Interrupt |
| 158       | pass_0_interrupts_sar_45_IRQn | Active     | SAR1, Logical Channel #13 Interrupt |
| 159       | pass_0_interrupts_sar_46_IRQn | Active     | SAR1, Logical Channel #14 Interrupt |
| 160       | pass_0_interrupts_sar_47_IRQn | Active     | SAR1, Logical Channel #15 Interrupt |
| 161       | pass_0_interrupts_sar_48_IRQn | Active     | SAR1, Logical Channel #16 Interrupt |
| 162       | pass_0_interrupts_sar_49_IRQn | Active     | SAR1, Logical Channel #17 Interrupt |
| 163       | pass_0_interrupts_sar_50_IRQn | Active     | SAR1, Logical Channel #18 Interrupt |
| 164       | pass_0_interrupts_sar_51_IRQn | Active     | SAR1, Logical Channel #19 Interrupt |
| 165       | pass_0_interrupts_sar_52_IRQn | Active     | SAR1, Logical Channel #20 Interrupt |
| 166       | pass_0_interrupts_sar_53_IRQn | Active     | SAR1, Logical Channel #21 Interrupt |
| 167       | pass_0_interrupts_sar_54_IRQn | Active     | SAR1, Logical Channel #22 Interrupt |
| 168       | pass_0_interrupts_sar_55_IRQn | Active     | SAR1, Logical Channel #23 Interrupt |
| 169       | pass_0_interrupts_sar_56_IRQn | Active     | SAR1, Logical Channel #24 Interrupt |
| 170       | pass_0_interrupts_sar_57_IRQn | Active     | SAR1, Logical Channel #25 Interrupt |
| 171       | pass_0_interrupts_sar_58_IRQn | Active     | SAR1, Logical Channel #26 Interrupt |
| 172       | pass_0_interrupts_sar_59_IRQn | Active     | SAR1, Logical Channel #27 Interrupt |
| 173       | pass_0_interrupts_sar_60_IRQn | Active     | SAR1, Logical Channel #28 Interrupt |
| 174       | pass_0_interrupts_sar_61_IRQn | Active     | SAR1, Logical Channel #29 Interrupt |
| 175       | pass_0_interrupts_sar_62_IRQn | Active     | SAR1, Logical Channel #30 Interrupt |
| 176       | pass_0_interrupts_sar_63_IRQn | Active     | SAR1, Logical Channel #31 Interrupt |
| 177       | pass_0_interrupts_sar_64_IRQn | Active     | SAR2, Logical Channel #0 Interrupt  |

## Interrupts and wake-up assignments

**Table 14-1 Peripheral interrupt assignments and wake-up sources (continued)**

| Interrupt | Source                        | Power Mode | Description                         |
|-----------|-------------------------------|------------|-------------------------------------|
| 178       | pass_0_interrupts_sar_65_IRQn | Active     | SAR2, Logical Channel #1 Interrupt  |
| 179       | pass_0_interrupts_sar_66_IRQn | Active     | SAR2, Logical Channel #2 Interrupt  |
| 180       | pass_0_interrupts_sar_67_IRQn | Active     | SAR2, Logical Channel #3 Interrupt  |
| 181       | pass_0_interrupts_sar_68_IRQn | Active     | SAR2, Logical Channel #4 Interrupt  |
| 182       | pass_0_interrupts_sar_69_IRQn | Active     | SAR2, Logical Channel #5 Interrupt  |
| 183       | pass_0_interrupts_sar_70_IRQn | Active     | SAR2, Logical Channel #6 Interrupt  |
| 184       | pass_0_interrupts_sar_71_IRQn | Active     | SAR2, Logical Channel #7 Interrupt  |
| 185       | cpuss_interrupts_dmac_0_IRQn  | Active     | CPUSS M-DMA0, Channel #0 Interrupt  |
| 186       | cpuss_interrupts_dmac_1_IRQn  | Active     | CPUSS M-DMA0, Channel #1 Interrupt  |
| 187       | cpuss_interrupts_dmac_2_IRQn  | Active     | CPUSS M-DMA0, Channel #2 Interrupt  |
| 188       | cpuss_interrupts_dmac_3_IRQn  | Active     | CPUSS M-DMA0, Channel #3 Interrupt  |
| 189       | cpuss_interrupts_dmac_4_IRQn  | Active     | CPUSS M-DMA0, Channel #4 Interrupt  |
| 190       | cpuss_interrupts_dmac_5_IRQn  | Active     | CPUSS M-DMA0, Channel #5 Interrupt  |
| 191       | cpuss_interrupts_dmac_6_IRQn  | Active     | CPUSS M-DMA0, Channel #6 Interrupt  |
| 192       | cpuss_interrupts_dmac_7_IRQn  | Active     | CPUSS M-DMA0, Channel #7 Interrupt  |
| 193       | cpuss_interrupts_dw0_0_IRQn   | Active     | CPUSS P-DMA0, Channel #0 Interrupt  |
| 194       | cpuss_interrupts_dw0_1_IRQn   | Active     | CPUSS P-DMA0, Channel #1 Interrupt  |
| 195       | cpuss_interrupts_dw0_2_IRQn   | Active     | CPUSS P-DMA0, Channel #2 Interrupt  |
| 196       | cpuss_interrupts_dw0_3_IRQn   | Active     | CPUSS P-DMA0, Channel #3 Interrupt  |
| 197       | cpuss_interrupts_dw0_4_IRQn   | Active     | CPUSS P-DMA0, Channel #4 Interrupt  |
| 198       | cpuss_interrupts_dw0_5_IRQn   | Active     | CPUSS P-DMA0, Channel #5 Interrupt  |
| 199       | cpuss_interrupts_dw0_6_IRQn   | Active     | CPUSS P-DMA0, Channel #6 Interrupt  |
| 200       | cpuss_interrupts_dw0_7_IRQn   | Active     | CPUSS P-DMA0, Channel #7 Interrupt  |
| 201       | cpuss_interrupts_dw0_8_IRQn   | Active     | CPUSS P-DMA0, Channel #8 Interrupt  |
| 202       | cpuss_interrupts_dw0_9_IRQn   | Active     | CPUSS P-DMA0, Channel #9 Interrupt  |
| 203       | cpuss_interrupts_dw0_10_IRQn  | Active     | CPUSS P-DMA0, Channel #10 Interrupt |
| 204       | cpuss_interrupts_dw0_11_IRQn  | Active     | CPUSS P-DMA0, Channel #11 Interrupt |
| 205       | cpuss_interrupts_dw0_12_IRQn  | Active     | CPUSS P-DMA0, Channel #12 Interrupt |
| 206       | cpuss_interrupts_dw0_13_IRQn  | Active     | CPUSS P-DMA0, Channel #13 Interrupt |
| 207       | cpuss_interrupts_dw0_14_IRQn  | Active     | CPUSS P-DMA0, Channel #14 Interrupt |
| 208       | cpuss_interrupts_dw0_15_IRQn  | Active     | CPUSS P-DMA0, Channel #15 Interrupt |
| 209       | cpuss_interrupts_dw0_16_IRQn  | Active     | CPUSS P-DMA0, Channel #16 Interrupt |
| 210       | cpuss_interrupts_dw0_17_IRQn  | Active     | CPUSS P-DMA0, Channel #17 Interrupt |
| 211       | cpuss_interrupts_dw0_18_IRQn  | Active     | CPUSS P-DMA0, Channel #18 Interrupt |
| 212       | cpuss_interrupts_dw0_19_IRQn  | Active     | CPUSS P-DMA0, Channel #19 Interrupt |
| 213       | cpuss_interrupts_dw0_20_IRQn  | Active     | CPUSS P-DMA0, Channel #20 Interrupt |
| 214       | cpuss_interrupts_dw0_21_IRQn  | Active     | CPUSS P-DMA0, Channel #21 Interrupt |
| 215       | cpuss_interrupts_dw0_22_IRQn  | Active     | CPUSS P-DMA0, Channel #22 Interrupt |
| 216       | cpuss_interrupts_dw0_23_IRQn  | Active     | CPUSS P-DMA0, Channel #23 Interrupt |
| 217       | cpuss_interrupts_dw0_24_IRQn  | Active     | CPUSS P-DMA0, Channel #24 Interrupt |
| 218       | cpuss_interrupts_dw0_25_IRQn  | Active     | CPUSS P-DMA0, Channel #25 Interrupt |
| 219       | cpuss_interrupts_dw0_26_IRQn  | Active     | CPUSS P-DMA0, Channel #26 Interrupt |
| 220       | cpuss_interrupts_dw0_27_IRQn  | Active     | CPUSS P-DMA0, Channel #27 Interrupt |
| 221       | cpuss_interrupts_dw0_28_IRQn  | Active     | CPUSS P-DMA0, Channel #28 Interrupt |
| 222       | cpuss_interrupts_dw0_29_IRQn  | Active     | CPUSS P-DMA0, Channel #29 Interrupt |

**Table 14-1 Peripheral interrupt assignments and wake-up sources** *(continued)*

| Interrupt | Source                       | Power Mode | Description                         |
|-----------|------------------------------|------------|-------------------------------------|
| 223       | cpuss_interrupts_dw0_30_IRQn | Active     | CPUSS P-DMA0, Channel #30 Interrupt |
| 224       | cpuss_interrupts_dw0_31_IRQn | Active     | CPUSS P-DMA0, Channel #31 Interrupt |
| 225       | cpuss_interrupts_dw0_32_IRQn | Active     | CPUSS P-DMA0, Channel #32 Interrupt |
| 226       | cpuss_interrupts_dw0_33_IRQn | Active     | CPUSS P-DMA0, Channel #33 Interrupt |
| 227       | cpuss_interrupts_dw0_34_IRQn | Active     | CPUSS P-DMA0, Channel #34 Interrupt |
| 228       | cpuss_interrupts_dw0_35_IRQn | Active     | CPUSS P-DMA0, Channel #35 Interrupt |
| 229       | cpuss_interrupts_dw0_36_IRQn | Active     | CPUSS P-DMA0, Channel #36 Interrupt |
| 230       | cpuss_interrupts_dw0_37_IRQn | Active     | CPUSS P-DMA0, Channel #37 Interrupt |
| 231       | cpuss_interrupts_dw0_38_IRQn | Active     | CPUSS P-DMA0, Channel #38 Interrupt |
| 232       | cpuss_interrupts_dw0_39_IRQn | Active     | CPUSS P-DMA0, Channel #39 Interrupt |
| 233       | cpuss_interrupts_dw0_40_IRQn | Active     | CPUSS P-DMA0, Channel #40 Interrupt |
| 234       | cpuss_interrupts_dw0_41_IRQn | Active     | CPUSS P-DMA0, Channel #41 Interrupt |
| 235       | cpuss_interrupts_dw0_42_IRQn | Active     | CPUSS P-DMA0, Channel #42 Interrupt |
| 236       | cpuss_interrupts_dw0_43_IRQn | Active     | CPUSS P-DMA0, Channel #43 Interrupt |
| 237       | cpuss_interrupts_dw0_44_IRQn | Active     | CPUSS P-DMA0, Channel #44 Interrupt |
| 238       | cpuss_interrupts_dw0_45_IRQn | Active     | CPUSS P-DMA0, Channel #45 Interrupt |
| 239       | cpuss_interrupts_dw0_46_IRQn | Active     | CPUSS P-DMA0, Channel #46 Interrupt |
| 240       | cpuss_interrupts_dw0_47_IRQn | Active     | CPUSS P-DMA0, Channel #47 Interrupt |
| 241       | cpuss_interrupts_dw0_48_IRQn | Active     | CPUSS P-DMA0, Channel #48 Interrupt |
| 242       | cpuss_interrupts_dw0_49_IRQn | Active     | CPUSS P-DMA0, Channel #49 Interrupt |
| 243       | cpuss_interrupts_dw0_50_IRQn | Active     | CPUSS P-DMA0, Channel #50 Interrupt |
| 244       | cpuss_interrupts_dw0_51_IRQn | Active     | CPUSS P-DMA0, Channel #51 Interrupt |
| 245       | cpuss_interrupts_dw0_52_IRQn | Active     | CPUSS P-DMA0, Channel #52 Interrupt |
| 246       | cpuss_interrupts_dw0_53_IRQn | Active     | CPUSS P-DMA0, Channel #53 Interrupt |
| 247       | cpuss_interrupts_dw0_54_IRQn | Active     | CPUSS P-DMA0, Channel #54 Interrupt |
| 248       | cpuss_interrupts_dw0_55_IRQn | Active     | CPUSS P-DMA0, Channel #55 Interrupt |
| 249       | cpuss_interrupts_dw0_56_IRQn | Active     | CPUSS P-DMA0, Channel #56 Interrupt |
| 250       | cpuss_interrupts_dw0_57_IRQn | Active     | CPUSS P-DMA0, Channel #57 Interrupt |
| 251       | cpuss_interrupts_dw0_58_IRQn | Active     | CPUSS P-DMA0, Channel #58 Interrupt |
| 252       | cpuss_interrupts_dw0_59_IRQn | Active     | CPUSS P-DMA0, Channel #59 Interrupt |
| 253       | cpuss_interrupts_dw0_60_IRQn | Active     | CPUSS P-DMA0, Channel #60 Interrupt |
| 254       | cpuss_interrupts_dw0_61_IRQn | Active     | CPUSS P-DMA0, Channel #61 Interrupt |
| 255       | cpuss_interrupts_dw0_62_IRQn | Active     | CPUSS P-DMA0, Channel #62 Interrupt |
| 256       | cpuss_interrupts_dw0_63_IRQn | Active     | CPUSS P-DMA0, Channel #63 Interrupt |
| 257       | cpuss_interrupts_dw0_64_IRQn | Active     | CPUSS P-DMA0, Channel #64 Interrupt |
| 258       | cpuss_interrupts_dw0_65_IRQn | Active     | CPUSS P-DMA0, Channel #65 Interrupt |
| 259       | cpuss_interrupts_dw0_66_IRQn | Active     | CPUSS P-DMA0, Channel #66 Interrupt |
| 260       | cpuss_interrupts_dw0_67_IRQn | Active     | CPUSS P-DMA0, Channel #67 Interrupt |
| 261       | cpuss_interrupts_dw0_68_IRQn | Active     | CPUSS P-DMA0, Channel #68 Interrupt |
| 262       | cpuss_interrupts_dw0_69_IRQn | Active     | CPUSS P-DMA0, Channel #69 Interrupt |
| 263       | cpuss_interrupts_dw0_70_IRQn | Active     | CPUSS P-DMA0, Channel #70 Interrupt |
| 264       | cpuss_interrupts_dw0_71_IRQn | Active     | CPUSS P-DMA0, Channel #71 Interrupt |
| 265       | cpuss_interrupts_dw0_72_IRQn | Active     | CPUSS P-DMA0, Channel #72 Interrupt |
| 266       | cpuss_interrupts_dw0_73_IRQn | Active     | CPUSS P-DMA0, Channel #73 Interrupt |
| 267       | cpuss_interrupts_dw0_74_IRQn | Active     | CPUSS P-DMA0, Channel #74 Interrupt |

**Table 14-1 Peripheral interrupt assignments and wake-up sources (continued)**

| Interrupt | Source                       | Power Mode | Description                         |
|-----------|------------------------------|------------|-------------------------------------|
| 268       | cpuss_interrupts_dw0_75_IRQn | Active     | CPUSS P-DMA0, Channel #75 Interrupt |
| 269       | cpuss_interrupts_dw0_76_IRQn | Active     | CPUSS P-DMA0, Channel #76 Interrupt |
| 270       | cpuss_interrupts_dw0_77_IRQn | Active     | CPUSS P-DMA0, Channel #77 Interrupt |
| 271       | cpuss_interrupts_dw0_78_IRQn | Active     | CPUSS P-DMA0, Channel #78 Interrupt |
| 272       | cpuss_interrupts_dw0_79_IRQn | Active     | CPUSS P-DMA0, Channel #79 Interrupt |
| 273       | cpuss_interrupts_dw0_80_IRQn | Active     | CPUSS P-DMA0, Channel #80 Interrupt |
| 274       | cpuss_interrupts_dw0_81_IRQn | Active     | CPUSS P-DMA0, Channel #81 Interrupt |
| 275       | cpuss_interrupts_dw0_82_IRQn | Active     | CPUSS P-DMA0, Channel #82 Interrupt |
| 276       | cpuss_interrupts_dw0_83_IRQn | Active     | CPUSS P-DMA0, Channel #83 Interrupt |
| 277       | cpuss_interrupts_dw0_84_IRQn | Active     | CPUSS P-DMA0, Channel #84 Interrupt |
| 278       | cpuss_interrupts_dw0_85_IRQn | Active     | CPUSS P-DMA0, Channel #85 Interrupt |
| 279       | cpuss_interrupts_dw0_86_IRQn | Active     | CPUSS P-DMA0, Channel #86 Interrupt |
| 280       | cpuss_interrupts_dw0_87_IRQn | Active     | CPUSS P-DMA0, Channel #87 Interrupt |
| 281       | cpuss_interrupts_dw0_88_IRQn | Active     | CPUSS P-DMA0, Channel #88 Interrupt |
| 282       | cpuss_interrupts_dw0_89_IRQn | Active     | CPUSS P-DMA0, Channel #89 Interrupt |
| 283       | cpuss_interrupts_dw0_90_IRQn | Active     | CPUSS P-DMA0, Channel #90 Interrupt |
| 284       | cpuss_interrupts_dw0_91_IRQn | Active     | CPUSS P-DMA0, Channel #91 Interrupt |
| 285       | cpuss_interrupts_dw0_92_IRQn | Active     | CPUSS P-DMA0, Channel #92 Interrupt |
| 286       | cpuss_interrupts_dw0_93_IRQn | Active     | CPUSS P-DMA0, Channel #93 Interrupt |
| 287       | cpuss_interrupts_dw0_94_IRQn | Active     | CPUSS P-DMA0, Channel #94 Interrupt |
| 288       | cpuss_interrupts_dw0_95_IRQn | Active     | CPUSS P-DMA0, Channel #95 Interrupt |
| 289       | cpuss_interrupts_dw0_96_IRQn | Active     | CPUSS P-DMA0, Channel #96 Interrupt |
| 290       | cpuss_interrupts_dw0_97_IRQn | Active     | CPUSS P-DMA0, Channel #97 Interrupt |
| 291       | cpuss_interrupts_dw0_98_IRQn | Active     | CPUSS P-DMA0, Channel #98 Interrupt |
| 292       | cpuss_interrupts_dw0_99_IRQn | Active     | CPUSS P-DMA0, Channel #99 Interrupt |
| 293       | cpuss_interrupts_dw1_0_IRQn  | Active     | CPUSS P-DMA1, Channel #0 Interrupt  |
| 294       | cpuss_interrupts_dw1_1_IRQn  | Active     | CPUSS P-DMA1, Channel #1 Interrupt  |
| 295       | cpuss_interrupts_dw1_2_IRQn  | Active     | CPUSS P-DMA1, Channel #2 Interrupt  |
| 296       | cpuss_interrupts_dw1_3_IRQn  | Active     | CPUSS P-DMA1, Channel #3 Interrupt  |
| 297       | cpuss_interrupts_dw1_4_IRQn  | Active     | CPUSS P-DMA1, Channel #4 Interrupt  |
| 298       | cpuss_interrupts_dw1_5_IRQn  | Active     | CPUSS P-DMA1, Channel #5 Interrupt  |
| 299       | cpuss_interrupts_dw1_6_IRQn  | Active     | CPUSS P-DMA1, Channel #6 Interrupt  |
| 300       | cpuss_interrupts_dw1_7_IRQn  | Active     | CPUSS P-DMA1, Channel #7 Interrupt  |
| 301       | cpuss_interrupts_dw1_8_IRQn  | Active     | CPUSS P-DMA1, Channel #8 Interrupt  |
| 302       | cpuss_interrupts_dw1_9_IRQn  | Active     | CPUSS P-DMA1, Channel #9 Interrupt  |
| 303       | cpuss_interrupts_dw1_10_IRQn | Active     | CPUSS P-DMA1, Channel #10 Interrupt |
| 304       | cpuss_interrupts_dw1_11_IRQn | Active     | CPUSS P-DMA1, Channel #11 Interrupt |
| 305       | cpuss_interrupts_dw1_12_IRQn | Active     | CPUSS P-DMA1, Channel #12 Interrupt |
| 306       | cpuss_interrupts_dw1_13_IRQn | Active     | CPUSS P-DMA1, Channel #13 Interrupt |
| 307       | cpuss_interrupts_dw1_14_IRQn | Active     | CPUSS P-DMA1, Channel #14 Interrupt |
| 308       | cpuss_interrupts_dw1_15_IRQn | Active     | CPUSS P-DMA1, Channel #15 Interrupt |
| 309       | cpuss_interrupts_dw1_16_IRQn | Active     | CPUSS P-DMA1, Channel #16 Interrupt |
| 310       | cpuss_interrupts_dw1_17_IRQn | Active     | CPUSS P-DMA1, Channel #17 Interrupt |
| 311       | cpuss_interrupts_dw1_18_IRQn | Active     | CPUSS P-DMA1, Channel #18 Interrupt |
| 312       | cpuss_interrupts_dw1_19_IRQn | Active     | CPUSS P-DMA1, Channel #19 Interrupt |

## Interrupts and wake-up assignments

**Table 14-1 Peripheral interrupt assignments and wake-up sources (continued)**

| Interrupt | Source                       | Power Mode | Description                           |
|-----------|------------------------------|------------|---------------------------------------|
| 313       | cpuss_interrupts_dw1_20_IRQn | Active     | CPUSS P-DMA1, Channel #20 Interrupt   |
| 314       | cpuss_interrupts_dw1_21_IRQn | Active     | CPUSS P-DMA1, Channel #21 Interrupt   |
| 315       | cpuss_interrupts_dw1_22_IRQn | Active     | CPUSS P-DMA1, Channel #22 Interrupt   |
| 316       | cpuss_interrupts_dw1_23_IRQn | Active     | CPUSS P-DMA1, Channel #23 Interrupt   |
| 317       | cpuss_interrupts_dw1_24_IRQn | Active     | CPUSS P-DMA1, Channel #24 Interrupt   |
| 318       | cpuss_interrupts_dw1_25_IRQn | Active     | CPUSS P-DMA1, Channel #25 Interrupt   |
| 319       | cpuss_interrupts_dw1_26_IRQn | Active     | CPUSS P-DMA1, Channel #26 Interrupt   |
| 320       | cpuss_interrupts_dw1_27_IRQn | Active     | CPUSS P-DMA1, Channel #27 Interrupt   |
| 321       | cpuss_interrupts_dw1_28_IRQn | Active     | CPUSS P-DMA1, Channel #28 Interrupt   |
| 322       | cpuss_interrupts_dw1_29_IRQn | Active     | CPUSS P-DMA1, Channel #29 Interrupt   |
| 323       | cpuss_interrupts_dw1_30_IRQn | Active     | CPUSS P-DMA1, Channel #30 Interrupt   |
| 324       | cpuss_interrupts_dw1_31_IRQn | Active     | CPUSS P-DMA1, Channel #31 Interrupt   |
| 325       | cpuss_interrupts_dw1_32_IRQn | Active     | CPUSS P-DMA1, Channel #32 Interrupt   |
| 326       | cpuss_interrupts_dw1_33_IRQn | Active     | CPUSS P-DMA1, Channel #33 Interrupt   |
| 327       | cpuss_interrupts_dw1_34_IRQn | Active     | CPUSS P-DMA1, Channel #34 Interrupt   |
| 328       | cpuss_interrupts_dw1_35_IRQn | Active     | CPUSS P-DMA1, Channel #35 Interrupt   |
| 329       | cpuss_interrupts_dw1_36_IRQn | Active     | CPUSS P-DMA1, Channel #36 Interrupt   |
| 330       | cpuss_interrupts_dw1_37_IRQn | Active     | CPUSS P-DMA1, Channel #37 Interrupt   |
| 331       | cpuss_interrupts_dw1_38_IRQn | Active     | CPUSS P-DMA1, Channel #38 Interrupt   |
| 332       | cpuss_interrupts_dw1_39_IRQn | Active     | CPUSS P-DMA1, Channel #39 Interrupt   |
| 333       | cpuss_interrupts_dw1_40_IRQn | Active     | CPUSS P-DMA1, Channel #40 Interrupt   |
| 334       | cpuss_interrupts_dw1_41_IRQn | Active     | CPUSS P-DMA1, Channel #41 Interrupt   |
| 335       | cpuss_interrupts_dw1_42_IRQn | Active     | CPUSS P-DMA1, Channel #42 Interrupt   |
| 336       | cpuss_interrupts_dw1_43_IRQn | Active     | CPUSS P-DMA1, Channel #43 Interrupt   |
| 337       | cpuss_interrupts_dw1_44_IRQn | Active     | CPUSS P-DMA1, Channel #44 Interrupt   |
| 338       | cpuss_interrupts_dw1_45_IRQn | Active     | CPUSS P-DMA1, Channel #45 Interrupt   |
| 339       | cpuss_interrupts_dw1_46_IRQn | Active     | CPUSS P-DMA1, Channel #46 Interrupt   |
| 340       | cpuss_interrupts_dw1_47_IRQn | Active     | CPUSS P-DMA1, Channel #47 Interrupt   |
| 341       | cpuss_interrupts_dw1_48_IRQn | Active     | CPUSS P-DMA1, Channel #48 Interrupt   |
| 342       | cpuss_interrupts_dw1_49_IRQn | Active     | CPUSS P-DMA1, Channel #49 Interrupt   |
| 343       | cpuss_interrupts_dw1_50_IRQn | Active     | CPUSS P-DMA1, Channel #50 Interrupt   |
| 344       | cpuss_interrupts_dw1_51_IRQn | Active     | CPUSS P-DMA1, Channel #51 Interrupt   |
| 345       | cpuss_interrupts_dw1_52_IRQn | Active     | CPUSS P-DMA1, Channel #52 Interrupt   |
| 346       | cpuss_interrupts_dw1_53_IRQn | Active     | CPUSS P-DMA1, Channel #53 Interrupt   |
| 347       | cpuss_interrupts_dw1_54_IRQn | Active     | CPUSS P-DMA1, Channel #54 Interrupt   |
| 348       | cpuss_interrupts_dw1_55_IRQn | Active     | CPUSS P-DMA1, Channel #55 Interrupt   |
| 349       | cpuss_interrupts_dw1_56_IRQn | Active     | CPUSS P-DMA1, Channel #56 Interrupt   |
| 350       | cpuss_interrupts_dw1_57_IRQn | Active     | CPUSS P-DMA1, Channel #57 Interrupt   |
| 351       | tcpwm_0_interrupts_0_IRQn    | Active     | TCPWM0 Group #0, Counter #0 Interrupt |
| 352       | tcpwm_0_interrupts_1_IRQn    | Active     | TCPWM0 Group #0, Counter #1 Interrupt |
| 353       | tcpwm_0_interrupts_2_IRQn    | Active     | TCPWM0 Group #0, Counter #2 Interrupt |
| 354       | tcpwm_0_interrupts_3_IRQn    | Active     | TCPWM0 Group #0, Counter #3 Interrupt |
| 355       | tcpwm_0_interrupts_4_IRQn    | Active     | TCPWM0 Group #0, Counter #4 Interrupt |
| 356       | tcpwm_0_interrupts_5_IRQn    | Active     | TCPWM0 Group #0, Counter #5 Interrupt |
| 357       | tcpwm_0_interrupts_6_IRQn    | Active     | TCPWM0 Group #0, Counter #6 Interrupt |

**Table 14-1 Peripheral interrupt assignments and wake-up sources (continued)**

| Interrupt | Source                     | Power Mode | Description                            |
|-----------|----------------------------|------------|----------------------------------------|
| 358       | tcpwm_0_interrupts_7_IRQn  | Active     | TCPWM0 Group #0, Counter #7 Interrupt  |
| 359       | tcpwm_0_interrupts_8_IRQn  | Active     | TCPWM0 Group #0, Counter #8 Interrupt  |
| 360       | tcpwm_0_interrupts_9_IRQn  | Active     | TCPWM0 Group #0, Counter #9 Interrupt  |
| 361       | tcpwm_0_interrupts_10_IRQn | Active     | TCPWM0 Group #0, Counter #10 Interrupt |
| 362       | tcpwm_0_interrupts_11_IRQn | Active     | TCPWM0 Group #0, Counter #11 Interrupt |
| 363       | tcpwm_0_interrupts_12_IRQn | Active     | TCPWM0 Group #0, Counter #12 Interrupt |
| 364       | tcpwm_0_interrupts_13_IRQn | Active     | TCPWM0 Group #0, Counter #13 Interrupt |
| 365       | tcpwm_0_interrupts_14_IRQn | Active     | TCPWM0 Group #0, Counter #14 Interrupt |
| 366       | tcpwm_0_interrupts_15_IRQn | Active     | TCPWM0 Group #0, Counter #15 Interrupt |
| 367       | tcpwm_0_interrupts_16_IRQn | Active     | TCPWM0 Group #0, Counter #16 Interrupt |
| 368       | tcpwm_0_interrupts_17_IRQn | Active     | TCPWM0 Group #0, Counter #17 Interrupt |
| 369       | tcpwm_0_interrupts_18_IRQn | Active     | TCPWM0 Group #0, Counter #18 Interrupt |
| 370       | tcpwm_0_interrupts_19_IRQn | Active     | TCPWM0 Group #0, Counter #19 Interrupt |
| 371       | tcpwm_0_interrupts_20_IRQn | Active     | TCPWM0 Group #0, Counter #20 Interrupt |
| 372       | tcpwm_0_interrupts_21_IRQn | Active     | TCPWM0 Group #0, Counter #21 Interrupt |
| 373       | tcpwm_0_interrupts_22_IRQn | Active     | TCPWM0 Group #0, Counter #22 Interrupt |
| 374       | tcpwm_0_interrupts_23_IRQn | Active     | TCPWM0 Group #0, Counter #23 Interrupt |
| 375       | tcpwm_0_interrupts_24_IRQn | Active     | TCPWM0 Group #0, Counter #24 Interrupt |
| 376       | tcpwm_0_interrupts_25_IRQn | Active     | TCPWM0 Group #0, Counter #25 Interrupt |
| 377       | tcpwm_0_interrupts_26_IRQn | Active     | TCPWM0 Group #0, Counter #26 Interrupt |
| 378       | tcpwm_0_interrupts_27_IRQn | Active     | TCPWM0 Group #0, Counter #27 Interrupt |
| 379       | tcpwm_0_interrupts_28_IRQn | Active     | TCPWM0 Group #0, Counter #28 Interrupt |
| 380       | tcpwm_0_interrupts_29_IRQn | Active     | TCPWM0 Group #0, Counter #29 Interrupt |
| 381       | tcpwm_0_interrupts_30_IRQn | Active     | TCPWM0 Group #0, Counter #30 Interrupt |
| 382       | tcpwm_0_interrupts_31_IRQn | Active     | TCPWM0 Group #0, Counter #31 Interrupt |
| 383       | tcpwm_0_interrupts_32_IRQn | Active     | TCPWM0 Group #0, Counter #32 Interrupt |
| 384       | tcpwm_0_interrupts_33_IRQn | Active     | TCPWM0 Group #0, Counter #33 Interrupt |
| 385       | tcpwm_0_interrupts_34_IRQn | Active     | TCPWM0 Group #0, Counter #34 Interrupt |
| 386       | tcpwm_0_interrupts_35_IRQn | Active     | TCPWM0 Group #0, Counter #35 Interrupt |
| 387       | tcpwm_0_interrupts_36_IRQn | Active     | TCPWM0 Group #0, Counter #36 Interrupt |
| 388       | tcpwm_0_interrupts_37_IRQn | Active     | TCPWM0 Group #0, Counter #37 Interrupt |
| 389       | tcpwm_0_interrupts_38_IRQn | Active     | TCPWM0 Group #0, Counter #38 Interrupt |
| 390       | tcpwm_0_interrupts_39_IRQn | Active     | TCPWM0 Group #0, Counter #39 Interrupt |
| 391       | tcpwm_0_interrupts_40_IRQn | Active     | TCPWM0 Group #0, Counter #40 Interrupt |
| 392       | tcpwm_0_interrupts_41_IRQn | Active     | TCPWM0 Group #0, Counter #41 Interrupt |
| 393       | tcpwm_0_interrupts_42_IRQn | Active     | TCPWM0 Group #0, Counter #42 Interrupt |
| 394       | tcpwm_0_interrupts_43_IRQn | Active     | TCPWM0 Group #0, Counter #43 Interrupt |
| 395       | tcpwm_0_interrupts_44_IRQn | Active     | TCPWM0 Group #0, Counter #44 Interrupt |
| 396       | tcpwm_0_interrupts_45_IRQn | Active     | TCPWM0 Group #0, Counter #45 Interrupt |
| 397       | tcpwm_0_interrupts_46_IRQn | Active     | TCPWM0 Group #0, Counter #46 Interrupt |
| 398       | tcpwm_0_interrupts_47_IRQn | Active     | TCPWM0 Group #0, Counter #47 Interrupt |
| 399       | tcpwm_0_interrupts_48_IRQn | Active     | TCPWM0 Group #0, Counter #48 Interrupt |
| 400       | tcpwm_0_interrupts_49_IRQn | Active     | TCPWM0 Group #0, Counter #49 Interrupt |
| 401       | tcpwm_0_interrupts_50_IRQn | Active     | TCPWM0 Group #0, Counter #50 Interrupt |
| 402       | tcpwm_0_interrupts_51_IRQn | Active     | TCPWM0 Group #0, Counter #51 Interrupt |

**Table 14-1 Peripheral interrupt assignments and wake-up sources (continued)**

| Interrupt | Source                        | Power Mode | Description                                 |
|-----------|-------------------------------|------------|---------------------------------------------|
| 403       | tcpwm_0_interrupts_52_IRQn    | Active     | TCPWM0 Group #0, Counter #52 Interrupt      |
| 404       | tcpwm_0_interrupts_53_IRQn    | Active     | TCPWM0 Group #0, Counter #53 Interrupt      |
| 405       | tcpwm_0_interrupts_54_IRQn    | Active     | TCPWM0 Group #0, Counter #54 Interrupt      |
| 406       | tcpwm_0_interrupts_55_IRQn    | Active     | TCPWM0 Group #0, Counter #55 Interrupt      |
| 407       | tcpwm_0_interrupts_56_IRQn    | Active     | TCPWM0 Group #0, Counter #56 Interrupt      |
| 408       | tcpwm_0_interrupts_57_IRQn    | Active     | TCPWM0 Group #0, Counter #57 Interrupt      |
| 409       | tcpwm_0_interrupts_58_IRQn    | Active     | TCPWM0 Group #0, Counter #58 Interrupt      |
| 410       | tcpwm_0_interrupts_59_IRQn    | Active     | TCPWM0 Group #0, Counter #59 Interrupt      |
| 411       | tcpwm_0_interrupts_60_IRQn    | Active     | TCPWM0 Group #0, Counter #60 Interrupt      |
| 412       | tcpwm_0_interrupts_61_IRQn    | Active     | TCPWM0 Group #0, Counter #61 Interrupt      |
| 413       | tcpwm_0_interrupts_62_IRQn    | Active     | TCPWM0 Group #0, Counter #62 Interrupt      |
| 414       | tcpwm_0_interrupts_256_IRQn   | Active     | TCPWM0 Group #1, Counter #0 Interrupt       |
| 415       | tcpwm_0_interrupts_257_IRQn   | Active     | TCPWM0 Group #1, Counter #1 Interrupt       |
| 416       | tcpwm_0_interrupts_258_IRQn   | Active     | TCPWM0 Group #1, Counter #2 Interrupt       |
| 417       | tcpwm_0_interrupts_259_IRQn   | Active     | TCPWM0 Group #1, Counter #3 Interrupt       |
| 418       | tcpwm_0_interrupts_260_IRQn   | Active     | TCPWM0 Group #1, Counter #4 Interrupt       |
| 419       | tcpwm_0_interrupts_261_IRQn   | Active     | TCPWM0 Group #1, Counter #5 Interrupt       |
| 420       | tcpwm_0_interrupts_262_IRQn   | Active     | TCPWM0 Group #1, Counter #6 Interrupt       |
| 421       | tcpwm_0_interrupts_263_IRQn   | Active     | TCPWM0 Group #1, Counter #7 Interrupt       |
| 422       | tcpwm_0_interrupts_264_IRQn   | Active     | TCPWM0 Group #1, Counter #8 Interrupt       |
| 423       | tcpwm_0_interrupts_265_IRQn   | Active     | TCPWM0 Group #1, Counter #9 Interrupt       |
| 424       | tcpwm_0_interrupts_266_IRQn   | Active     | TCPWM0 Group #1, Counter #10 Interrupt      |
| 425       | tcpwm_0_interrupts_267_IRQn   | Active     | TCPWM0 Group #1, Counter #11 Interrupt      |
| 426       | tcpwm_0_interrupts_512_IRQn   | Active     | TCPWM0 Group #2, Counter #0 Interrupt       |
| 427       | tcpwm_0_interrupts_513_IRQn   | Active     | TCPWM0 Group #2, Counter #1 Interrupt       |
| 428       | tcpwm_0_interrupts_514_IRQn   | Active     | TCPWM0 Group #2, Counter #2 Interrupt       |
| 429       | tcpwm_0_interrupts_515_IRQn   | Active     | TCPWM0 Group #2, Counter #3 Interrupt       |
| 430       | tcpwm_0_interrupts_516_IRQn   | Active     | TCPWM0 Group #2, Counter #4 Interrupt       |
| 431       | tcpwm_0_interrupts_517_IRQn   | Active     | TCPWM0 Group #2, Counter #5 Interrupt       |
| 432       | tcpwm_0_interrupts_518_IRQn   | Active     | TCPWM0 Group #2, Counter #6 Interrupt       |
| 433       | tcpwm_0_interrupts_519_IRQn   | Active     | TCPWM0 Group #2, Counter #7 Interrupt       |
| 434       | smif_0_interrupt_IRQn         | Active     | SMIF0 (QSPI) interrupt                      |
| 435       | eth_0_interrupt_eth_0_IRQn    | Active     | Ethernet0 interrupt for dma_priority_queue0 |
| 436       | eth_0_interrupt_eth_2_IRQn    | Active     | Ethernet0 interrupt for dma_priority_queue2 |
| 437       | eth_0_interrupt_eth_1_IRQn    | Active     | Ethernet0 interrupt for dma_priority_queue1 |
| 438       | sdhc_0_interrupt_general_IRQn | Active     | SDHC0 general interrupt                     |
| 439       | sdhc_0_interrupt_wakeup_IRQn  | Active     | SDHC0 wakeup interrupt                      |
| 440       | audioss_0_interrupt_i2s_IRQn  | Active     | AUDIOSS I <sup>2</sup> S0 interrupt         |
| 441       | audioss_1_interrupt_i2s_IRQn  | Active     | AUDIOSS I <sup>2</sup> S1 interrupt         |
| 442       | audioss_2_interrupt_i2s_IRQn  | Active     | AUDIOSS I <sup>2</sup> S2 interrupt         |

## 15 Core interrupt types

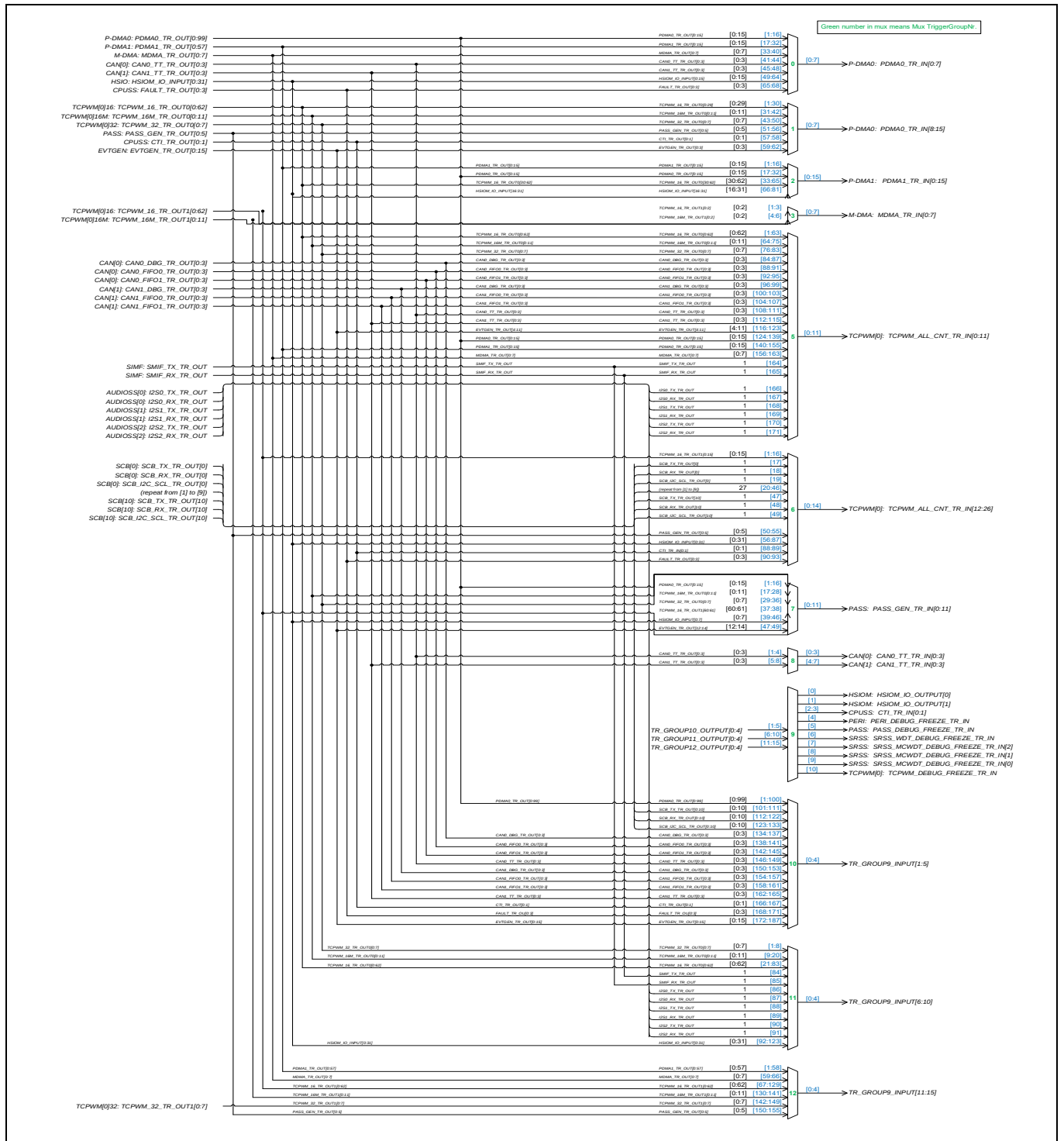
**Table 15-1 Core interrupt types**

| Interrupt | Source                          | Power mode | Description                    |
|-----------|---------------------------------|------------|--------------------------------|
| 0         | CPUIntIdx0_IRQn <sup>[33]</sup> | DeepSleep  | CPU User Interrupt #0          |
| 1         | CPUIntIdx1_IRQn <sup>[33]</sup> | DeepSleep  | CPU User Interrupt #1          |
| 2         | CPUIntIdx2_IRQn                 | DeepSleep  | CPU User Interrupt #2          |
| 3         | CPUIntIdx3_IRQn                 | DeepSleep  | CPU User Interrupt #3          |
| 4         | CPUIntIdx4_IRQn                 | DeepSleep  | CPU User Interrupt #4          |
| 5         | CPUIntIdx5_IRQn                 | DeepSleep  | CPU User Interrupt #5          |
| 6         | CPUIntIdx6_IRQn                 | DeepSleep  | CPU User Interrupt #6          |
| 7         | CPUIntIdx7_IRQn                 | DeepSleep  | CPU User Interrupt #7          |
| 8         | Internal0_IRQn                  | Active     | Internal Software Interrupt #0 |
| 9         | Internal1_IRQn                  | Active     | Internal Software Interrupt #1 |
| 10        | Internal2_IRQn                  | Active     | Internal Software Interrupt #2 |
| 11        | Internal3_IRQn                  | Active     | Internal Software Interrupt #3 |
| 12        | Internal4_IRQn                  | Active     | Internal Software Interrupt #4 |
| 13        | Internal5_IRQn                  | Active     | Internal Software Interrupt #5 |
| 14        | Internal6_IRQn                  | Active     | Internal Software Interrupt #6 |
| 15        | Internal7_IRQn                  | Active     | Internal Software Interrupt #7 |

**Note**

33. User interrupt cannot be used for CM0+ application, as it is used internally by system calls. Note, this does not impact CM7 application.

# 16 Trigger multiplexer



**Figure 16-1 Trigger multiplexer group** <sup>[34]</sup>

**Note**

34. This diagram shows only the TRIG\_LABEL; the final trigger formation is based on the formula  $\text{TRIG\_}{\{ \text{PREFIX}(\text{IN/OUT}) \}}_{\{ \text{MUX\_x} \}}_{\{ \text{TRIG\_LABEL} \}}$  and the information provided in [Table 17-1](#) and [Table 18-1](#).

Triggers group inputs

## 17 Triggers group inputs

**Table 17-1 Trigger inputs**

| Input                                                    | Trigger                 | Description                                                                 |
|----------------------------------------------------------|-------------------------|-----------------------------------------------------------------------------|
| <b>MUX Group 0:</b> P-DMA0 trigger multiplexer           |                         |                                                                             |
| 1:16 <sup>[35]</sup>                                     | PDMA0_TR_OUT[0:15]      | Allow P-DMA0 to chain to itself. Channels 0 - 15 are dedicated for chaining |
| 17:32                                                    | PDMA1_TR_OUT[0:15]      | Cross connections from P-DMA1 to P-DMA0, Channels 0-15 are used             |
| 33:40                                                    | MDMA_TR_OUT[0:7]        | Cross connections from M-DMA0 to P-DMA0                                     |
| 41:44                                                    | CAN0_TT_TR_OUT[0:3]     | CAN0 TT Sync Outputs                                                        |
| 45:48                                                    | CAN1_TT_TR_OUT[0:3]     | CAN1 TT Sync Outputs                                                        |
| 49:64                                                    | HSIOM_IO_INPUT[0:15]    | I/O Inputs                                                                  |
| 65:68                                                    | FAULT_TR_OUT[0:3]       | Fault events                                                                |
| <b>MUX Group 1:</b> TCPWM to P-DMA0 trigger multiplexer  |                         |                                                                             |
| 1:30                                                     | TCPWM_16_TR_OUT0[0:29]  | 16-bit TCPWM0 counters                                                      |
| 31:42                                                    | TCPWM_16M_TR_OUT0[0:11] | 16-bit Motor enhanced TCPWM0 counters                                       |
| 43:50                                                    | TCPWM_32_TR_OUT0[0:7]   | 32-bit TCPWM0 counters                                                      |
| 51:56                                                    | PASS_GEN_TR_OUT[0:5]    | PASS SAR events                                                             |
| 57:58                                                    | CTI_TR_OUT[0:1]         | Trace events                                                                |
| 59:62                                                    | EVTGEN_TR_OUT[0:3]      | Event generator triggers                                                    |
| <b>MUX Group 2:</b> P-DMA1 trigger multiplexer           |                         |                                                                             |
| 1:16                                                     | PDMA1_TR_OUT[0:15]      | Allow P-DMA1 to chain to itself. Channels 0–15 are dedicated for chaining   |
| 17:32                                                    | PDMA0_TR_OUT[0:15]      | Cross connections from P-DMA0 to P-DMA1, channels 0–15 are used             |
| 33:65                                                    | TCPWM_16_TR_OUT0[30:62] | 16-bit TCPWM0 counters                                                      |
| 66:81                                                    | HSIOM_IO_INPUT[16:31]   | I/O Inputs                                                                  |
| <b>MUX Group 3:</b> M-DMA0 trigger multiplexer           |                         |                                                                             |
| 1:3                                                      | TCPWM_16_TR_OUT1[0:2]   | 16-bit TCPWM0 counters                                                      |
| 4:6                                                      | TCPWM_16M_TR_OUT1[0:2]  | 16-bit Motor enhanced TCPWM0 counters                                       |
| <b>MUX Group 5:</b> TCPWM0 Loop back trigger multiplexer |                         |                                                                             |
| 1:63                                                     | TCPWM_16_TR_OUT0[0:62]  | 16-bit TCPWM0 counters                                                      |
| 64:75                                                    | TCPWM_16M_TR_OUT0[0:11] | 16-bit Motor enhanced TCPWM0 counters                                       |
| 76:83                                                    | TCPWM_32_TR_OUT0[0:7]   | 32-bit TCPWM0 counters                                                      |
| 84:87                                                    | CAN0_DBG_TR_OUT[0:3]    | CAN0 M-DMA0 events                                                          |
| 88:91                                                    | CAN0_FIFO0_TR_OUT[0:3]  | CAN0 FIFO0 events                                                           |
| 92:95                                                    | CAN0_FIFO1_TR_OUT[0:3]  | CAN0 FIFO1 events                                                           |
| 96:99                                                    | CAN1_DBG_TR_OUT[0:3]    | CAN1 M-DMA0 events                                                          |
| 100:103                                                  | CAN1_FIFO0_TR_OUT[0:3]  | CAN1 FIFO0 events                                                           |
| 104:107                                                  | CAN1_FIFO1_TR_OUT[0:3]  | CAN1 FIFO1 events                                                           |
| 108:111                                                  | CAN0_TT_TR_OUT[0:3]     | CAN0 TT Sync Outputs                                                        |
| 112:115                                                  | CAN1_TT_TR_OUT[0:3]     | CAN1 TT Sync Outputs                                                        |
| 116:123                                                  | EVTGEN_TR_OUT[4:11]     | Event generator triggers                                                    |
| 124:139                                                  | PDMA0_TR_OUT[0:15]      | P-DMA0 general-purpose triggers                                             |
| 140:155                                                  | PDMA1_TR_OUT[0:15]      | P-DMA1 general-purpose triggers                                             |
| 156:163                                                  | MDMA_TR_OUT[0:7]        | M-DMA0 events                                                               |
| 164                                                      | SMIF_TX_TR_OUT          | SMIF0 TX trigger                                                            |
| 165                                                      | SMIF_RX_TR_OUT          | SMIF0 RX trigger                                                            |
| 166                                                      | I2S0_TX_TR_OUT          | I <sup>2</sup> S0 TX trigger                                                |

**Note**

35. “x:y” depicts a range starting from ‘x’ through ‘y’.

Triggers group inputs

**Table 17-1**     **Trigger inputs** (continued)

| Input                                          | Trigger                | Description                    |
|------------------------------------------------|------------------------|--------------------------------|
| 167                                            | I2S0_RX_TR_OUT         | I <sup>2</sup> S0 RX trigger   |
| 168                                            | I2S1_TX_TR_OUT         | I <sup>2</sup> S1 TX trigger   |
| 169                                            | I2S1_RX_TR_OUT         | I <sup>2</sup> S1 RX trigger   |
| 170                                            | I2S2_TX_TR_OUT         | I <sup>2</sup> S2 TX trigger   |
| 171                                            | I2S2_RX_TR_OUT         | I <sup>2</sup> S2 RX trigger   |
| <b>MUX Group 6: TCPWM0 trigger Multiplexer</b> |                        |                                |
| 1:16                                           | TCPWM_16_TR_OUT1[0:15] | 16-bit TCPWM0 counters         |
| 17                                             | SCB_TX_TR_OUT[0]       | SCB0 TX trigger                |
| 18                                             | SCB_RX_TR_OUT[0]       | SCB0 RX trigger                |
| 19                                             | SCB_I2C_SCL_TR_OUT[0]  | SCB0 I <sup>2</sup> C trigger  |
| 20                                             | SCB_TX_TR_OUT[1]       | SCB1 TX trigger                |
| 21                                             | SCB_RX_TR_OUT[1]       | SCB1 RX trigger                |
| 22                                             | SCB_I2C_SCL_TR_OUT[1]  | SCB1 I <sup>2</sup> C trigger  |
| 23                                             | SCB_TX_TR_OUT[2]       | SCB2 TX trigger                |
| 24                                             | SCB_RX_TR_OUT[2]       | SCB2 RX trigger                |
| 25                                             | SCB_I2C_SCL_TR_OUT[2]  | SCB2 I <sup>2</sup> C trigger  |
| 26                                             | SCB_TX_TR_OUT[3]       | SCB3 TX trigger                |
| 27                                             | SCB_RX_TR_OUT[3]       | SCB3 RX trigger                |
| 28                                             | SCB_I2C_SCL_TR_OUT[3]  | SCB3 I <sup>2</sup> C trigger  |
| 29                                             | SCB_TX_TR_OUT[4]       | SCB4 TX trigger                |
| 30                                             | SCB_RX_TR_OUT[4]       | SCB4 RX trigger                |
| 31                                             | SCB_I2C_SCL_TR_OUT[4]  | SCB4 I <sup>2</sup> C trigger  |
| 32                                             | SCB_TX_TR_OUT[5]       | SCB5 TX trigger                |
| 33                                             | SCB_RX_TR_OUT[5]       | SCB5 RX trigger                |
| 34                                             | SCB_I2C_SCL_TR_OUT[5]  | SCB5 I <sup>2</sup> C trigger  |
| 35                                             | SCB_TX_TR_OUT[6]       | SCB6 TX trigger                |
| 36                                             | SCB_RX_TR_OUT[6]       | SCB6 RX trigger                |
| 37                                             | SCB_I2C_SCL_TR_OUT[6]  | SCB6 I <sup>2</sup> C trigger  |
| 38                                             | SCB_TX_TR_OUT[7]       | SCB7 TX trigger                |
| 39                                             | SCB_RX_TR_OUT[7]       | SCB7 RX trigger                |
| 40                                             | SCB_I2C_SCL_TR_OUT[7]  | SCB7 I <sup>2</sup> C trigger  |
| 41                                             | SCB_TX_TR_OUT[8]       | SCB8 TX trigger                |
| 42                                             | SCB_RX_TR_OUT[8]       | SCB8 RX trigger                |
| 43                                             | SCB_I2C_SCL_TR_OUT[8]  | SCB8 I <sup>2</sup> C trigger  |
| 44                                             | SCB_TX_TR_OUT[9]       | SCB9 TX trigger                |
| 45                                             | SCB_RX_TR_OUT[9]       | SCB9 RX trigger                |
| 46                                             | SCB_I2C_SCL_TR_OUT[9]  | SCB9 I <sup>2</sup> C trigger  |
| 47                                             | SCB_TX_TR_OUT[10]      | SCB10 TX trigger               |
| 48                                             | SCB_RX_TR_OUT[10]      | SCB10 RX trigger               |
| 49                                             | SCB_I2C_SCL_TR_OUT[10] | SCB10 I <sup>2</sup> C trigger |
| 50:55                                          | PASS_GEN_TR_OUT[0:5]   | PASS SAR events                |
| 56:87                                          | HSIOM_IO_INPUT[0:31]   | I/O Inputs                     |
| 88:89                                          | CTI_TR_IN[0:1]         | Trace events                   |
| 90:93                                          | FAULT_TR_OUT[0:3]      | Fault events                   |

Triggers group inputs

**Table 17-1 Trigger inputs** (continued)

| Input                                        | Trigger                  | Description                                |
|----------------------------------------------|--------------------------|--------------------------------------------|
| <b>MUX Group 7: PASS trigger multiplexer</b> |                          |                                            |
| 1:16                                         | PDMA0_TR_OUT[0:15]       | General-purpose P-DMA0 triggers            |
| 17:28                                        | TCPWM_16M_TR_OUT0[0:11]  | 16-bit Motor enhanced TCPWM0 counters      |
| 29:36                                        | TCPWM_32_TR_OUT0[0:7]    | 32-bit TCPWM0 counters                     |
| 37:38                                        | TCPWM_16_TR_OUT1[60:61]  | 16-bit TCPWM0 counters                     |
| 39:46                                        | HSIOM_IO_INPUT[0:7]      | I/O Inputs                                 |
| 47:49                                        | EVTGEN_TR_OUT[12:14]     | Event generator triggers                   |
| <b>MUX Group 8: CAN TT Sync</b>              |                          |                                            |
| 1:4                                          | CAN0_TT_TR_OUT[0:3]      | CAN0 TT Sync Outputs                       |
| 5:8                                          | CAN1_TT_TR_OUT[0:3]      | CAN1 TT Sync Outputs                       |
| <b>MUX Group 9: Debug multiplexer</b>        |                          |                                            |
| 1:5                                          | TR_GROUP10_OUTPUT[0:4]   | Output from debug reduction multiplexer #1 |
| 6:10                                         | TR_GROUP11_OUTPUT[0:4]   | Output from debug reduction multiplexer #2 |
| 11:15                                        | TR_GROUP12_OUTPUT[0:4]   | Output from debug reduction multiplexer #3 |
| <b>MUX Group 10: Debug Reduction #1</b>      |                          |                                            |
| 1:100                                        | PDMA0_TR_OUT[0:99]       | General-purpose P-DMA0 triggers            |
| 101:111                                      | SCB_TX_TR_OUT[0:10]      | SCB TX triggers                            |
| 112:122                                      | SCB_RX_TR_OUT[0:10]      | SCB RX triggers                            |
| 123:133                                      | SCB_I2C_SCL_TR_OUT[0:10] | SCB I <sup>2</sup> C triggers              |
| 134:137                                      | CAN0_DBG_TR_OUT[0:3]     | CAN0 DMA                                   |
| 138:141                                      | CAN0_FIFO0_TR_OUT[0:3]   | CAN0 FIFO0                                 |
| 142:145                                      | CAN0_FIFO1_TR_OUT[0:3]   | CAN0 FIFO1                                 |
| 146:149                                      | CAN0_TT_TR_OUT[0:3]      | CAN0 TT Sync Outputs                       |
| 150:153                                      | CAN1_DBG_TR_OUT[0:3]     | CAN1 DMA                                   |
| 154:157                                      | CAN1_FIFO0_TR_OUT[0:3]   | CAN1 FIFO0                                 |
| 158:161                                      | CAN1_FIFO1_TR_OUT[0:3]   | CAN1 FIFO1                                 |
| 162:165                                      | CAN1_TT_TR_OUT[0:3]      | CAN1 TT Sync Outputs                       |
| 166:167                                      | CTI_TR_OUT[0:1]          | Trace events                               |
| 168:171                                      | FAULT_TR_OUT[0:3]        | Fault events                               |
| 172:187                                      | EVTGEN_TR_OUT[0:15]      | EVTGEN Triggers                            |
| <b>MUX Group 11: Debug Reduction #2</b>      |                          |                                            |
| 1:8                                          | TCPWM_32_TR_OUT0[0:7]    | 32-bit TCPWM0 counters                     |
| 9:20                                         | TCPWM_16M_TR_OUT0[0:11]  | 16-bit Motor enhanced TCPWM0 counters      |
| 21:83                                        | TCPWM_16_TR_OUT0[0:62]   | 16-bit TCPWM0 counters                     |
| 84                                           | SMIF_TX_TR_OUT           | SMIF TX trigger                            |
| 85                                           | SMIF_RX_TR_OUT           | SMIF RX trigger                            |
| 86                                           | I2S0_TX_TR_OUT           | I <sup>2</sup> S0 TX trigger               |
| 87                                           | I2S0_RX_TR_OUT           | I <sup>2</sup> S0 RX trigger               |
| 88                                           | I2S1_TX_TR_OUT           | I <sup>2</sup> S1 TX trigger               |
| 89                                           | I2S1_RX_TR_OUT           | I <sup>2</sup> S1 RX trigger               |
| 90                                           | I2S2_TX_TR_OUT           | I <sup>2</sup> S2 TX trigger               |
| 91                                           | I2S2_RX_TR_OUT           | I <sup>2</sup> S2 RX trigger               |
| 92:123                                       | HSIOM_IO_INPUT[0:31]     | I/O inputs                                 |
| <b>MUX Group 12: Debug Reduction #3</b>      |                          |                                            |
| 1:58                                         | PDMA1_TR_OUT[0:57]       | General-purpose P-DMA1 triggers            |

Triggers group inputs

**Table 17-1**    **Trigger inputs** *(continued)*

| Input   | Trigger                 | Description                           |
|---------|-------------------------|---------------------------------------|
| 59:66   | MDMA_TR_OUT[0:7]        | M-DMA0 triggers                       |
| 67:129  | TCPWM_16_TR_OUT1[0:62]  | 16-bit TCPWM0 counters                |
| 130:141 | TCPWM_16M_TR_OUT1[0:11] | 16-bit Motor enhanced TCPWM0 counters |
| 142:149 | TCPWM_32_TR_OUT1[0:7]   | 32-bit TCPWM0 counters                |
| 150:155 | PASS_GEN_TR_OUT[0:5]    | PASS SAR events                       |

Triggers group outputs

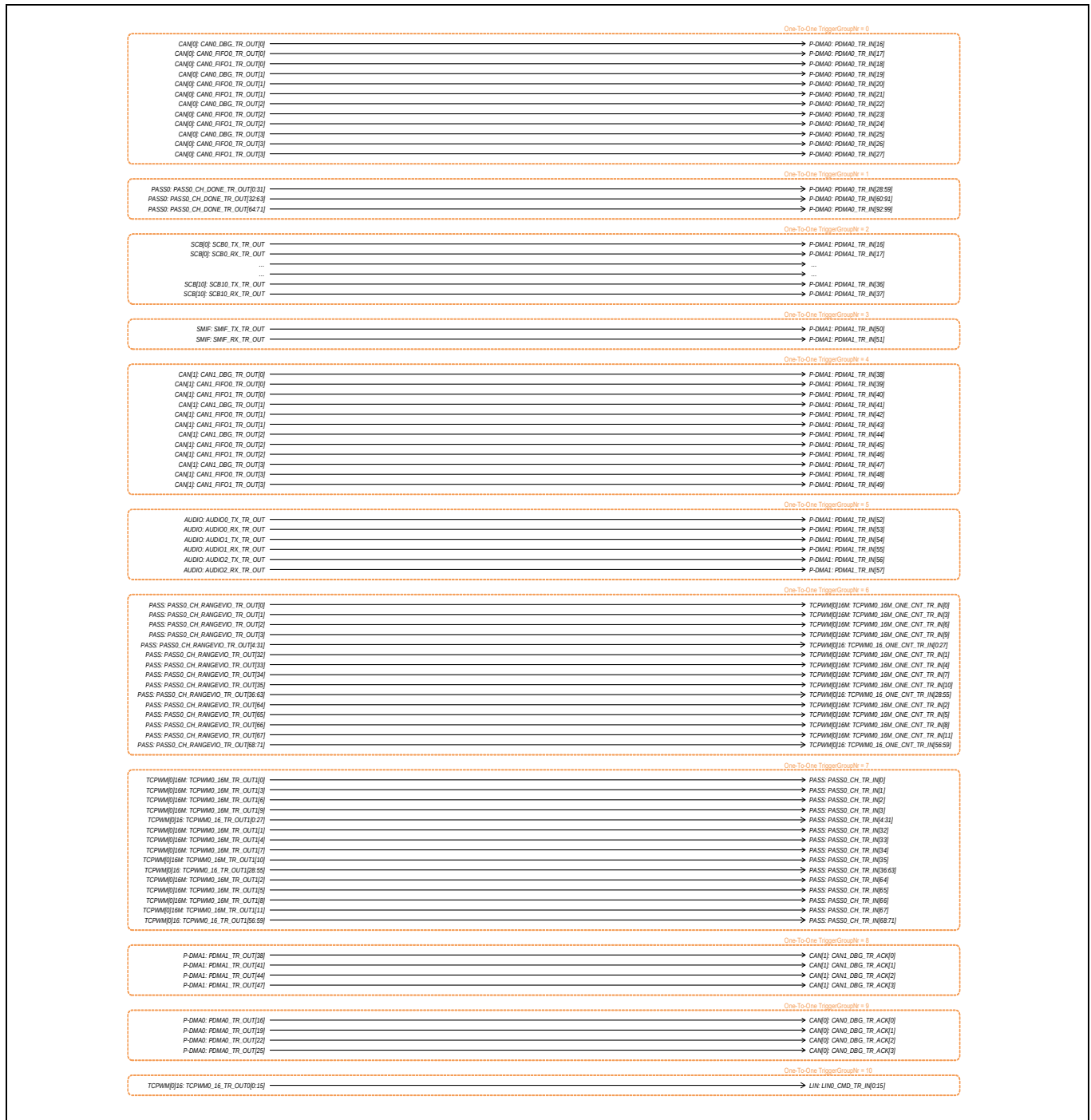
## 18 Triggers group outputs

**Table 18-1 Trigger outputs**

| Output                                                  | Trigger                          | Description                       |
|---------------------------------------------------------|----------------------------------|-----------------------------------|
| <b>MUX Group 0:</b> P-DMA0 trigger multiplexer          |                                  |                                   |
| 0:7                                                     | PDMA0_TR_IN[0:7]                 | Triggers to P-DMA0[0:7]           |
| <b>MUX Group 1:</b> TCPWM to P-DMA0 trigger multiplexer |                                  |                                   |
| 0:7                                                     | PDMA0_TR_IN[8:15]                | Triggers to P-DMA0[8:15]          |
| <b>MUX Group 2:</b> P-DMA1 trigger multiplexer          |                                  |                                   |
| 0:15                                                    | PDMA1_TR_IN[0:15]                | Triggers to P-DMA1                |
| <b>MUX Group 3:</b> M-DMA0 trigger multiplexer          |                                  |                                   |
| 0:7                                                     | MDMA_TR_IN[0:7]                  | Triggers to M-DMA0                |
| <b>MUX Group 5:</b> TCPWM0 loop-back multiplexer        |                                  |                                   |
| 0:11                                                    | TCPWM_ALL_CNT_TR_IN[0:11]        | Triggers to TCPWM0                |
| <b>MUX Group 6:</b> TCPWM0 Trigger Multiplexer          |                                  |                                   |
| 0:14                                                    | TCPWM_ALL_CNT_TR_IN[12:26]       | Triggers to TCPWM0                |
| <b>MUX Group 7:</b> PASS trigger multiplexer            |                                  |                                   |
| 0:11                                                    | PASS_GEN_TR_IN[0:11]             | Triggers to SAR ADCs              |
| <b>MUX Group 8:</b> CAN TT Sync                         |                                  |                                   |
| 0:3                                                     | CAN0_TT_TR_IN[0:3]               | CAN0 TT Sync Inputs               |
| 4:7                                                     | CAN1_TT_TR_IN[0:3]               | CAN1 TT Sync Inputs               |
| <b>MUX Group 9:</b> Debug multiplexer                   |                                  |                                   |
| 0                                                       | HSIOM_IO_OUTPUT[0]               | To HSIOM as an output             |
| 1                                                       | HSIOM_IO_OUTPUT[1]               | To HSIOM as an output             |
| 2:3                                                     | CTI_TR_IN[0:1]                   | To the Cross Trigger system       |
| 4                                                       | PERI_DEBUG_FREEZE_TR_IN          | Signal to Freeze PERI operation   |
| 5                                                       | PASS_DEBUG_FREEZE_TR_IN          | Signal to Freeze PASS operation   |
| 6                                                       | SRSS_WDT_DEBUG_FREEZE_TR_IN      | Signal to Freeze WDT operation    |
| 7                                                       | SRSS_MCWDT_DEBUG_FREEZE_TR_IN[2] | Signal to Freeze MCWDT2 operation |
| 8                                                       | SRSS_MCWDT_DEBUG_FREEZE_TR_IN[1] | Signal to Freeze MCWDT1 operation |
| 9                                                       | SRSS_MCWDT_DEBUG_FREEZE_TR_IN[0] | Signal to Freeze MCWDT0 operation |
| 10                                                      | TCPWM_DEBUG_FREEZE_TR_IN         | Signal to Freeze TCPWM0 operation |
| <b>MUX Group 10:</b> Debug Reduction #1                 |                                  |                                   |
| 0:4                                                     | TR_GROUP9_INPUT[1:5]             | To main debug multiplexer         |
| <b>MUX Group 11:</b> Debug Reduction #2                 |                                  |                                   |
| 0:4                                                     | TR_GROUP9_INPUT[6:10]            | To main debug multiplexer         |
| <b>MUX Group 12:</b> Debug Reduction #3                 |                                  |                                   |
| 0:4                                                     | TR_GROUP9_INPUT[11:15]           | To main debug multiplexer         |

Triggers one-to-one

## 19 Triggers one-to-one



**Figure 19-1 Triggers one-to-one**<sup>[36]</sup>

**Note**

36. The diagram shows only the TRIG\_LABEL; the final trigger formation is based on the formula TRIG\_{PREFIX(IN\_1TO1/OUT\_1-TO1)}\_{x}\_{TRIG\_LABEL} and the information provided in [Table 19-1](#).

Triggers one-to-one

**Table 19-1 One-to-one triggers**

| Input                                                  | Trigger in                  | Trigger out        | Description                               |
|--------------------------------------------------------|-----------------------------|--------------------|-------------------------------------------|
| <b>MUX Group 0: CAN0 to P-DMA0 Triggers</b>            |                             |                    |                                           |
| 0                                                      | CAN0_DBG_TR_OUT[0]          | PDMA0_TR_IN[16]    | CAN0, Channel #0 P-DMA0 trigger           |
| 1                                                      | CAN0_FIFO0_TR_OUT[0]        | PDMA0_TR_IN[17]    | CAN0, Channel #0 FIFO0 trigger            |
| 2                                                      | CAN0_FIFO1_TR_OUT[0]        | PDMA0_TR_IN[18]    | CAN0, Channel #0 FIFO1 trigger            |
| 3                                                      | CAN0_DBG_TR_OUT[1]          | PDMA0_TR_IN[19]    | CAN0, Channel #1 P-DMA0 trigger           |
| 4                                                      | CAN0_FIFO0_TR_OUT[1]        | PDMA0_TR_IN[20]    | CAN0, Channel #1 FIFO0 trigger            |
| 5                                                      | CAN0_FIFO1_TR_OUT[1]        | PDMA0_TR_IN[21]    | CAN0, Channel #1 FIFO1 trigger            |
| 6                                                      | CAN0_DBG_TR_OUT[2]          | PDMA0_TR_IN[22]    | CAN0, Channel #2 P-DMA0 trigger           |
| 7                                                      | CAN0_FIFO0_TR_OUT[2]        | PDMA0_TR_IN[23]    | CAN0, Channel #2 FIFO0 trigger            |
| 8                                                      | CAN0_FIFO1_TR_OUT[2]        | PDMA0_TR_IN[24]    | CAN0, Channel #2 FIFO1 trigger            |
| 9                                                      | CAN0_DBG_TR_OUT[3]          | PDMA0_TR_IN[25]    | CAN0, Channel #3 P-DMA0 trigger           |
| 10                                                     | CAN0_FIFO0_TR_OUT[3]        | PDMA0_TR_IN[26]    | CAN0, Channel #3 FIFO0 trigger            |
| 11                                                     | CAN0_FIFO1_TR_OUT[3]        | PDMA0_TR_IN[27]    | CAN0, Channel #3 FIFO1 trigger            |
| <b>MUX Group 1: PASS SARx to P-DMA0 direct connect</b> |                             |                    |                                           |
| 0:31                                                   | PASS0_CH_DONE_TR_OUT[0:31]  | PDMA0_TR_IN[28:59] | PASS SAR0 [0:31] to P-DMA0 direct connect |
| 32:63                                                  | PASS0_CH_DONE_TR_OUT[32:63] | PDMA0_TR_IN[60:91] | PASS SAR1 [0:31] to P-DMA0 direct connect |
| 64:71                                                  | PASS0_CH_DONE_TR_OUT[64:71] | PDMA0_TR_IN[92:99] | PASS SAR2 [0:7] to P-DMA0 direct connect  |
| <b>MUX Group 2: SCBx to P-DMA1 Triggers</b>            |                             |                    |                                           |
| 0                                                      | SCB0_TX_TR_OUT              | PDMA1_TR_IN[16]    | SCB0 to P-DMA1 Trigger                    |
| 1                                                      | SCB0_RX_TR_OUT              | PDMA1_TR_IN[17]    | SCB0 to P-DMA1 Trigger                    |
| 2                                                      | SCB1_TX_TR_OUT              | PDMA1_TR_IN[18]    | SCB1 to P-DMA1 Trigger                    |
| 3                                                      | SCB1_RX_TR_OUT              | PDMA1_TR_IN[19]    | SCB1 to P-DMA1 Trigger                    |
| 4                                                      | SCB2_TX_TR_OUT              | PDMA1_TR_IN[20]    | SCB2 to P-DMA1 Trigger                    |
| 5                                                      | SCB2_RX_TR_OUT              | PDMA1_TR_IN[21]    | SCB2 to P-DMA1 Trigger                    |
| 6                                                      | SCB3_TX_TR_OUT              | PDMA1_TR_IN[22]    | SCB3 to P-DMA1 Trigger                    |
| 7                                                      | SCB3_RX_TR_OUT              | PDMA1_TR_IN[23]    | SCB3 to P-DMA1 Trigger                    |
| 8                                                      | SCB4_TX_TR_OUT              | PDMA1_TR_IN[24]    | SCB4 to P-DMA1 Trigger                    |
| 9                                                      | SCB4_RX_TR_OUT              | PDMA1_TR_IN[25]    | SCB4 to P-DMA1 Trigger                    |
| 10                                                     | SCB5_TX_TR_OUT              | PDMA1_TR_IN[26]    | SCB5 to P-DMA1 Trigger                    |
| 11                                                     | SCB5_RX_TR_OUT              | PDMA1_TR_IN[27]    | SCB5 to P-DMA1 Trigger                    |
| 12                                                     | SCB6_TX_TR_OUT              | PDMA1_TR_IN[28]    | SCB6 to P-DMA1 Trigger                    |
| 13                                                     | SCB6_RX_TR_OUT              | PDMA1_TR_IN[29]    | SCB6 to P-DMA1 Trigger                    |
| 14                                                     | SCB7_TX_TR_OUT              | PDMA1_TR_IN[30]    | SCB7 to P-DMA1 Trigger                    |
| 15                                                     | SCB7_RX_TR_OUT              | PDMA1_TR_IN[31]    | SCB7 to P-DMA1 Trigger                    |
| 16                                                     | SCB8_TX_TR_OUT              | PDMA1_TR_IN[32]    | SCB8 to P-DMA1 Trigger                    |
| 17                                                     | SCB8_RX_TR_OUT              | PDMA1_TR_IN[33]    | SCB8 to P-DMA1 Trigger                    |
| 18                                                     | SCB9_TX_TR_OUT              | PDMA1_TR_IN[34]    | SCB9 to P-DMA1 Trigger                    |
| 19                                                     | SCB9_RX_TR_OUT              | PDMA1_TR_IN[35]    | SCB9 to P-DMA1 Trigger                    |
| 20                                                     | SCB10_TX_TR_OUT             | PDMA1_TR_IN[36]    | SCB10 to P-DMA1 Trigger                   |
| 21                                                     | SCB10_RX_TR_OUT             | PDMA1_TR_IN[37]    | SCB10 to P-DMA1 Trigger                   |
| <b>MUX Group 3: SMIF0 to P-DMA1 Triggers</b>           |                             |                    |                                           |
| 0                                                      | SMIF_TX_TR_OUT              | PDMA1_TR_IN[50]    | SMIF0 to P-DMA1 Trigger                   |
| 1                                                      | SMIF_RX_TR_OUT              | PDMA1_TR_IN[51]    | SMIF0 to P-DMA1 Trigger                   |
| <b>MUX Group 4: CAN1 to P-DMA1 triggers</b>            |                             |                    |                                           |
| 0                                                      | CAN1_DBG_TR_OUT[0]          | PDMA1_TR_IN[38]    | CAN1 Channel #0 P-DMA1 trigger            |
| 1                                                      | CAN1_FIFO0_TR_OUT[0]        | PDMA1_TR_IN[39]    | CAN1 Channel #0 FIFO0 trigger             |
| 2                                                      | CAN1_FIFO1_TR_OUT[0]        | PDMA1_TR_IN[40]    | CAN1 Channel #0 FIFO1 trigger             |
| 3                                                      | CAN1_DBG_TR_OUT[1]          | PDMA1_TR_IN[41]    | CAN1 Channel #1 P-DMA1 trigger            |
| 4                                                      | CAN1_FIFO0_TR_OUT[1]        | PDMA1_TR_IN[42]    | CAN1 Channel #1 FIFO0 trigger             |

Triggers one-to-one

**Table 19-1 One-to-one triggers (continued)**

| Input                                                  | Trigger in                   | Trigger out                  | Description                                                                         |
|--------------------------------------------------------|------------------------------|------------------------------|-------------------------------------------------------------------------------------|
| 5                                                      | CAN1_FIFO1_TR_OUT[1]         | PDMA1_TR_IN[43]              | CAN1 Channel #1 FIFO1 trigger                                                       |
| 6                                                      | CAN1_DBG_TR_OUT[2]           | PDMA1_TR_IN[44]              | CAN1 Channel #2 P-DMA1 trigger                                                      |
| 7                                                      | CAN1_FIFO0_TR_OUT[2]         | PDMA1_TR_IN[45]              | CAN1 Channel #2 FIFO0 trigger                                                       |
| 8                                                      | CAN1_FIFO1_TR_OUT[2]         | PDMA1_TR_IN[46]              | CAN1 Channel #2 FIFO1 trigger                                                       |
| 9                                                      | CAN1_DBG_TR_OUT[3]           | PDMA1_TR_IN[47]              | CAN1 Channel #3 P-DMA1 trigger                                                      |
| 10                                                     | CAN1_FIFO0_TR_OUT[3]         | PDMA1_TR_IN[48]              | CAN1 Channel #3 FIFO0 trigger                                                       |
| 11                                                     | CAN1_FIFO1_TR_OUT[3]         | PDMA1_TR_IN[49]              | CAN1 Channel #3 FIFO1 trigger                                                       |
| <b>MUX Group 5: I<sup>2</sup>Sx to P-DMA1 Triggers</b> |                              |                              |                                                                                     |
| 0                                                      | AUDIO0_TX_TR_OUT             | PDMA1_TR_IN[52]              | I <sup>2</sup> S0 TX to P-DMA1 trigger                                              |
| 1                                                      | AUDIO0_RX_TR_OUT             | PDMA1_TR_IN[53]              | I <sup>2</sup> S0 RX to P-DMA1 trigger                                              |
| 2                                                      | AUDIO1_TX_TR_OUT             | PDMA1_TR_IN[54]              | I <sup>2</sup> S1 TX to P-DMA1 trigger                                              |
| 3                                                      | AUDIO1_RX_TR_OUT             | PDMA1_TR_IN[55]              | I <sup>2</sup> S1 RX to P-DMA1 trigger                                              |
| 4                                                      | AUDIO2_TX_TR_OUT             | PDMA1_TR_IN[56]              | I <sup>2</sup> S2 TX to P-DMA1 trigger                                              |
| 5                                                      | AUDIO2_RX_TR_OUT             | PDMA1_TR_IN[57]              | I <sup>2</sup> S2 RX to P-DMA1 trigger                                              |
| <b>MUX Group 6: PASS SARx to TCPWM0 direct connect</b> |                              |                              |                                                                                     |
| 0                                                      | PASS0_CH_RANGEVIO_TR_OUT[0]  | TCPWM0_16M_ONE_CNT_TR_IN[0]  | SAR0 ch#0 <sup>[37]</sup> , range violation to TCPWM0 Group #1 Counter #00 trig = 2 |
| 1                                                      | PASS0_CH_RANGEVIO_TR_OUT[1]  | TCPWM0_16M_ONE_CNT_TR_IN[3]  | SAR0 ch#1, range violation to TCPWM0 Group #1 Counter #03 trig = 2                  |
| 2                                                      | PASS0_CH_RANGEVIO_TR_OUT[2]  | TCPWM0_16M_ONE_CNT_TR_IN[6]  | SAR0 ch#2, range violation to TCPWM0 Group #1 Counter #06 trig = 2                  |
| 3                                                      | PASS0_CH_RANGEVIO_TR_OUT[3]  | TCPWM0_16M_ONE_CNT_TR_IN[9]  | SAR0 ch#3, range violation to TCPWM0 Group #1 Counter #09 trig = 2                  |
| 4                                                      | PASS0_CH_RANGEVIO_TR_OUT[4]  | TCPWM0_16M_ONE_CNT_TR_IN[0]  | SAR0 ch#4, range violation to TCPWM0 Group #0 Counter #00 trig = 2                  |
| 5                                                      | PASS0_CH_RANGEVIO_TR_OUT[5]  | TCPWM0_16M_ONE_CNT_TR_IN[1]  | SAR0 ch#5, range violation to TCPWM0 Group #0 Counter #01 trig = 2                  |
| 6                                                      | PASS0_CH_RANGEVIO_TR_OUT[6]  | TCPWM0_16M_ONE_CNT_TR_IN[2]  | SAR0 ch#6, range violation to TCPWM0 Group #0 Counter #02 trig = 2                  |
| 7                                                      | PASS0_CH_RANGEVIO_TR_OUT[7]  | TCPWM0_16M_ONE_CNT_TR_IN[3]  | SAR0 ch#7, range violation to TCPWM0 Group #0 Counter #03 trig = 2                  |
| 8                                                      | PASS0_CH_RANGEVIO_TR_OUT[8]  | TCPWM0_16M_ONE_CNT_TR_IN[4]  | SAR0 ch#8, range violation to TCPWM0 Group #0 Counter #04 trig = 2                  |
| 9                                                      | PASS0_CH_RANGEVIO_TR_OUT[9]  | TCPWM0_16M_ONE_CNT_TR_IN[5]  | SAR0 ch#9, range violation to TCPWM0 Group #0 Counter #05 trig = 2                  |
| 10                                                     | PASS0_CH_RANGEVIO_TR_OUT[10] | TCPWM0_16M_ONE_CNT_TR_IN[6]  | SAR0 ch#10, range violation to TCPWM0 Group #0 Counter #06 trig = 2                 |
| 11                                                     | PASS0_CH_RANGEVIO_TR_OUT[11] | TCPWM0_16M_ONE_CNT_TR_IN[7]  | SAR0 ch#11, range violation to TCPWM0 Group #0 Counter #07 trig = 2                 |
| 12                                                     | PASS0_CH_RANGEVIO_TR_OUT[12] | TCPWM0_16M_ONE_CNT_TR_IN[8]  | SAR0 ch#12, range violation to TCPWM0 Group #0 Counter #08 trig = 2                 |
| 13                                                     | PASS0_CH_RANGEVIO_TR_OUT[13] | TCPWM0_16M_ONE_CNT_TR_IN[9]  | SAR0 ch#13, range violation to TCPWM0 Group #0 Counter #09 trig = 2                 |
| 14                                                     | PASS0_CH_RANGEVIO_TR_OUT[14] | TCPWM0_16M_ONE_CNT_TR_IN[10] | SAR0 ch#14, range violation to TCPWM0 Group #0 Counter #10 trig = 2                 |
| 15                                                     | PASS0_CH_RANGEVIO_TR_OUT[15] | TCPWM0_16M_ONE_CNT_TR_IN[11] | SAR0 ch#15, range violation to TCPWM0 Group #0 Counter #11 trig = 2                 |
| 16                                                     | PASS0_CH_RANGEVIO_TR_OUT[16] | TCPWM0_16M_ONE_CNT_TR_IN[12] | SAR0 ch#16, range violation to TCPWM0 Group #0 Counter #12 trig = 2                 |
| 17                                                     | PASS0_CH_RANGEVIO_TR_OUT[17] | TCPWM0_16M_ONE_CNT_TR_IN[13] | SAR0 ch#17, range violation to TCPWM0 Group #0 Counter #13 trig = 2                 |
| 18                                                     | PASS0_CH_RANGEVIO_TR_OUT[18] | TCPWM0_16M_ONE_CNT_TR_IN[14] | SAR0 ch#18, range violation to TCPWM0 Group #0 Counter #14 trig = 2                 |
| 19                                                     | PASS0_CH_RANGEVIO_TR_OUT[19] | TCPWM0_16M_ONE_CNT_TR_IN[15] | SAR0 ch#19, range violation to TCPWM0 Group #0 Counter #15 trig = 2                 |
| 20                                                     | PASS0_CH_RANGEVIO_TR_OUT[20] | TCPWM0_16M_ONE_CNT_TR_IN[16] | SAR0 ch#20, range violation to TCPWM0 Group #0 Counter #16 trig = 2                 |
| 21                                                     | PASS0_CH_RANGEVIO_TR_OUT[21] | TCPWM0_16M_ONE_CNT_TR_IN[17] | SAR0 ch#21, range violation to TCPWM0 Group #0 Counter #17 trig = 2                 |

**Note**

37. Each logical channel of SAR ADC[x] can be connected to any of the SAR ADC[x]\_y external pin. (x = 0, or 1, or 2 and y=0 to 31).

Triggers one-to-one

**Table 19-1 One-to-one triggers (continued)**

| Input | Trigger in                   | Trigger out                  | Description                                                         |
|-------|------------------------------|------------------------------|---------------------------------------------------------------------|
| 22    | PASS0_CH_RANGEVIO_TR_OUT[22] | TCPWM0_16_ONE_CNT_TR_IN[18]  | SAR0 ch#22, range violation to TCPWM0 Group #0 Counter #18 trig = 2 |
| 23    | PASS0_CH_RANGEVIO_TR_OUT[23] | TCPWM0_16_ONE_CNT_TR_IN[19]  | SAR0 ch#23, range violation to TCPWM0 Group #0 Counter #19 trig = 2 |
| 24    | PASS0_CH_RANGEVIO_TR_OUT[24] | TCPWM0_16_ONE_CNT_TR_IN[20]  | SAR0 ch#24, range violation to TCPWM0 Group #0 Counter #20 trig = 2 |
| 25    | PASS0_CH_RANGEVIO_TR_OUT[25] | TCPWM0_16_ONE_CNT_TR_IN[21]  | SAR0 ch#25, range violation to TCPWM0 Group #0 Counter #21 trig = 2 |
| 26    | PASS0_CH_RANGEVIO_TR_OUT[26] | TCPWM0_16_ONE_CNT_TR_IN[22]  | SAR0 ch#26, range violation to TCPWM0 Group #0 Counter #22 trig = 2 |
| 27    | PASS0_CH_RANGEVIO_TR_OUT[27] | TCPWM0_16_ONE_CNT_TR_IN[23]  | SAR0 ch#27, range violation to TCPWM0 Group #0 Counter #23 trig = 2 |
| 28    | PASS0_CH_RANGEVIO_TR_OUT[28] | TCPWM0_16_ONE_CNT_TR_IN[24]  | SAR0 ch#28, range violation to TCPWM0 Group #0 Counter #24 trig = 2 |
| 29    | PASS0_CH_RANGEVIO_TR_OUT[29] | TCPWM0_16_ONE_CNT_TR_IN[25]  | SAR0 ch#29, range violation to TCPWM0 Group #0 Counter #25 trig = 2 |
| 30    | PASS0_CH_RANGEVIO_TR_OUT[30] | TCPWM0_16_ONE_CNT_TR_IN[26]  | SAR0 ch#30, range violation to TCPWM0 Group #0 Counter #26 trig = 2 |
| 31    | PASS0_CH_RANGEVIO_TR_OUT[31] | TCPWM0_16_ONE_CNT_TR_IN[27]  | SAR0 ch#31, range violation to TCPWM0 Group #0 Counter #27 trig = 2 |
| 32    | PASS0_CH_RANGEVIO_TR_OUT[32] | TCPWM0_16M_ONE_CNT_TR_IN[1]  | SAR1 ch#0, range violation to TCPWM0 Group #1 Counter #01 trig = 2  |
| 33    | PASS0_CH_RANGEVIO_TR_OUT[33] | TCPWM0_16M_ONE_CNT_TR_IN[4]  | SAR1 ch#1, range violation to TCPWM0 Group #1 Counter #04 trig = 2  |
| 34    | PASS0_CH_RANGEVIO_TR_OUT[34] | TCPWM0_16M_ONE_CNT_TR_IN[7]  | SAR1 ch#2, range violation to TCPWM0 Group #1 Counter #07 trig = 2  |
| 35    | PASS0_CH_RANGEVIO_TR_OUT[35] | TCPWM0_16M_ONE_CNT_TR_IN[10] | SAR1 ch#3, range violation to TCPWM0 Group #1 Counter #10 trig = 2  |
| 36    | PASS0_CH_RANGEVIO_TR_OUT[36] | TCPWM0_16_ONE_CNT_TR_IN[28]  | SAR1 ch#4, range violation to TCPWM0 Group #0 Counter #28 trig = 2  |
| 37    | PASS0_CH_RANGEVIO_TR_OUT[37] | TCPWM0_16_ONE_CNT_TR_IN[29]  | SAR1 ch#5, range violation to TCPWM0 Group #0 Counter #29 trig = 2  |
| 38    | PASS0_CH_RANGEVIO_TR_OUT[38] | TCPWM0_16_ONE_CNT_TR_IN[30]  | SAR1 ch#6, range violation to TCPWM0 Group #0 Counter #30 trig = 2  |
| 39    | PASS0_CH_RANGEVIO_TR_OUT[39] | TCPWM0_16_ONE_CNT_TR_IN[31]  | SAR1 ch#7, range violation to TCPWM0 Group #0 Counter #31 trig = 2  |
| 40    | PASS0_CH_RANGEVIO_TR_OUT[40] | TCPWM0_16_ONE_CNT_TR_IN[32]  | SAR1 ch#8, range violation to TCPWM0 Group #0 Counter #32 trig = 2  |
| 41    | PASS0_CH_RANGEVIO_TR_OUT[41] | TCPWM0_16_ONE_CNT_TR_IN[33]  | SAR1 ch#9, range violation to TCPWM0 Group #0 Counter #33 trig = 2  |
| 42    | PASS0_CH_RANGEVIO_TR_OUT[42] | TCPWM0_16_ONE_CNT_TR_IN[34]  | SAR1 ch#10, range violation to TCPWM0 Group #0 Counter #34 trig = 2 |
| 43    | PASS0_CH_RANGEVIO_TR_OUT[43] | TCPWM0_16_ONE_CNT_TR_IN[35]  | SAR1 ch#11, range violation to TCPWM0 Group #0 Counter #35 trig = 2 |
| 44    | PASS0_CH_RANGEVIO_TR_OUT[44] | TCPWM0_16_ONE_CNT_TR_IN[36]  | SAR1 ch#12, range violation to TCPWM0 Group #0 Counter #36 trig = 2 |
| 45    | PASS0_CH_RANGEVIO_TR_OUT[45] | TCPWM0_16_ONE_CNT_TR_IN[37]  | SAR1 ch#13, range violation to TCPWM0 Group #0 Counter #37 trig = 2 |
| 46    | PASS0_CH_RANGEVIO_TR_OUT[46] | TCPWM0_16_ONE_CNT_TR_IN[38]  | SAR1 ch#14, range violation to TCPWM0 Group #0 Counter #38 trig = 2 |
| 47    | PASS0_CH_RANGEVIO_TR_OUT[47] | TCPWM0_16_ONE_CNT_TR_IN[39]  | SAR1 ch#15, range violation to TCPWM0 Group #0 Counter #39 trig = 2 |
| 48    | PASS0_CH_RANGEVIO_TR_OUT[48] | TCPWM0_16_ONE_CNT_TR_IN[40]  | SAR1 ch#16, range violation to TCPWM0 Group #0 Counter #40 trig = 2 |
| 49    | PASS0_CH_RANGEVIO_TR_OUT[49] | TCPWM0_16_ONE_CNT_TR_IN[41]  | SAR1 ch#17, range violation to TCPWM0 Group #0 Counter #41 trig = 2 |
| 50    | PASS0_CH_RANGEVIO_TR_OUT[50] | TCPWM0_16_ONE_CNT_TR_IN[42]  | SAR1 ch#18, range violation to TCPWM0 Group #0 Counter #42 trig = 2 |
| 51    | PASS0_CH_RANGEVIO_TR_OUT[51] | TCPWM0_16_ONE_CNT_TR_IN[43]  | SAR1 ch#19, range violation to TCPWM0 Group #0 Counter #43 trig = 2 |
| 52    | PASS0_CH_RANGEVIO_TR_OUT[52] | TCPWM0_16_ONE_CNT_TR_IN[44]  | SAR1 ch#20, range violation to TCPWM0 Group #0 Counter #44 trig = 2 |
| 53    | PASS0_CH_RANGEVIO_TR_OUT[53] | TCPWM0_16_ONE_CNT_TR_IN[45]  | SAR1 ch#21, range violation to TCPWM0 Group #0 Counter #45 trig = 2 |
| 54    | PASS0_CH_RANGEVIO_TR_OUT[54] | TCPWM0_16_ONE_CNT_TR_IN[46]  | SAR1 ch#22, range violation to TCPWM0 Group #0 Counter #46 trig = 2 |
| 55    | PASS0_CH_RANGEVIO_TR_OUT[55] | TCPWM0_16_ONE_CNT_TR_IN[47]  | SAR1 ch#23, range violation to TCPWM0 Group #0 Counter #47 trig = 2 |

Triggers one-to-one

**Table 19-1 One-to-one triggers (continued)**

| Input                                                        | Trigger in                   | Trigger out                  | Description                                                                                 |
|--------------------------------------------------------------|------------------------------|------------------------------|---------------------------------------------------------------------------------------------|
| 56                                                           | PASS0_CH_RANGEVIO_TR_OUT[56] | TCPWM0_16_ONE_CNT_TR_IN[48]  | SAR1 ch#24, range violation to TCPWM0 Group #0 Counter #48 trig = 2                         |
| 57                                                           | PASS0_CH_RANGEVIO_TR_OUT[57] | TCPWM0_16_ONE_CNT_TR_IN[49]  | SAR1 ch#25, range violation to TCPWM0 Group #0 Counter #49 trig = 2                         |
| 58                                                           | PASS0_CH_RANGEVIO_TR_OUT[58] | TCPWM0_16_ONE_CNT_TR_IN[50]  | SAR1 ch#26, range violation to TCPWM0 Group #0 Counter #50 trig = 2                         |
| 59                                                           | PASS0_CH_RANGEVIO_TR_OUT[59] | TCPWM0_16_ONE_CNT_TR_IN[51]  | SAR1 ch#27, range violation to TCPWM0 Group #0 Counter #51 trig = 2                         |
| 60                                                           | PASS0_CH_RANGEVIO_TR_OUT[60] | TCPWM0_16_ONE_CNT_TR_IN[52]  | SAR1 ch#28, range violation to TCPWM0 Group #0 Counter #52 trig = 2                         |
| 61                                                           | PASS0_CH_RANGEVIO_TR_OUT[61] | TCPWM0_16_ONE_CNT_TR_IN[53]  | SAR1 ch#29, range violation to TCPWM0 Group #0 Counter #53 trig = 2                         |
| 62                                                           | PASS0_CH_RANGEVIO_TR_OUT[62] | TCPWM0_16_ONE_CNT_TR_IN[54]  | SAR1 ch#30, range violation to TCPWM0 Group #0 Counter #54 trig = 2                         |
| 63                                                           | PASS0_CH_RANGEVIO_TR_OUT[63] | TCPWM0_16_ONE_CNT_TR_IN[55]  | SAR1 ch#31, range violation to TCPWM0 Group #0 Counter #55 trig = 2                         |
| 64                                                           | PASS0_CH_RANGEVIO_TR_OUT[64] | TCPWM0_16M_ONE_CNT_TR_IN[2]  | SAR2 ch#0, range violation to TCPWM0 Group #1 Counter #02 trig = 2                          |
| 65                                                           | PASS0_CH_RANGEVIO_TR_OUT[65] | TCPWM0_16M_ONE_CNT_TR_IN[5]  | SAR2 ch#1, range violation to TCPWM0 Group #1 Counter #05 trig = 2                          |
| 66                                                           | PASS0_CH_RANGEVIO_TR_OUT[66] | TCPWM0_16M_ONE_CNT_TR_IN[8]  | SAR2 ch#2, range violation to TCPWM0 Group #1 Counter #08 trig = 2                          |
| 67                                                           | PASS0_CH_RANGEVIO_TR_OUT[67] | TCPWM0_16M_ONE_CNT_TR_IN[11] | SAR2 ch#3, range violation to TCPWM0 Group #1 Counter #11 trig = 2                          |
| 68                                                           | PASS0_CH_RANGEVIO_TR_OUT[68] | TCPWM0_16_ONE_CNT_TR_IN[56]  | SAR2 ch#4, range violation to TCPWM0 Group #0 Counter #56 trig = 2                          |
| 69                                                           | PASS0_CH_RANGEVIO_TR_OUT[69] | TCPWM0_16_ONE_CNT_TR_IN[57]  | SAR2 ch#5, range violation to TCPWM0 Group #0 Counter #57 trig = 2                          |
| 70                                                           | PASS0_CH_RANGEVIO_TR_OUT[70] | TCPWM0_16_ONE_CNT_TR_IN[58]  | SAR2 ch#6, range violation to TCPWM0 Group #0 Counter #58 trig = 2                          |
| 71                                                           | PASS0_CH_RANGEVIO_TR_OUT[71] | TCPWM0_16_ONE_CNT_TR_IN[59]  | SAR2 ch#7, range violation to TCPWM0 Group #0 Counter #59 trig = 2                          |
| <b>MUX Group 7: TCPWM0 to PASS SARx</b>                      |                              |                              |                                                                                             |
| 0                                                            | TCPWM0_16M_TR_OUT1[0]        | PASS0_CH_TR_IN[0]            | TCPWM0 Group #1 Counter #00 (PWM0_M_0) to SAR0 ch#0                                         |
| 1                                                            | TCPWM0_16M_TR_OUT1[3]        | PASS0_CH_TR_IN[1]            | TCPWM0 Group #1 Counter #03 (PWM0_M_3) to SAR0 ch#1                                         |
| 2                                                            | TCPWM0_16M_TR_OUT1[6]        | PASS0_CH_TR_IN[2]            | TCPWM0 Group #1 Counter #06 (PWM0_M_6) to SAR0 ch#2                                         |
| 3                                                            | TCPWM0_16M_TR_OUT1[9]        | PASS0_CH_TR_IN[3]            | TCPWM0 Group #1 Counter #09 (PWM0_M_9) to SAR0 ch#3                                         |
| 4:31                                                         | TCPWM0_16_TR_OUT1[0:27]      | PASS0_CH_TR_IN[4:31]         | TCPWM0 Group #0 Counter #00 through 27 (PWM0_0 to PWM0_27) to SAR0 ch#4 through SAR0 ch#31  |
| 32                                                           | TCPWM0_16M_TR_OUT1[1]        | PASS0_CH_TR_IN[32]           | TCPWM0 Group #1 Counter #01 (PWM0_M_1) to SAR1 ch#0                                         |
| 33                                                           | TCPWM0_16M_TR_OUT1[4]        | PASS0_CH_TR_IN[33]           | TCPWM0 Group #1 Counter #04 (PWM0_M_4) to SAR1 ch#1                                         |
| 34                                                           | TCPWM0_16M_TR_OUT1[7]        | PASS0_CH_TR_IN[34]           | TCPWM0 Group #1 Counter #07 (PWM0_M_7) to SAR1 ch#2                                         |
| 35                                                           | TCPWM0_16M_TR_OUT1[10]       | PASS0_CH_TR_IN[35]           | TCPWM0 Group #1 Counter #10 (PWM0_M_10) to SAR1 ch#3                                        |
| 36:63                                                        | TCPWM0_16_TR_OUT1[28:55]     | PASS0_CH_TR_IN[36:63]        | TCPWM0 Group #0 Counter #28 through 55 (PWM0_28 to PWM0_55) to SAR1 ch#4 through SAR1 ch#31 |
| 64                                                           | TCPWM0_16M_TR_OUT1[2]        | PASS0_CH_TR_IN[64]           | TCPWM0 Group #1 Counter #02 (PWM0_M_2) to SAR2 ch#0                                         |
| 65                                                           | TCPWM0_16M_TR_OUT1[5]        | PASS0_CH_TR_IN[65]           | TCPWM0 Group #1 Counter #05 (PWM0_M_5) to SAR2 ch#1                                         |
| 66                                                           | TCPWM0_16M_TR_OUT1[8]        | PASS0_CH_TR_IN[66]           | TCPWM0 Group #1 Counter #08 (PWM0_M_8) to SAR2 ch#2                                         |
| 67                                                           | TCPWM0_16M_TR_OUT1[11]       | PASS0_CH_TR_IN[67]           | TCPWM0 Group #1 Counter #11 (PWM0_M_11) to SAR2 ch#3                                        |
| 68:71                                                        | TCPWM0_16_TR_OUT1[56:59]     | PASS0_CH_TR_IN[68:71]        | TCPWM0 Group #0 Counter #56 through 59 (PWM0_56 to PWM0_59) to SAR2 ch#4 through SAR2 ch#7  |
| <b>MUX Group 8: Acknowledge triggers from P-DMA1 to CAN1</b> |                              |                              |                                                                                             |
| 0                                                            | PDMA1_TR_OUT[38]             | CAN1_DBG_TR_ACK[0]           | CAN1 Channel#0 P-DMA1 acknowledge                                                           |
| 1                                                            | PDMA1_TR_OUT[41]             | CAN1_DBG_TR_ACK[1]           | CAN1 Channel#1 P-DMA1 acknowledge                                                           |

Triggers one-to-one

**Table 19-1 One-to-one triggers (continued)**

| Input                                                        | Trigger in              | Trigger out          | Description                                  |
|--------------------------------------------------------------|-------------------------|----------------------|----------------------------------------------|
| 2                                                            | PDMA1_TR_OUT[44]        | CAN1_DBG_TR_ACK[2]   | CAN1 Channel#2 P-DMA1 acknowledge            |
| 3                                                            | PDMA1_TR_OUT[47]        | CAN1_DBG_TR_ACK[3]   | CAN1 Channel#3 P-DMA1 acknowledge            |
| <b>MUX Group 9:</b> Acknowledge triggers from P-DMA0 to CAN0 |                         |                      |                                              |
| 0                                                            | PDMA0_TR_OUT[32]        | CAN0_DBG_TR_ACK[0]   | CAN0 Channel#0 P-DMA0 acknowledge            |
| 1                                                            | PDMA0_TR_OUT[35]        | CAN0_DBG_TR_ACK[1]   | CAN0 Channel#1 P-DMA0 acknowledge            |
| 2                                                            | PDMA0_TR_OUT[38]        | CAN0_DBG_TR_ACK[2]   | CAN0 Channel#2 P-DMA0 acknowledge            |
| 3                                                            | PDMA0_TR_OUT[41]        | CAN0_DBG_TR_ACK[3]   | CAN0 Channel#3 P-DMA0 acknowledge            |
| <b>MUX Group 10:</b> TCPWM0 to LIN0 triggers                 |                         |                      |                                              |
| 0:15                                                         | TCPWM0_16_TR_OUT0[0:15] | LIN0_CMD_TR_IN[0:15] | TCPWM0 (Group #0 Counter #00 to #15) to LIN0 |

## 20 Peripheral clocks

**Table 20-1 Peripheral clock assignments**

| Output                             | Destination               | Description       |
|------------------------------------|---------------------------|-------------------|
| <b>CPUSS root clocks (Group 0)</b> |                           |                   |
| 0                                  | PCLK_CPUSS_CLOCK_TRACE_IN | Trace clock       |
| 1                                  | PCLK_SMARTIO12_CLOCK      | Smart I/O #12     |
| 2                                  | PCLK_SMARTIO13_CLOCK      | Smart I/O #13     |
| 3                                  | PCLK_SMARTIO14_CLOCK      | Smart I/O #14     |
| 4                                  | PCLK_SMARTIO15_CLOCK      | Smart I/O #15     |
| 5                                  | PCLK_SMARTIO17_CLOCK      | Smart I/O #17     |
| <b>COMM root clocks (Group 1)</b>  |                           |                   |
| 0                                  | PCLK_CANFD0_CLOCK_CAN0    | CAN0, Channel #0  |
| 1                                  | PCLK_CANFD0_CLOCK_CAN1    | CAN0, Channel #1  |
| 2                                  | PCLK_CANFD0_CLOCK_CAN2    | CAN0, Channel #2  |
| 3                                  | PCLK_CANFD0_CLOCK_CAN3    | CAN0, Channel #3  |
| 4                                  | PCLK_CANFD1_CLOCK_CAN0    | CAN1, Channel #0  |
| 5                                  | PCLK_CANFD1_CLOCK_CAN1    | CAN1, Channel #1  |
| 6                                  | PCLK_CANFD1_CLOCK_CAN2    | CAN1, Channel #2  |
| 7                                  | PCLK_CANFD1_CLOCK_CAN3    | CAN1, Channel #3  |
| 8                                  | PCLK_LIN0_CLOCK_CH_EN0    | LIN0, Channel #0  |
| 9                                  | PCLK_LIN0_CLOCK_CH_EN1    | LIN0, Channel #1  |
| 10                                 | PCLK_LIN0_CLOCK_CH_EN2    | LIN0, Channel #2  |
| 11                                 | PCLK_LIN0_CLOCK_CH_EN3    | LIN0, Channel #3  |
| 12                                 | PCLK_LIN0_CLOCK_CH_EN4    | LIN0, Channel #4  |
| 13                                 | PCLK_LIN0_CLOCK_CH_EN5    | LIN0, Channel #5  |
| 14                                 | PCLK_LIN0_CLOCK_CH_EN6    | LIN0, Channel #6  |
| 15                                 | PCLK_LIN0_CLOCK_CH_EN7    | LIN0, Channel #7  |
| 16                                 | PCLK_LIN0_CLOCK_CH_EN8    | LIN0, Channel #8  |
| 17                                 | PCLK_LIN0_CLOCK_CH_EN9    | LIN0, Channel #9  |
| 18                                 | PCLK_LIN0_CLOCK_CH_EN10   | LIN0, Channel #10 |
| 19                                 | PCLK_LIN0_CLOCK_CH_EN11   | LIN0, Channel #11 |
| 20                                 | PCLK_LIN0_CLOCK_CH_EN12   | LIN0, Channel #12 |
| 21                                 | PCLK_LIN0_CLOCK_CH_EN13   | LIN0, Channel #13 |
| 22                                 | PCLK_LIN0_CLOCK_CH_EN14   | LIN0, Channel #14 |
| 23                                 | PCLK_LIN0_CLOCK_CH_EN15   | LIN0, Channel #15 |
| 24                                 | PCLK_SCB0_CLOCK           | SCB0              |
| 25                                 | PCLK_SCB1_CLOCK           | SCB1              |
| 26                                 | PCLK_SCB2_CLOCK           | SCB2              |
| 27                                 | PCLK_SCB3_CLOCK           | SCB3              |
| 28                                 | PCLK_SCB4_CLOCK           | SCB4              |
| 29                                 | PCLK_SCB5_CLOCK           | SCB5              |
| 30                                 | PCLK_SCB6_CLOCK           | SCB6              |
| 31                                 | PCLK_SCB7_CLOCK           | SCB7              |
| 32                                 | PCLK_SCB8_CLOCK           | SCB8              |

## Peripheral clocks

**Table 20-1** Peripheral clock assignments (continued)

| Output | Destination           | Description                  |
|--------|-----------------------|------------------------------|
| 33     | PCLK_SCB9_CLOCK       | SCB9                         |
| 34     | PCLK_SCB10_CLOCK      | SCB10                        |
| 35     | PCLK_PASS0_CLOCK_SAR0 | SAR0                         |
| 36     | PCLK_PASS0_CLOCK_SAR1 | SAR1                         |
| 37     | PCLK_PASS0_CLOCK_SAR2 | SAR2                         |
| 38     | PCLK_TCPWM0_CLOCKS0   | TCPWM0 Group #0, Counter #0  |
| 39     | PCLK_TCPWM0_CLOCKS1   | TCPWM0 Group #0, Counter #1  |
| 40     | PCLK_TCPWM0_CLOCKS2   | TCPWM0 Group #0, Counter #2  |
| 41     | PCLK_TCPWM0_CLOCKS3   | TCPWM0 Group #0, Counter #3  |
| 42     | PCLK_TCPWM0_CLOCKS4   | TCPWM0 Group #0, Counter #4  |
| 43     | PCLK_TCPWM0_CLOCKS5   | TCPWM0 Group #0, Counter #5  |
| 44     | PCLK_TCPWM0_CLOCKS6   | TCPWM0 Group #0, Counter #6  |
| 45     | PCLK_TCPWM0_CLOCKS7   | TCPWM0 Group #0, Counter #7  |
| 46     | PCLK_TCPWM0_CLOCKS8   | TCPWM0 Group #0, Counter #8  |
| 47     | PCLK_TCPWM0_CLOCKS9   | TCPWM0 Group #0, Counter #9  |
| 48     | PCLK_TCPWM0_CLOCKS10  | TCPWM0 Group #0, Counter #10 |
| 49     | PCLK_TCPWM0_CLOCKS11  | TCPWM0 Group #0, Counter #11 |
| 50     | PCLK_TCPWM0_CLOCKS12  | TCPWM0 Group #0, Counter #12 |
| 51     | PCLK_TCPWM0_CLOCKS13  | TCPWM0 Group #0, Counter #13 |
| 52     | PCLK_TCPWM0_CLOCKS14  | TCPWM0 Group #0, Counter #14 |
| 53     | PCLK_TCPWM0_CLOCKS15  | TCPWM0 Group #0, Counter #15 |
| 54     | PCLK_TCPWM0_CLOCKS16  | TCPWM0 Group #0, Counter #16 |
| 55     | PCLK_TCPWM0_CLOCKS17  | TCPWM0 Group #0, Counter #17 |
| 56     | PCLK_TCPWM0_CLOCKS18  | TCPWM0 Group #0, Counter #18 |
| 57     | PCLK_TCPWM0_CLOCKS19  | TCPWM0 Group #0, Counter #19 |
| 58     | PCLK_TCPWM0_CLOCKS20  | TCPWM0 Group #0, Counter #20 |
| 59     | PCLK_TCPWM0_CLOCKS21  | TCPWM0 Group #0, Counter #21 |
| 60     | PCLK_TCPWM0_CLOCKS22  | TCPWM0 Group #0, Counter #22 |
| 61     | PCLK_TCPWM0_CLOCKS23  | TCPWM0 Group #0, Counter #23 |
| 62     | PCLK_TCPWM0_CLOCKS24  | TCPWM0 Group #0, Counter #24 |
| 63     | PCLK_TCPWM0_CLOCKS25  | TCPWM0 Group #0, Counter #25 |
| 64     | PCLK_TCPWM0_CLOCKS26  | TCPWM0 Group #0, Counter #26 |
| 65     | PCLK_TCPWM0_CLOCKS27  | TCPWM0 Group #0, Counter #27 |
| 66     | PCLK_TCPWM0_CLOCKS28  | TCPWM0 Group #0, Counter #28 |
| 67     | PCLK_TCPWM0_CLOCKS29  | TCPWM0 Group #0, Counter #29 |
| 68     | PCLK_TCPWM0_CLOCKS30  | TCPWM0 Group #0, Counter #30 |
| 69     | PCLK_TCPWM0_CLOCKS31  | TCPWM0 Group #0, Counter #31 |
| 70     | PCLK_TCPWM0_CLOCKS32  | TCPWM0 Group #0, Counter #32 |
| 71     | PCLK_TCPWM0_CLOCKS33  | TCPWM0 Group #0, Counter #33 |
| 72     | PCLK_TCPWM0_CLOCKS34  | TCPWM0 Group #0, Counter #34 |
| 73     | PCLK_TCPWM0_CLOCKS35  | TCPWM0 Group #0, Counter #35 |
| 74     | PCLK_TCPWM0_CLOCKS36  | TCPWM0 Group #0, Counter #36 |

## Peripheral clocks

**Table 20-1** Peripheral clock assignments (continued)

| Output | Destination           | Description                  |
|--------|-----------------------|------------------------------|
| 75     | PCLK_TCPWM0_CLOCKS37  | TCPWM0 Group #0, Counter #37 |
| 76     | PCLK_TCPWM0_CLOCKS38  | TCPWM0 Group #0, Counter #38 |
| 77     | PCLK_TCPWM0_CLOCKS39  | TCPWM0 Group #0, Counter #39 |
| 78     | PCLK_TCPWM0_CLOCKS40  | TCPWM0 Group #0, Counter #40 |
| 79     | PCLK_TCPWM0_CLOCKS41  | TCPWM0 Group #0, Counter #41 |
| 80     | PCLK_TCPWM0_CLOCKS42  | TCPWM0 Group #0, Counter #42 |
| 81     | PCLK_TCPWM0_CLOCKS43  | TCPWM0 Group #0, Counter #43 |
| 82     | PCLK_TCPWM0_CLOCKS44  | TCPWM0 Group #0, Counter #44 |
| 83     | PCLK_TCPWM0_CLOCKS45  | TCPWM0 Group #0, Counter #45 |
| 84     | PCLK_TCPWM0_CLOCKS46  | TCPWM0 Group #0, Counter #46 |
| 85     | PCLK_TCPWM0_CLOCKS47  | TCPWM0 Group #0, Counter #47 |
| 86     | PCLK_TCPWM0_CLOCKS48  | TCPWM0 Group #0, Counter #48 |
| 87     | PCLK_TCPWM0_CLOCKS49  | TCPWM0 Group #0, Counter #49 |
| 88     | PCLK_TCPWM0_CLOCKS50  | TCPWM0 Group #0, Counter #50 |
| 89     | PCLK_TCPWM0_CLOCKS51  | TCPWM0 Group #0, Counter #51 |
| 90     | PCLK_TCPWM0_CLOCKS52  | TCPWM0 Group #0, Counter #52 |
| 91     | PCLK_TCPWM0_CLOCKS53  | TCPWM0 Group #0, Counter #53 |
| 92     | PCLK_TCPWM0_CLOCKS54  | TCPWM0 Group #0, Counter #54 |
| 93     | PCLK_TCPWM0_CLOCKS55  | TCPWM0 Group #0, Counter #55 |
| 94     | PCLK_TCPWM0_CLOCKS56  | TCPWM0 Group #0, Counter #56 |
| 95     | PCLK_TCPWM0_CLOCKS57  | TCPWM0 Group #0, Counter #57 |
| 96     | PCLK_TCPWM0_CLOCKS58  | TCPWM0 Group #0, Counter #58 |
| 97     | PCLK_TCPWM0_CLOCKS59  | TCPWM0 Group #0, Counter #59 |
| 98     | PCLK_TCPWM0_CLOCKS60  | TCPWM0 Group #0, Counter #60 |
| 99     | PCLK_TCPWM0_CLOCKS61  | TCPWM0 Group #0, Counter #61 |
| 100    | PCLK_TCPWM0_CLOCKS62  | TCPWM0 Group #0, Counter #62 |
| 101    | PCLK_TCPWM0_CLOCKS256 | TCPWM0 Group #1, Counter #0  |
| 102    | PCLK_TCPWM0_CLOCKS257 | TCPWM0 Group #1, Counter #1  |
| 103    | PCLK_TCPWM0_CLOCKS258 | TCPWM0 Group #1, Counter #2  |
| 104    | PCLK_TCPWM0_CLOCKS259 | TCPWM0 Group #1, Counter #3  |
| 105    | PCLK_TCPWM0_CLOCKS260 | TCPWM0 Group #1, Counter #4  |
| 106    | PCLK_TCPWM0_CLOCKS261 | TCPWM0 Group #1, Counter #5  |
| 107    | PCLK_TCPWM0_CLOCKS262 | TCPWM0 Group #1, Counter #6  |
| 108    | PCLK_TCPWM0_CLOCKS263 | TCPWM0 Group #1, Counter #7  |
| 109    | PCLK_TCPWM0_CLOCKS264 | TCPWM0 Group #1, Counter #8  |
| 110    | PCLK_TCPWM0_CLOCKS265 | TCPWM0 Group #1, Counter #9  |
| 111    | PCLK_TCPWM0_CLOCKS266 | TCPWM0 Group #1, Counter #10 |
| 112    | PCLK_TCPWM0_CLOCKS267 | TCPWM0 Group #1, Counter #11 |
| 113    | PCLK_TCPWM0_CLOCKS512 | TCPWM0 Group #2, Counter #0  |
| 114    | PCLK_TCPWM0_CLOCKS513 | TCPWM0 Group #2, Counter #1  |
| 115    | PCLK_TCPWM0_CLOCKS514 | TCPWM0 Group #2, Counter #2  |
| 116    | PCLK_TCPWM0_CLOCKS515 | TCPWM0 Group #2, Counter #3  |

Peripheral clocks

**Table 20-1**     **Peripheral clock assignments** *(continued)*

| Output | Destination           | Description                 |
|--------|-----------------------|-----------------------------|
| 117    | PCLK_TCPWM0_CLOCKS516 | TCPWM0 Group #2, Counter #4 |
| 118    | PCLK_TCPWM0_CLOCKS517 | TCPWM0 Group #2, Counter #5 |
| 119    | PCLK_TCPWM0_CLOCKS518 | TCPWM0 Group #2, Counter #6 |
| 120    | PCLK_TCPWM0_CLOCKS519 | TCPWM0 Group #2, Counter #7 |

## Faults

## 21 Faults

**Table 21-1 Fault assignments**

| Fault | Source                   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | CPUSS_MPU_VIO_0          | CM0+ SMPU violation<br>DATA0[31:0]: Violating address.<br>DATA1[0]: User read.<br>DATA1[1]: User write.<br>DATA1[2]: User execute.<br>DATA1[3]: Privileged read.<br>DATA1[4]: Privileged write.<br>DATA1[5]: Privileged execute.<br>DATA1[6]: Non-secure.<br>DATA1[11:8]: Master identifier.<br>DATA1[15:12]: Protection context identifier.<br>DATA1[31]: '0' MPU violation; '1': SMPU violation.                                                                                      |
| 1     | CPUSS_MPU_VIO_1          | CRYPTO SMPU violation. See CPUSS_MPU_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 2     | CPUSS_MPU_VIO_2          | P-DMA0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 3     | CPUSS_MPU_VIO_3          | P-DMA1 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 4     | CPUSS_MPU_VIO_4          | M-DMA0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 5     | CPUSS_MPU_VIO_5          | SDHC MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 9     | CPUSS_MPU_VIO_6          | Ethernet0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 13    | CPUSS_MPU_VIO_13         | CM7_1 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 14    | CPUSS_MPU_VIO_14         | CM7_0 MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 15    | CPUSS_MPU_VIO_15         | Test Controller MPU/SMPU violation. See CPUSS_MPU_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 16    | CPUSS_CM7_1_TCM_C_ECC    | Correctable ECC error in CM7_1 TCM memory<br>DATA0[23:2]: Violating address.<br>DATA1[7:0]: Syndrome of code word (at address offset 0x0).<br>DATA1[31:30]: 0=ITCM, 2=D0TCM, 3=D1TCM                                                                                                                                                                                                                                                                                                    |
| 17    | CPUSS_CM7_1_TCM_NC_ECC   | Non Correctable ECC error in CM7_1 TCM memory.<br>See CPUSS_CM7_1_TCM_C_ECC description.                                                                                                                                                                                                                                                                                                                                                                                                |
| 18    | CPUSS_CM7_0_CACHE_C_ECC  | Correctable ECC error in CM7_0 Cache memories<br>DATA0[16:2]: location information: Tag/Data SRAM, Way, Index and line Offset, see CM7 UGRM IEBR0/DEBR0 description for details.<br>DATA0[31]: 0=Instruction cache, 1= Data cache                                                                                                                                                                                                                                                       |
| 19    | CPUSS_CM7_0_CACHE_NC_ECC | Non Correctable ECC error in CM7_0 Cache memories.<br>See CPUSS_CM7_0_CACHE_C_ECC description.                                                                                                                                                                                                                                                                                                                                                                                          |
| 20    | CPUSS_CM7_1_CACHE_C_ECC  | Correctable ECC error in CM7_1 Cache memories.<br>See CPUSS_CM7_0_CACHE_C_ECC description.                                                                                                                                                                                                                                                                                                                                                                                              |
| 21    | CPUSS_CM7_1_CACHE_NC_ECC | Non Correctable ECC error in CM7_1 Cache memories.<br>See CPUSS_CM7_0_CACHE_C_ECC description.                                                                                                                                                                                                                                                                                                                                                                                          |
| 25    | PERI_MS_VIO_4            | P-DMA1 Peripheral Master Interface PPU violation.<br>See PERI_MS_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                                                     |
| 26    | PERI_PERI_C_ECC          | Peripheral protection SRAM correctable ECC violation<br>DATA0[10:0]: Violating address.<br>DATA1[7:0]: Syndrome of SRAM word.                                                                                                                                                                                                                                                                                                                                                           |
| 27    | PERI_PERI_NC_ECC         | Peripheral protection SRAM non-correctable ECC violation                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 28    | PERI_MS_VIO_0            | CM0+ Peripheral Master Interface PPU violation<br>DATA0[31:0]: Violating address.<br>DATA1[0]: User read.<br>DATA1[1]: User write.<br>DATA1[2]: User execute.<br>DATA1[3]: Privileged read.<br>DATA1[4]: Privileged write.<br>DATA1[5]: Privileged execute.<br>DATA1[6]: Non-secure.<br>DATA1[11:8]: Master identifier.<br>DATA1[15:12]: Protection context identifier.<br>DATA1[31:28]: "0": master interface, PPU violation, "1": timeout detected, "2": bus error, other: undefined. |
| 29    | PERI_MS_VIO_1            | CM7_0 Peripheral Master Interface PPU violation.<br>See PERI_MS_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                                                      |
| 30    | PERI_MS_VIO_2            | CM7_1 Peripheral Master Interface PPU violation.<br>See PERI_MS_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                                                      |
| 31    | PERI_MS_VIO_3            | P-DMA0 Peripheral Master Interface PPU_3 violation.<br>See PERI_MS_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                                                   |

## Faults

**Table 21-1**      **Fault assignments** *(continued)*

| Fault | Source                     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 32    | PERI_GROUP_VIO_0           | Peripheral Group #0 violation.<br>DATA0[31:0]: Violating address.<br>DATA1[0]: User read.<br>DATA1[1]: User write.<br>DATA1[2]: User execute.<br>DATA1[3]: Privileged read.<br>DATA1[4]: Privileged write.<br>DATA1[5]: Privileged execute.<br>DATA1[6]: Non-secure.<br>DATA1[11:8]: Master identifier.<br>DATA1[15:12]: Protection context identifier.<br>DATA1[31:28]: "0": decoder or peripheral bus error, other: undefined.           |
| 33    | PERI_GROUP_VIO_1           | Peripheral Group #1 violation. See PERI_GROUP_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                           |
| 34    | PERI_GROUP_VIO_2           | Peripheral Group #2 violation. See PERI_GROUP_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                           |
| 35    | PERI_GROUP_VIO_3           | Peripheral Group #3 violation. See PERI_GROUP_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                           |
| 36    | PERI_GROUP_VIO_4           | Peripheral Group #4 violation. See PERI_GROUP_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                           |
| 37    | PERI_GROUP_VIO_5           | Peripheral Group #5 violation. See PERI_GROUP_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                           |
| 38    | PERI_GROUP_VIO_6           | Peripheral Group #6 violation. See PERI_GROUP_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                           |
| 40    | PERI_GROUP_VIO_8           | Peripheral Group #8 violation. See PERI_GROUP_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                           |
| 41    | PERI_GROUP_VIO_9           | Peripheral Group #9 violation. See PERI_GROUP_VIO_0 description.                                                                                                                                                                                                                                                                                                                                                                           |
| 48    | CPUSS_FLASHC_MAIN_BUS_ERR  | Flash controller main flash bus error<br>FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address.<br>FAULT_DATA1[11:8]: Master identifier.                                                                                                                                                                                                                                          |
| 49    | CPUSS_FLASHC_MAIN_C_ECC    | Flash controller main flash correctable ECC violation<br>DATA[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address.<br>DATA1[7:0]: Syndrome of 64-bit word (at address offset 0x00).<br>DATA1[15:8]: Syndrome of 64-bit word (at address offset 0x08).<br>DATA1[23:16]: Syndrome of 64-bit word (at address offset 0x10).<br>DATA1[31:24]: Syndrome of 64-bit word (at address offset 0x18). |
| 50    | CPUSS_FLASHC_MAIN_NC_ECC   | Flash controller main flash non-correctable ECC violation.<br>See CPUSS_FLASHC_MAIN_C_ECC description.                                                                                                                                                                                                                                                                                                                                     |
| 51    | CPUSS_FLASHC_WORK_BUS_ERR  | Flash controller work-flash bus error.<br>See CPUSS_FLASHC_MAIN_BUS_ERR description.                                                                                                                                                                                                                                                                                                                                                       |
| 52    | CPUSS_FLASHC_WORK_C_ECC    | Flash controller work flash correctable ECC violation.<br>DATA[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address.<br>DATA1[6:0]: Syndrome of 32-bit word.                                                                                                                                                                                                                                 |
| 53    | CPUSS_FLASHC_WORK_NC_ECC   | Flash controller work-flash non-correctable ECC violation.<br>See CPUSS_FLASHC_WORK_C_ECC description.                                                                                                                                                                                                                                                                                                                                     |
| 54    | CPUSS_FLASHC_CM0_CA_C_ECC  | Flash controller CM0+ cache correctable ECC violation.<br>DATA0[26:0]: Violating address.<br>DATA1[6:0]: Syndrome of 32-bit SRAM word (at address offset 0x0).<br>DATA1[14:8]: Syndrome of 32-bit SRAM word (at address offset 0x4).<br>DATA1[22:16]: Syndrome of 32-bit SRAM word (at address offset 0x8).<br>DATA1[30:24]: Syndrome of 32-bit SRAM word (at address offset 0xc).                                                         |
| 55    | CPUSS_FLASHC_CM0_CA_NC_ECC | Flash controller CM0+ cache non-correctable ECC violation.<br>See CPUSS_FLASHC_CM0_CA_C_ECC description.                                                                                                                                                                                                                                                                                                                                   |
| 56    | CPUSS_CM7_0_TCM_C_ECC      | CPU CM7_0 TCM memory correctable ECC violation.<br>See CPUSS_CM7_1_TCM_C_ECC description.                                                                                                                                                                                                                                                                                                                                                  |
| 57    | CPUSS_CM7_0_TCM_NC_ECC     | CPU CM7_0 TCM memory non-correctable ECC violation.<br>See CPUSS_CM7_1_TCM_C_ECC description.                                                                                                                                                                                                                                                                                                                                              |
| 58    | CPUSS_RAMC0_C_ECC          | System memory controller 0 correctable ECC violation:<br>DATA0[31:0]: Violating address.<br>DATA1[6:0]: Syndrome of 32-bit SRAM code word.                                                                                                                                                                                                                                                                                                 |
| 59    | CPUSS_RAMC0_NC_ECC         | System memory controller 0 non-correctable ECC violation.<br>See CPUSS_RAMC0_C_ECC description.                                                                                                                                                                                                                                                                                                                                            |
| 60    | CPUSS_RAMC1_C_ECC          | System memory controller 1 correctable ECC violation.<br>See CPUSS_RAMC0_C_ECC description.                                                                                                                                                                                                                                                                                                                                                |
| 61    | CPUSS_RAMC1_NC_ECC         | System memory controller 1 non-correctable ECC violation.<br>See CPUSS_RAMC0_C_ECC description.                                                                                                                                                                                                                                                                                                                                            |
| 64    | CPUSS_CRYPT0_C_ECC         | Crypto memory correctable ECC violation.<br>DATA0[31:0]: Violating address.<br>DATA1[6:0]: Syndrome of Least Significant 32-bit SRAM.<br>DATA1[14:8]: Syndrome of Most Significant 32-bit SRAM.                                                                                                                                                                                                                                            |

## Faults

**Table 21-1 Fault assignments (continued)**

| Fault | Source               | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 65    | CPUSS_CRYPTO_NC_ECC  | CRYPTO memory non-correctable ECC violation.<br>See CPUSS_CRYPTO_C_ECC description.                                                                                                                                                                                                                                                                                                                                                                                              |
| 70    | CPUSS_DW0_C_ECC      | P-DMA0 memory correctable ECC violation:<br>DATA0[11:0]: Violating DW SRAM address<br>(word address, assuming byte addressable).<br>DATA1[6:0]: Syndrome of 32-bit SRAM code word.                                                                                                                                                                                                                                                                                               |
| 71    | CPUSS_DW0_NC_ECC     | P-DMA0 memory non-correctable ECC violation.<br>See CPUSS_DW0_C_ECC description.                                                                                                                                                                                                                                                                                                                                                                                                 |
| 72    | CPUSS_DW1_C_ECC      | P-DMA1 memory correctable ECC violation.<br>See CPUSS_DW0_C_ECC description.                                                                                                                                                                                                                                                                                                                                                                                                     |
| 73    | CPUSS_DW1_NC_ECC     | P-DMA1 memory non-correctable ECC violation.<br>See CPUSS_DW0_C_ECC description.                                                                                                                                                                                                                                                                                                                                                                                                 |
| 74    | CPUSS_FM_SRAM_C_ECC  | Flash code storage SRAM memory correctable ECC violation:<br>DATA0[15:0]: Address location in the eCT Flash SRAM.<br>DATA1[6:0]: Syndrome of 32-bit SRAM word.                                                                                                                                                                                                                                                                                                                   |
| 75    | CPUSS_FM_SRAM_NC_ECC | Flash code storage SRAM memory non-correctable ECC violation:<br>See CPUSS_FM_SRAM_C_ECC description.                                                                                                                                                                                                                                                                                                                                                                            |
| 80    | CANFD_0__CAN_C_ECC   | CAN0 message buffer correctable ECC violation:<br>DATA0[15:0]: Violating address.<br>DATA0[22:16]: ECC violating data[38:32] from MRAM.<br>DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxrtcanfd cluster, 8 = AHB I/F<br>DATA1[31:0]: ECC violating data[31:0] from MRAM.                                                                                                                                                                                               |
| 81    | CANFD_0__CAN_NC_ECC  | CAN0 message buffer non-correctable ECC violation:<br>DATA0[15:0]: Violating address.<br>DATA0[22:16]: ECC violating data[38:32] from MRAM (not for Address Error).<br>DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxrtcanfd cluster, 8 = AHB I/F<br>DATA0[30]: Write access, only possible for Address Error<br>DATA0[31]: Address Error: a CAN channel did an MRAM access above MRAM_SIZE<br>DATA1[31:0]: ECC violating data[31:0] from MRAM (not for Address Error). |
| 82    | CANFD_1__CAN_C_ECC   | CAN1 message buffer correctable ECC violation.<br>See CANFD_0__CAN_C_ECC description.                                                                                                                                                                                                                                                                                                                                                                                            |
| 83    | CANFD_1__CAN_NC_ECC  | CAN1 message buffer non-correctable ECC violation.<br>See CANFD_0__CAN_NC_ECC description.                                                                                                                                                                                                                                                                                                                                                                                       |
| 90    | SRSS_FAULT_CSV       | Consolidated fault output for clock supervisors. Multiple CSV can detect a violation at the same time.<br>DATA0[15:0]: CLK_HF* root CSV violation flags.<br>DATA0[24]: CLK_REF CSV violation flag (reference clock for CLK_HF CSVs)<br>DATA0[25]: CLK_LF CSV violation flag<br>DATA0[26]: CLK_HVIL0 CSV violation flag                                                                                                                                                           |
| 91    | SRSS_FAULT_SSV       | Consolidated fault output for supply supervisors. Multiple CSV can detect a violation at the same time.<br>DATA0[0]: BOD on VDPA<br>DATA0[1]: OVD on VDPA<br>DATA0[16]: LVD/HVD #1<br>DATA0[17]: LVD/HVD #2                                                                                                                                                                                                                                                                      |
| 92    | SRSS_FAULT_MCWDT0    | Fault output for MCWDT0 (all sub-counters) Multiple counters can detect a violation at the same time.<br>DATA0[0]: MCWDT sub counter 0 LOWER_LIMIT<br>DATA0[1]: MCWDT sub counter 0 UPPER_LIMIT<br>DATA0[2]: MCWDT sub counter 1 LOWER_LIMIT<br>DATA0[3]: MCWDT sub counter 1 UPPER_LIMIT                                                                                                                                                                                        |
| 93    | SRSS_FAULT_MCWDT1    | Fault output for MCWDT1 (all sub-counters).<br>See SRSS_FAULT_MCWDT0 description.                                                                                                                                                                                                                                                                                                                                                                                                |
| 94    | SRSS_FAULT_MCWDT2    | Fault output for MCWDT2 (all sub-counters).<br>See SRSS_FAULT_MCWDT0 description.                                                                                                                                                                                                                                                                                                                                                                                                |

## 22 Peripheral protection unit fixed structure pairs

Protection pair is a pair PPU structures, a master, and a slave structure. The master structure protects the slave structure, and the slave structure protects resources such as peripheral registers, or the peripheral itself.

**Table 22-1 PPU fixed structure pairs**

| Pair no. | PPU fixed structure pair                  | Address    | Size       | Description                     |
|----------|-------------------------------------------|------------|------------|---------------------------------|
| 0        | PERI_MS_PPU_FX_PERI_MAIN                  | 0x40000200 | 0x00000040 | Peripheral Interconnect main    |
| 1        | PERI_MS_PPU_FX_PERI_SECURE                | 0x40002000 | 0x00000004 | Peripheral interconnect secure  |
| 2        | PERI_MS_PPU_FX_PERI_GR0_GROUP             | 0x40004010 | 0x00000004 | Peripheral Group #0 main        |
| 3        | PERI_MS_PPU_FX_PERI_GR1_GROUP             | 0x40004050 | 0x00000004 | Peripheral Group #1 main        |
| 4        | PERI_MS_PPU_FX_PERI_GR2_GROUP             | 0x40004090 | 0x00000004 | Peripheral Group #2 main        |
| 5        | PERI_MS_PPU_FX_PERI_GR3_GROUP             | 0x400040C0 | 0x00000020 | Peripheral Group #3 main        |
| 6        | PERI_MS_PPU_FX_PERI_GR4_GROUP             | 0x40004100 | 0x00000020 | Peripheral Group #4 main        |
| 7        | PERI_MS_PPU_FX_PERI_GR5_GROUP             | 0x40004140 | 0x00000020 | Peripheral Group #5 main        |
| 8        | PERI_MS_PPU_FX_PERI_GR6_GROUP             | 0x40004180 | 0x00000020 | Peripheral Group #6 main        |
| 9        | PERI_MS_PPU_FX_PERI_GR8_GROUP             | 0x40004200 | 0x00000020 | Peripheral Group #8 main        |
| 10       | PERI_MS_PPU_FX_PERI_GR9_GROUP             | 0x40004240 | 0x00000020 | Peripheral Group #9 main        |
| 11       | PERI_MS_PPU_FX_PERI_GR0_BOOT              | 0x40004020 | 0x00000004 | Peripheral Group #0 boot        |
| 12       | PERI_MS_PPU_FX_PERI_GR1_BOOT              | 0x40004060 | 0x00000004 | Peripheral Group #1 boot        |
| 13       | PERI_MS_PPU_FX_PERI_GR2_BOOT              | 0x400040A0 | 0x00000004 | Peripheral Group #2 boot        |
| 14       | PERI_MS_PPU_FX_PERI_GR3_BOOT              | 0x400040E0 | 0x00000004 | Peripheral Group #3 boot        |
| 15       | PERI_MS_PPU_FX_PERI_GR4_BOOT              | 0x40004120 | 0x00000004 | Peripheral Group #4 boot        |
| 16       | PERI_MS_PPU_FX_PERI_GR5_BOOT              | 0x40004160 | 0x00000004 | Peripheral Group #5 boot        |
| 17       | PERI_MS_PPU_FX_PERI_GR6_BOOT              | 0x400041A0 | 0x00000004 | Peripheral Group #6 boot        |
| 18       | PERI_MS_PPU_FX_PERI_GR8_BOOT              | 0x40004220 | 0x00000004 | Peripheral Group #8 boot        |
| 19       | PERI_MS_PPU_FX_PERI_GR9_BOOT              | 0x40004260 | 0x00000004 | Peripheral Group #9 boot        |
| 20       | PERI_MS_PPU_FX_PERI_TR                    | 0x40008000 | 0x00008000 | Peripheral trigger multiplexer  |
| 21       | PERI_MS_PPU_FX_PERI_MS_BOOT               | 0x40030000 | 0x00001000 | Peripheral master slave boot    |
| 22       | PERI_MS_PPU_FX_PERI_PCLK_MAIN             | 0x40040000 | 0x00004000 | Peripheral clock main           |
| 23       | PERI_MS_PPU_FX_CRYPT0_MAIN                | 0x40100000 | 0x00000400 | Crypto main                     |
| 24       | PERI_MS_PPU_FX_CRYPT0_CRYPT0              | 0x40101000 | 0x00000800 | Crypto MMIO (Memory Mapped I/O) |
| 25       | PERI_MS_PPU_FX_CRYPT0_BOOT                | 0x40102000 | 0x00000100 | Crypto boot                     |
| 26       | PERI_MS_PPU_FX_CRYPT0_KEY0                | 0x40102100 | 0x00000004 | Crypto Key #0                   |
| 27       | PERI_MS_PPU_FX_CRYPT0_KEY1                | 0x40102120 | 0x00000004 | Crypto Key #1                   |
| 28       | PERI_MS_PPU_FX_CRYPT0_BUF                 | 0x40108000 | 0x00002000 | Crypto buffer                   |
| 29       | PERI_MS_PPU_FX_CPUSS_CM7_0                | 0x40200000 | 0x00000400 | CM7_0 CPU core                  |
| 30       | PERI_MS_PPU_FX_CPUSS_CM7_1                | 0x40200400 | 0x00000400 | CM7_1 CPU core                  |
| 31       | PERI_MS_PPU_FX_CPUSS_CM0                  | 0x40201000 | 0x00001000 | CM0+ CPU core                   |
| 32       | PERI_MS_PPU_FX_CPUSS_BOOT <sup>[40]</sup> | 0x40202000 | 0x00000200 | CPUSS boot                      |
| 33       | PERI_MS_PPU_FX_CPUSS_CM0_INT              | 0x40208000 | 0x00001000 | CPUSS CM0+ interrupts           |
| 34       | PERI_MS_PPU_FX_CPUSS_CM7_0_INT            | 0x4020A000 | 0x00001000 | CPUSS CM7_0 interrupts          |
| 35       | PERI_MS_PPU_FX_CPUSS_CM7_1_INT            | 0x4020C000 | 0x00001000 | CPUSS CM7_1 interrupts          |
| 36       | PERI_MS_PPU_FX_FAULT_STRUCT0_MAIN         | 0x40210000 | 0x00000100 | CPUSS Fault Structure #0 main   |
| 37       | PERI_MS_PPU_FX_FAULT_STRUCT1_MAIN         | 0x40210100 | 0x00000100 | CPUSS Fault Structure #1 main   |

**Note**

40.Fixed PPU is configured inside the Boot and user is not allowed to change the attributes of this PPU.

**Table 22-1 PPU fixed structure pairs** (continued)

| Pair no. | PPU fixed structure pair                        | Address    | Size       | Description                        |
|----------|-------------------------------------------------|------------|------------|------------------------------------|
| 38       | PERI_MS_PPU_FX_FAULT_STRUCT2_MAIN               | 0x40210200 | 0x00000100 | CPUSS Fault Structure #2 main      |
| 39       | PERI_MS_PPU_FX_FAULT_STRUCT3_MAIN               | 0x40210300 | 0x00000100 | CPUSS Fault Structure #3 main      |
| 40       | PERI_MS_PPU_FX_IPC_STRUCT0_IPC                  | 0x40220000 | 0x00000020 | CPUSS IPC Structure #0             |
| 41       | PERI_MS_PPU_FX_IPC_STRUCT1_IPC                  | 0x40220020 | 0x00000020 | CPUSS IPC Structure #1             |
| 42       | PERI_MS_PPU_FX_IPC_STRUCT2_IPC                  | 0x40220040 | 0x00000020 | CPUSS IPC Structure #2             |
| 43       | PERI_MS_PPU_FX_IPC_STRUCT3_IPC                  | 0x40220060 | 0x00000020 | CPUSS IPC Structure #3             |
| 44       | PERI_MS_PPU_FX_IPC_STRUCT4_IPC                  | 0x40220080 | 0x00000020 | CPUSS IPC Structure #4             |
| 45       | PERI_MS_PPU_FX_IPC_STRUCT5_IPC                  | 0x402200A0 | 0x00000020 | CPUSS IPC Structure #5             |
| 46       | PERI_MS_PPU_FX_IPC_STRUCT6_IPC                  | 0x402200C0 | 0x00000020 | CPUSS IPC Structure #6             |
| 47       | PERI_MS_PPU_FX_IPC_STRUCT7_IPC                  | 0x402200E0 | 0x00000020 | CPUSS IPC Structure #7             |
| 48       | PERI_MS_PPU_FX_IPC_INTR_STRUCT0_INTR            | 0x40221000 | 0x00000010 | CPUSS IPC Interrupt Structure #0   |
| 49       | PERI_MS_PPU_FX_IPC_INTR_STRUCT1_INTR            | 0x40221020 | 0x00000010 | CPUSS IPC Interrupt Structure #1   |
| 50       | PERI_MS_PPU_FX_IPC_INTR_STRUCT2_INTR            | 0x40221040 | 0x00000010 | CPUSS IPC Interrupt Structure #2   |
| 51       | PERI_MS_PPU_FX_IPC_INTR_STRUCT3_INTR            | 0x40221060 | 0x00000010 | CPUSS IPC Interrupt Structure #3   |
| 52       | PERI_MS_PPU_FX_IPC_INTR_STRUCT4_INTR            | 0x40221080 | 0x00000010 | CPUSS IPC Interrupt Structure #4   |
| 53       | PERI_MS_PPU_FX_IPC_INTR_STRUCT5_INTR            | 0x402210A0 | 0x00000010 | CPUSS IPC Interrupt Structure #5   |
| 54       | PERI_MS_PPU_FX_IPC_INTR_STRUCT6_INTR            | 0x402210C0 | 0x00000010 | CPUSS IPC Interrupt Structure #6   |
| 55       | PERI_MS_PPU_FX_IPC_INTR_STRUCT7_INTR            | 0x402210E0 | 0x00000010 | CPUSS IPC Interrupt Structure #7   |
| 56       | PERI_MS_PPU_FX_PROT_SMPU_MAIN                   | 0x40230000 | 0x00000040 | Peripheral protection S MPU main   |
| 57       | PERI_MS_PPU_FX_PROT_MPU0_MAIN                   | 0x40234000 | 0x00000004 | Peripheral protection MPU #0 main  |
| 58       | PERI_MS_PPU_FX_PROT_MPU5_MAIN                   | 0x40235400 | 0x00000400 | Peripheral protection MPU #5 main  |
| 59       | PERI_MS_PPU_FX_PROT_MPU6_MAIN                   | 0x40235800 | 0x00000400 | Peripheral protection MPU #6 main  |
| 60       | PERI_MS_PPU_FX_PROT_MPU13_MAIN                  | 0x40237400 | 0x00000004 | Peripheral protection MPU #13 main |
| 61       | PERI_MS_PPU_FX_PROT_MPU14_MAIN                  | 0x40237800 | 0x00000004 | Peripheral protection MPU #14 main |
| 62       | PERI_MS_PPU_FX_PROT_MPU15_MAIN                  | 0x40237C00 | 0x00000400 | Peripheral protection MPU #15 main |
| 63       | PERI_MS_PPU_FX_FLASHC_MAIN                      | 0x40240000 | 0x00000008 | Flash controller main              |
| 64       | PERI_MS_PPU_FX_FLASHC_CMD                       | 0x40240008 | 0x00000004 | Flash controller command           |
| 65       | PERI_MS_PPU_FX_FLASHC_DFT                       | 0x40240200 | 0x00000100 | Flash controller tests             |
| 66       | PERI_MS_PPU_FX_FLASHC_CM0                       | 0x40240400 | 0x00000080 | Flash controller CM0+              |
| 67       | PERI_MS_PPU_FX_FLASHC_CM7_0                     | 0x402404E0 | 0x00000004 | Flash controller CM7_0             |
| 68       | PERI_MS_PPU_FX_FLASHC_CM7_1                     | 0x40240560 | 0x00000004 | Flash controller CM7_1             |
| 69       | PERI_MS_PPU_FX_FLASHC_CRYPT0                    | 0x40240580 | 0x00000004 | Flash controller Crypto            |
| 70       | PERI_MS_PPU_FX_FLASHC_DW0                       | 0x40240600 | 0x00000004 | Flash controller P-DMA0            |
| 71       | PERI_MS_PPU_FX_FLASHC_DW1                       | 0x40240680 | 0x00000004 | Flash controller P-DMA1            |
| 72       | PERI_MS_PPU_FX_FLASHC_DM0                       | 0x40240700 | 0x00000004 | Flash controller M-DMA0            |
| 73       | PERI_MS_PPU_FX_FLASHC_SLOW0                     | 0x40240780 | 0x00000004 | Flash External AHB-Lite Master 0   |
| 74       | PERI_MS_PPU_FX_FLASHC_FlashMgmt <sup>[41]</sup> | 0x4024F000 | 0x00000080 | Flash management                   |
| 75       | PERI_MS_PPU_FX_FLASHC_MainSafety                | 0x4024F400 | 0x00000008 | Flash controller code-flash safety |
| 76       | PERI_MS_PPU_FX_FLASHC_WorkSafety                | 0x4024F500 | 0x00000004 | Flash controller work-flash safety |
| 77       | PERI_MS_PPU_FX_FLASHC_FM                        | 0x4024F000 | 0x00001000 | Flash management                   |
| 78       | PERI_MS_PPU_FX_SRSS_GENERAL                     | 0x40260000 | 0x00000400 | SRSS General                       |

**Note**

41.Fixed PPU is configured inside the Boot and user is not allowed to change the attributes of this PPU.

**Table 22-1 PPU fixed structure pairs** (continued)

| Pair no. | PPU fixed structure pair          | Address    | Size       | Description              |
|----------|-----------------------------------|------------|------------|--------------------------|
| 79       | PERI_MS_PPU_FX_SRSS_MAIN          | 0x40261000 | 0x00001000 | SRSS main                |
| 80       | PERI_MS_PPU_FX_SRSS_SECURE        | 0x40262000 | 0x00002000 | SRSS secure              |
| 81       | PERI_MS_PPU_FX_MCWDT0_CONFIG      | 0x40268000 | 0x00000080 | MCWDT #0 configuration   |
| 82       | PERI_MS_PPU_FX_MCWDT1_CONFIG      | 0x40268100 | 0x00000080 | MCWDT #1 configuration   |
| 83       | PERI_MS_PPU_FX_MCWDT2_CONFIG      | 0x40268200 | 0x00000080 | MCWDT #2 configuration   |
| 84       | PERI_MS_PPU_FX_MCWDT0_MAIN        | 0x40268080 | 0x00000040 | MCWDT #0 main            |
| 85       | PERI_MS_PPU_FX_MCWDT1_MAIN        | 0x40268180 | 0x00000040 | MCWDT #1 main            |
| 86       | PERI_MS_PPU_FX_MCWDT2_MAIN        | 0x40268280 | 0x00000040 | MCWDT #2 main            |
| 87       | PERI_MS_PPU_FX_WDT_CONFIG         | 0x4026C000 | 0x00000020 | System WDT configuration |
| 88       | PERI_MS_PPU_FX_WDT_MAIN           | 0x4026C040 | 0x00000020 | System WDT main          |
| 89       | PERI_MS_PPU_FX_BACKUP_BACKUP      | 0x40270000 | 0x00010000 | SRSS backup              |
| 90       | PERI_MS_PPU_FX_DW0_DW             | 0x40280000 | 0x00000100 | P-DMA0 main              |
| 91       | PERI_MS_PPU_FX_DW1_DW             | 0x40290000 | 0x00000100 | P-DMA1 main              |
| 92       | PERI_MS_PPU_FX_DW0_DW_CRC         | 0x40280100 | 0x00000080 | P-DMA0 CRC               |
| 93       | PERI_MS_PPU_FX_DW1_DW_CRC         | 0x40290100 | 0x00000080 | P-DMA1 CRC               |
| 94       | PERI_MS_PPU_FX_DW0_CH_STRUCT0_CH  | 0x40288000 | 0x00000040 | P-DMA0 Channel #0        |
| 95       | PERI_MS_PPU_FX_DW0_CH_STRUCT1_CH  | 0x40288040 | 0x00000040 | P-DMA0 Channel #1        |
| 96       | PERI_MS_PPU_FX_DW0_CH_STRUCT2_CH  | 0x40288080 | 0x00000040 | P-DMA0 Channel #2        |
| 97       | PERI_MS_PPU_FX_DW0_CH_STRUCT3_CH  | 0x402880C0 | 0x00000040 | P-DMA0 Channel #3        |
| 98       | PERI_MS_PPU_FX_DW0_CH_STRUCT4_CH  | 0x40288100 | 0x00000040 | P-DMA0 Channel #4        |
| 99       | PERI_MS_PPU_FX_DW0_CH_STRUCT5_CH  | 0x40288140 | 0x00000040 | P-DMA0 Channel #5        |
| 100      | PERI_MS_PPU_FX_DW0_CH_STRUCT6_CH  | 0x40288180 | 0x00000040 | P-DMA0 Channel #6        |
| 101      | PERI_MS_PPU_FX_DW0_CH_STRUCT7_CH  | 0x402881C0 | 0x00000040 | P-DMA0 Channel #7        |
| 102      | PERI_MS_PPU_FX_DW0_CH_STRUCT8_CH  | 0x40288200 | 0x00000040 | P-DMA0 Channel #8        |
| 103      | PERI_MS_PPU_FX_DW0_CH_STRUCT9_CH  | 0x40288240 | 0x00000040 | P-DMA0 Channel #9        |
| 104      | PERI_MS_PPU_FX_DW0_CH_STRUCT10_CH | 0x40288280 | 0x00000040 | P-DMA0 Channel #10       |
| 105      | PERI_MS_PPU_FX_DW0_CH_STRUCT11_CH | 0x402882C0 | 0x00000040 | P-DMA0 Channel #11       |
| 106      | PERI_MS_PPU_FX_DW0_CH_STRUCT12_CH | 0x40288300 | 0x00000040 | P-DMA0 Channel #12       |
| 107      | PERI_MS_PPU_FX_DW0_CH_STRUCT13_CH | 0x40288340 | 0x00000040 | P-DMA0 Channel #13       |
| 108      | PERI_MS_PPU_FX_DW0_CH_STRUCT14_CH | 0x40288380 | 0x00000040 | P-DMA0 Channel #14       |
| 109      | PERI_MS_PPU_FX_DW0_CH_STRUCT15_CH | 0x402883C0 | 0x00000040 | P-DMA0 Channel #15       |
| 110      | PERI_MS_PPU_FX_DW0_CH_STRUCT16_CH | 0x40288400 | 0x00000040 | P-DMA0 Channel #16       |
| 111      | PERI_MS_PPU_FX_DW0_CH_STRUCT17_CH | 0x40288440 | 0x00000040 | P-DMA0 Channel #17       |
| 112      | PERI_MS_PPU_FX_DW0_CH_STRUCT18_CH | 0x40288480 | 0x00000040 | P-DMA0 Channel #18       |
| 113      | PERI_MS_PPU_FX_DW0_CH_STRUCT19_CH | 0x402884C0 | 0x00000040 | P-DMA0 Channel #19       |
| 114      | PERI_MS_PPU_FX_DW0_CH_STRUCT20_CH | 0x40288500 | 0x00000040 | P-DMA0 Channel #20       |
| 115      | PERI_MS_PPU_FX_DW0_CH_STRUCT21_CH | 0x40288540 | 0x00000040 | P-DMA0 Channel #21       |
| 116      | PERI_MS_PPU_FX_DW0_CH_STRUCT22_CH | 0x40288580 | 0x00000040 | P-DMA0 Channel #22       |
| 117      | PERI_MS_PPU_FX_DW0_CH_STRUCT23_CH | 0x402885C0 | 0x00000040 | P-DMA0 Channel #23       |
| 118      | PERI_MS_PPU_FX_DW0_CH_STRUCT24_CH | 0x40288600 | 0x00000040 | P-DMA0 Channel #24       |
| 119      | PERI_MS_PPU_FX_DW0_CH_STRUCT25_CH | 0x40288640 | 0x00000040 | P-DMA0 Channel #25       |
| 120      | PERI_MS_PPU_FX_DW0_CH_STRUCT26_CH | 0x40288680 | 0x00000040 | P-DMA0 Channel #26       |
| 121      | PERI_MS_PPU_FX_DW0_CH_STRUCT27_CH | 0x402886C0 | 0x00000040 | P-DMA0 Channel #27       |
| 122      | PERI_MS_PPU_FX_DW0_CH_STRUCT28_CH | 0x40288700 | 0x00000040 | P-DMA0 Channel #28       |
| 123      | PERI_MS_PPU_FX_DW0_CH_STRUCT29_CH | 0x40288740 | 0x00000040 | P-DMA0 Channel #29       |

**Table 22-1 PPU fixed structure pairs** (continued)

| Pair no. | PPU fixed structure pair          | Address    | Size       | Description        |
|----------|-----------------------------------|------------|------------|--------------------|
| 124      | PERI_MS_PPU_FX_DW0_CH_STRUCT30_CH | 0x40288780 | 0x00000040 | P-DMA0 Channel #30 |
| 125      | PERI_MS_PPU_FX_DW0_CH_STRUCT31_CH | 0x402887C0 | 0x00000040 | P-DMA0 Channel #31 |
| 126      | PERI_MS_PPU_FX_DW0_CH_STRUCT32_CH | 0x40288800 | 0x00000040 | P-DMA0 Channel #32 |
| 127      | PERI_MS_PPU_FX_DW0_CH_STRUCT33_CH | 0x40288840 | 0x00000040 | P-DMA0 Channel #33 |
| 128      | PERI_MS_PPU_FX_DW0_CH_STRUCT34_CH | 0x40288880 | 0x00000040 | P-DMA0 Channel #34 |
| 129      | PERI_MS_PPU_FX_DW0_CH_STRUCT35_CH | 0x402888C0 | 0x00000040 | P-DMA0 Channel #35 |
| 130      | PERI_MS_PPU_FX_DW0_CH_STRUCT36_CH | 0x40288900 | 0x00000040 | P-DMA0 Channel #36 |
| 131      | PERI_MS_PPU_FX_DW0_CH_STRUCT37_CH | 0x40288940 | 0x00000040 | P-DMA0 Channel #37 |
| 132      | PERI_MS_PPU_FX_DW0_CH_STRUCT38_CH | 0x40288980 | 0x00000040 | P-DMA0 Channel #38 |
| 133      | PERI_MS_PPU_FX_DW0_CH_STRUCT39_CH | 0x402889C0 | 0x00000040 | P-DMA0 Channel #39 |
| 134      | PERI_MS_PPU_FX_DW0_CH_STRUCT40_CH | 0x40288A00 | 0x00000040 | P-DMA0 Channel #40 |
| 135      | PERI_MS_PPU_FX_DW0_CH_STRUCT41_CH | 0x40288A40 | 0x00000040 | P-DMA0 Channel #41 |
| 136      | PERI_MS_PPU_FX_DW0_CH_STRUCT42_CH | 0x40288A80 | 0x00000040 | P-DMA0 Channel #42 |
| 137      | PERI_MS_PPU_FX_DW0_CH_STRUCT43_CH | 0x40288AC0 | 0x00000040 | P-DMA0 Channel #43 |
| 138      | PERI_MS_PPU_FX_DW0_CH_STRUCT44_CH | 0x40288B00 | 0x00000040 | P-DMA0 Channel #44 |
| 139      | PERI_MS_PPU_FX_DW0_CH_STRUCT45_CH | 0x40288B40 | 0x00000040 | P-DMA0 Channel #45 |
| 140      | PERI_MS_PPU_FX_DW0_CH_STRUCT46_CH | 0x40288B80 | 0x00000040 | P-DMA0 Channel #46 |
| 141      | PERI_MS_PPU_FX_DW0_CH_STRUCT47_CH | 0x40288BC0 | 0x00000040 | P-DMA0 Channel #47 |
| 142      | PERI_MS_PPU_FX_DW0_CH_STRUCT48_CH | 0x40288C00 | 0x00000040 | P-DMA0 Channel #48 |
| 143      | PERI_MS_PPU_FX_DW0_CH_STRUCT49_CH | 0x40288C40 | 0x00000040 | P-DMA0 Channel #49 |
| 144      | PERI_MS_PPU_FX_DW0_CH_STRUCT50_CH | 0x40288C80 | 0x00000040 | P-DMA0 Channel #50 |
| 145      | PERI_MS_PPU_FX_DW0_CH_STRUCT51_CH | 0x40288CC0 | 0x00000040 | P-DMA0 Channel #51 |
| 146      | PERI_MS_PPU_FX_DW0_CH_STRUCT52_CH | 0x40288D00 | 0x00000040 | P-DMA0 Channel #52 |
| 147      | PERI_MS_PPU_FX_DW0_CH_STRUCT53_CH | 0x40288D40 | 0x00000040 | P-DMA0 Channel #53 |
| 148      | PERI_MS_PPU_FX_DW0_CH_STRUCT54_CH | 0x40288D80 | 0x00000040 | P-DMA0 Channel #54 |
| 149      | PERI_MS_PPU_FX_DW0_CH_STRUCT55_CH | 0x40288DC0 | 0x00000040 | P-DMA0 Channel #55 |
| 150      | PERI_MS_PPU_FX_DW0_CH_STRUCT56_CH | 0x40288E00 | 0x00000040 | P-DMA0 Channel #56 |
| 151      | PERI_MS_PPU_FX_DW0_CH_STRUCT57_CH | 0x40288E40 | 0x00000040 | P-DMA0 Channel #57 |
| 152      | PERI_MS_PPU_FX_DW0_CH_STRUCT58_CH | 0x40288E80 | 0x00000040 | P-DMA0 Channel #58 |
| 153      | PERI_MS_PPU_FX_DW0_CH_STRUCT59_CH | 0x40288EC0 | 0x00000040 | P-DMA0 Channel #59 |
| 154      | PERI_MS_PPU_FX_DW0_CH_STRUCT60_CH | 0x40288F00 | 0x00000040 | P-DMA0 Channel #60 |
| 155      | PERI_MS_PPU_FX_DW0_CH_STRUCT61_CH | 0x40288F40 | 0x00000040 | P-DMA0 Channel #61 |
| 156      | PERI_MS_PPU_FX_DW0_CH_STRUCT62_CH | 0x40288F80 | 0x00000040 | P-DMA0 Channel #62 |
| 157      | PERI_MS_PPU_FX_DW0_CH_STRUCT63_CH | 0x40288FC0 | 0x00000040 | P-DMA0 Channel #63 |
| 158      | PERI_MS_PPU_FX_DW0_CH_STRUCT64_CH | 0x40289000 | 0x00000040 | P-DMA0 Channel #64 |
| 159      | PERI_MS_PPU_FX_DW0_CH_STRUCT65_CH | 0x40289040 | 0x00000040 | P-DMA0 Channel #65 |
| 160      | PERI_MS_PPU_FX_DW0_CH_STRUCT66_CH | 0x40289080 | 0x00000040 | P-DMA0 Channel #66 |
| 161      | PERI_MS_PPU_FX_DW0_CH_STRUCT67_CH | 0x402890C0 | 0x00000040 | P-DMA0 Channel #67 |
| 162      | PERI_MS_PPU_FX_DW0_CH_STRUCT68_CH | 0x40289100 | 0x00000040 | P-DMA0 Channel #68 |
| 163      | PERI_MS_PPU_FX_DW0_CH_STRUCT69_CH | 0x40289140 | 0x00000040 | P-DMA0 Channel #69 |
| 164      | PERI_MS_PPU_FX_DW0_CH_STRUCT70_CH | 0x40289180 | 0x00000040 | P-DMA0 Channel #70 |
| 165      | PERI_MS_PPU_FX_DW0_CH_STRUCT71_CH | 0x402891C0 | 0x00000040 | P-DMA0 Channel #71 |
| 166      | PERI_MS_PPU_FX_DW0_CH_STRUCT72_CH | 0x40289200 | 0x00000040 | P-DMA0 Channel #72 |
| 167      | PERI_MS_PPU_FX_DW0_CH_STRUCT73_CH | 0x40289240 | 0x00000040 | P-DMA0 Channel #73 |
| 168      | PERI_MS_PPU_FX_DW0_CH_STRUCT74_CH | 0x40289280 | 0x00000040 | P-DMA0 Channel #74 |

**Table 22-1 PPU fixed structure pairs** (continued)

| Pair no. | PPU fixed structure pair          | Address    | Size       | Description        |
|----------|-----------------------------------|------------|------------|--------------------|
| 169      | PERI_MS_PPU_FX_DW0_CH_STRUCT75_CH | 0x402892C0 | 0x00000040 | P-DMA0 Channel #75 |
| 170      | PERI_MS_PPU_FX_DW0_CH_STRUCT76_CH | 0x40289300 | 0x00000040 | P-DMA0 Channel #76 |
| 171      | PERI_MS_PPU_FX_DW0_CH_STRUCT77_CH | 0x40289340 | 0x00000040 | P-DMA0 Channel #77 |
| 172      | PERI_MS_PPU_FX_DW0_CH_STRUCT78_CH | 0x40289380 | 0x00000040 | P-DMA0 Channel #78 |
| 173      | PERI_MS_PPU_FX_DW0_CH_STRUCT79_CH | 0x402893C0 | 0x00000040 | P-DMA0 Channel #79 |
| 174      | PERI_MS_PPU_FX_DW0_CH_STRUCT80_CH | 0x40289400 | 0x00000040 | P-DMA0 Channel #80 |
| 175      | PERI_MS_PPU_FX_DW0_CH_STRUCT81_CH | 0x40289440 | 0x00000040 | P-DMA0 Channel #81 |
| 176      | PERI_MS_PPU_FX_DW0_CH_STRUCT82_CH | 0x40289480 | 0x00000040 | P-DMA0 Channel #82 |
| 177      | PERI_MS_PPU_FX_DW0_CH_STRUCT83_CH | 0x402894C0 | 0x00000040 | P-DMA0 Channel #83 |
| 178      | PERI_MS_PPU_FX_DW0_CH_STRUCT84_CH | 0x40289500 | 0x00000040 | P-DMA0 Channel #84 |
| 179      | PERI_MS_PPU_FX_DW0_CH_STRUCT85_CH | 0x40289540 | 0x00000040 | P-DMA0 Channel #85 |
| 180      | PERI_MS_PPU_FX_DW0_CH_STRUCT86_CH | 0x40289580 | 0x00000040 | P-DMA0 Channel #86 |
| 181      | PERI_MS_PPU_FX_DW0_CH_STRUCT87_CH | 0x402895C0 | 0x00000040 | P-DMA0 Channel #87 |
| 182      | PERI_MS_PPU_FX_DW0_CH_STRUCT88_CH | 0x40289600 | 0x00000040 | P-DMA0 Channel #88 |
| 183      | PERI_MS_PPU_FX_DW0_CH_STRUCT89_CH | 0x40289640 | 0x00000040 | P-DMA0 Channel #89 |
| 184      | PERI_MS_PPU_FX_DW0_CH_STRUCT90_CH | 0x40289680 | 0x00000040 | P-DMA0 Channel #90 |
| 185      | PERI_MS_PPU_FX_DW0_CH_STRUCT91_CH | 0x402896C0 | 0x00000040 | P-DMA0 Channel #91 |
| 186      | PERI_MS_PPU_FX_DW0_CH_STRUCT92_CH | 0x40289700 | 0x00000040 | P-DMA0 Channel #92 |
| 187      | PERI_MS_PPU_FX_DW0_CH_STRUCT93_CH | 0x40289740 | 0x00000040 | P-DMA0 Channel #93 |
| 188      | PERI_MS_PPU_FX_DW0_CH_STRUCT94_CH | 0x40289780 | 0x00000040 | P-DMA0 Channel #94 |
| 189      | PERI_MS_PPU_FX_DW0_CH_STRUCT95_CH | 0x402897C0 | 0x00000040 | P-DMA0 Channel #95 |
| 190      | PERI_MS_PPU_FX_DW0_CH_STRUCT96_CH | 0x40289800 | 0x00000040 | P-DMA0 Channel #96 |
| 191      | PERI_MS_PPU_FX_DW0_CH_STRUCT97_CH | 0x40289840 | 0x00000040 | P-DMA0 Channel #97 |
| 192      | PERI_MS_PPU_FX_DW0_CH_STRUCT98_CH | 0x40289880 | 0x00000040 | P-DMA0 Channel #98 |
| 193      | PERI_MS_PPU_FX_DW0_CH_STRUCT99_CH | 0x402898C0 | 0x00000040 | P-DMA0 Channel #99 |
| 194      | PERI_MS_PPU_FX_DW1_CH_STRUCT0_CH  | 0x40298000 | 0x00000040 | P-DMA1 Channel #0  |
| 195      | PERI_MS_PPU_FX_DW1_CH_STRUCT1_CH  | 0x40298040 | 0x00000040 | P-DMA1 Channel #1  |
| 196      | PERI_MS_PPU_FX_DW1_CH_STRUCT2_CH  | 0x40298080 | 0x00000040 | P-DMA1 Channel #2  |
| 197      | PERI_MS_PPU_FX_DW1_CH_STRUCT3_CH  | 0x402980C0 | 0x00000040 | P-DMA1 Channel #3  |
| 198      | PERI_MS_PPU_FX_DW1_CH_STRUCT4_CH  | 0x40298100 | 0x00000040 | P-DMA1 Channel #4  |
| 199      | PERI_MS_PPU_FX_DW1_CH_STRUCT5_CH  | 0x40298140 | 0x00000040 | P-DMA1 Channel #5  |
| 200      | PERI_MS_PPU_FX_DW1_CH_STRUCT6_CH  | 0x40298180 | 0x00000040 | P-DMA1 Channel #6  |
| 201      | PERI_MS_PPU_FX_DW1_CH_STRUCT7_CH  | 0x402981C0 | 0x00000040 | P-DMA1 Channel #7  |
| 202      | PERI_MS_PPU_FX_DW1_CH_STRUCT8_CH  | 0x40298200 | 0x00000040 | P-DMA1 Channel #8  |
| 203      | PERI_MS_PPU_FX_DW1_CH_STRUCT9_CH  | 0x40298240 | 0x00000040 | P-DMA1 Channel #9  |
| 204      | PERI_MS_PPU_FX_DW1_CH_STRUCT10_CH | 0x40298280 | 0x00000040 | P-DMA1 Channel #10 |
| 205      | PERI_MS_PPU_FX_DW1_CH_STRUCT11_CH | 0x402982C0 | 0x00000040 | P-DMA1 Channel #11 |
| 206      | PERI_MS_PPU_FX_DW1_CH_STRUCT12_CH | 0x40298300 | 0x00000040 | P-DMA1 Channel #12 |
| 207      | PERI_MS_PPU_FX_DW1_CH_STRUCT13_CH | 0x40298340 | 0x00000040 | P-DMA1 Channel #13 |
| 208      | PERI_MS_PPU_FX_DW1_CH_STRUCT14_CH | 0x40298380 | 0x00000040 | P-DMA1 Channel #14 |
| 209      | PERI_MS_PPU_FX_DW1_CH_STRUCT15_CH | 0x402983C0 | 0x00000040 | P-DMA1 Channel #15 |
| 210      | PERI_MS_PPU_FX_DW1_CH_STRUCT16_CH | 0x40298400 | 0x00000040 | P-DMA1 Channel #16 |
| 211      | PERI_MS_PPU_FX_DW1_CH_STRUCT17_CH | 0x40298440 | 0x00000040 | P-DMA1 Channel #17 |
| 212      | PERI_MS_PPU_FX_DW1_CH_STRUCT18_CH | 0x40298480 | 0x00000040 | P-DMA1 Channel #18 |
| 213      | PERI_MS_PPU_FX_DW1_CH_STRUCT19_CH | 0x402984C0 | 0x00000040 | P-DMA1 Channel #19 |

**Table 22-1 PPU fixed structure pairs** (continued)

| Pair no. | PPU fixed structure pair          | Address    | Size       | Description        |
|----------|-----------------------------------|------------|------------|--------------------|
| 214      | PERI_MS_PPU_FX_DW1_CH_STRUCT20_CH | 0x40298500 | 0x00000040 | P-DMA1 Channel #20 |
| 215      | PERI_MS_PPU_FX_DW1_CH_STRUCT21_CH | 0x40298540 | 0x00000040 | P-DMA1 Channel #21 |
| 216      | PERI_MS_PPU_FX_DW1_CH_STRUCT22_CH | 0x40298580 | 0x00000040 | P-DMA1 Channel #22 |
| 217      | PERI_MS_PPU_FX_DW1_CH_STRUCT23_CH | 0x402985C0 | 0x00000040 | P-DMA1 Channel #23 |
| 218      | PERI_MS_PPU_FX_DW1_CH_STRUCT24_CH | 0x40298600 | 0x00000040 | P-DMA1 Channel #24 |
| 219      | PERI_MS_PPU_FX_DW1_CH_STRUCT25_CH | 0x40298640 | 0x00000040 | P-DMA1 Channel #25 |
| 220      | PERI_MS_PPU_FX_DW1_CH_STRUCT26_CH | 0x40298680 | 0x00000040 | P-DMA1 Channel #26 |
| 221      | PERI_MS_PPU_FX_DW1_CH_STRUCT27_CH | 0x402986C0 | 0x00000040 | P-DMA1 Channel #27 |
| 222      | PERI_MS_PPU_FX_DW1_CH_STRUCT28_CH | 0x40298700 | 0x00000040 | P-DMA1 Channel #28 |
| 223      | PERI_MS_PPU_FX_DW1_CH_STRUCT29_CH | 0x40298740 | 0x00000040 | P-DMA1 Channel #29 |
| 224      | PERI_MS_PPU_FX_DW1_CH_STRUCT30_CH | 0x40298780 | 0x00000040 | P-DMA1 Channel #30 |
| 225      | PERI_MS_PPU_FX_DW1_CH_STRUCT31_CH | 0x402987C0 | 0x00000040 | P-DMA1 Channel #31 |
| 226      | PERI_MS_PPU_FX_DW1_CH_STRUCT32_CH | 0x40298800 | 0x00000040 | P-DMA1 Channel #32 |
| 227      | PERI_MS_PPU_FX_DW1_CH_STRUCT33_CH | 0x40298840 | 0x00000040 | P-DMA1 Channel #33 |
| 228      | PERI_MS_PPU_FX_DW1_CH_STRUCT34_CH | 0x40298880 | 0x00000040 | P-DMA1 Channel #34 |
| 229      | PERI_MS_PPU_FX_DW1_CH_STRUCT35_CH | 0x402988C0 | 0x00000040 | P-DMA1 Channel #35 |
| 230      | PERI_MS_PPU_FX_DW1_CH_STRUCT36_CH | 0x40298900 | 0x00000040 | P-DMA1 Channel #36 |
| 231      | PERI_MS_PPU_FX_DW1_CH_STRUCT37_CH | 0x40298940 | 0x00000040 | P-DMA1 Channel #37 |
| 232      | PERI_MS_PPU_FX_DW1_CH_STRUCT38_CH | 0x40298980 | 0x00000040 | P-DMA1 Channel #38 |
| 233      | PERI_MS_PPU_FX_DW1_CH_STRUCT39_CH | 0x402989C0 | 0x00000040 | P-DMA1 Channel #39 |
| 234      | PERI_MS_PPU_FX_DW1_CH_STRUCT40_CH | 0x40298A00 | 0x00000040 | P-DMA1 Channel #40 |
| 235      | PERI_MS_PPU_FX_DW1_CH_STRUCT41_CH | 0x40298A40 | 0x00000040 | P-DMA1 Channel #41 |
| 236      | PERI_MS_PPU_FX_DW1_CH_STRUCT42_CH | 0x40298A80 | 0x00000040 | P-DMA1 Channel #42 |
| 237      | PERI_MS_PPU_FX_DW1_CH_STRUCT43_CH | 0x40298AC0 | 0x00000040 | P-DMA1 Channel #43 |
| 238      | PERI_MS_PPU_FX_DW1_CH_STRUCT44_CH | 0x40298B00 | 0x00000040 | P-DMA1 Channel #44 |
| 239      | PERI_MS_PPU_FX_DW1_CH_STRUCT45_CH | 0x40298B40 | 0x00000040 | P-DMA1 Channel #45 |
| 240      | PERI_MS_PPU_FX_DW1_CH_STRUCT46_CH | 0x40298B80 | 0x00000040 | P-DMA1 Channel #46 |
| 241      | PERI_MS_PPU_FX_DW1_CH_STRUCT47_CH | 0x40298BC0 | 0x00000040 | P-DMA1 Channel #47 |
| 242      | PERI_MS_PPU_FX_DW1_CH_STRUCT48_CH | 0x40298C00 | 0x00000040 | P-DMA1 Channel #48 |
| 243      | PERI_MS_PPU_FX_DW1_CH_STRUCT49_CH | 0x40298C40 | 0x00000040 | P-DMA1 Channel #49 |
| 244      | PERI_MS_PPU_FX_DW1_CH_STRUCT50_CH | 0x40298C80 | 0x00000040 | P-DMA1 Channel #50 |
| 245      | PERI_MS_PPU_FX_DW1_CH_STRUCT51_CH | 0x40298CC0 | 0x00000040 | P-DMA1 Channel #51 |
| 246      | PERI_MS_PPU_FX_DW1_CH_STRUCT52_CH | 0x40298D00 | 0x00000040 | P-DMA1 Channel #52 |
| 247      | PERI_MS_PPU_FX_DW1_CH_STRUCT53_CH | 0x40298D40 | 0x00000040 | P-DMA1 Channel #53 |
| 248      | PERI_MS_PPU_FX_DW1_CH_STRUCT54_CH | 0x40298D80 | 0x00000040 | P-DMA1 Channel #54 |
| 249      | PERI_MS_PPU_FX_DW1_CH_STRUCT55_CH | 0x40298DC0 | 0x00000040 | P-DMA1 Channel #55 |
| 250      | PERI_MS_PPU_FX_DW1_CH_STRUCT56_CH | 0x40298E00 | 0x00000040 | P-DMA1 Channel #56 |
| 251      | PERI_MS_PPU_FX_DW1_CH_STRUCT57_CH | 0x40298E40 | 0x00000040 | P-DMA1 Channel #57 |
| 252      | PERI_MS_PPU_FX_DMACH0_TOP         | 0x402A0000 | 0x00000010 | M-DMA0 main        |
| 253      | PERI_MS_PPU_FX_DMACH0_CH          | 0x402A1000 | 0x00000100 | M-DMA0 Channel #0  |
| 254      | PERI_MS_PPU_FX_DMACH1_CH          | 0x402A1100 | 0x00000100 | M-DMA0 Channel #1  |
| 255      | PERI_MS_PPU_FX_DMACH2_CH          | 0x402A1200 | 0x00000100 | M-DMA0 Channel #2  |
| 256      | PERI_MS_PPU_FX_DMACH3_CH          | 0x402A1300 | 0x00000100 | M-DMA0 Channel #3  |
| 257      | PERI_MS_PPU_FX_DMACH4_CH          | 0x402A1400 | 0x00000100 | M-DMA0 Channel #4  |
| 258      | PERI_MS_PPU_FX_DMACH5_CH          | 0x402A1500 | 0x00000100 | M-DMA0 Channel #5  |

**Table 22-1 PPU fixed structure pairs** (continued)

| Pair no. | PPU fixed structure pair       | Address    | Size       | Description              |
|----------|--------------------------------|------------|------------|--------------------------|
| 259      | PERI_MS_PPU_FX_DMACH6_CH       | 0x402A1600 | 0x00000100 | M-DMA0 Channel #6        |
| 260      | PERI_MS_PPU_FX_DMACH7_CH       | 0x402A1700 | 0x00000100 | M-DMA0 Channel #7        |
| 261      | PERI_MS_PPU_FX_EFUSE_CTL       | 0x402C0000 | 0x00000200 | EFUSE control            |
| 262      | PERI_MS_PPU_FX_EFUSE_DATA      | 0x402C0800 | 0x00000200 | EFUSE data               |
| 263      | PERI_MS_PPU_FX_BIST            | 0x402F0000 | 0x00001000 | Built-in self test       |
| 264      | PERI_MS_PPU_FX_HSIOM_PRT0_PRT  | 0x40300000 | 0x00000008 | HSIOM Port #0            |
| 265      | PERI_MS_PPU_FX_HSIOM_PRT1_PRT  | 0x40300010 | 0x00000008 | HSIOM Port #1            |
| 266      | PERI_MS_PPU_FX_HSIOM_PRT2_PRT  | 0x40300020 | 0x00000008 | HSIOM Port #2            |
| 267      | PERI_MS_PPU_FX_HSIOM_PRT3_PRT  | 0x40300030 | 0x00000008 | HSIOM Port #3            |
| 268      | PERI_MS_PPU_FX_HSIOM_PRT4_PRT  | 0x40300040 | 0x00000008 | HSIOM Port #4            |
| 269      | PERI_MS_PPU_FX_HSIOM_PRT5_PRT  | 0x40300050 | 0x00000008 | HSIOM Port #5            |
| 270      | PERI_MS_PPU_FX_HSIOM_PRT6_PRT  | 0x40300060 | 0x00000008 | HSIOM Port #6            |
| 271      | PERI_MS_PPU_FX_HSIOM_PRT7_PRT  | 0x40300070 | 0x00000008 | HSIOM Port #7            |
| 272      | PERI_MS_PPU_FX_HSIOM_PRT8_PRT  | 0x40300080 | 0x00000008 | HSIOM Port #8            |
| 273      | PERI_MS_PPU_FX_HSIOM_PRT9_PRT  | 0x40300090 | 0x00000008 | HSIOM Port #9            |
| 274      | PERI_MS_PPU_FX_HSIOM_PRT10_PRT | 0x403000A0 | 0x00000008 | HSIOM Port #10           |
| 275      | PERI_MS_PPU_FX_HSIOM_PRT11_PRT | 0x403000B0 | 0x00000008 | HSIOM Port #11           |
| 276      | PERI_MS_PPU_FX_HSIOM_PRT12_PRT | 0x403000C0 | 0x00000008 | HSIOM Port #12           |
| 277      | PERI_MS_PPU_FX_HSIOM_PRT13_PRT | 0x403000D0 | 0x00000008 | HSIOM Port #13           |
| 278      | PERI_MS_PPU_FX_HSIOM_PRT14_PRT | 0x403000E0 | 0x00000008 | HSIOM Port #14           |
| 279      | PERI_MS_PPU_FX_HSIOM_PRT15_PRT | 0x403000F0 | 0x00000008 | HSIOM Port #15           |
| 280      | PERI_MS_PPU_FX_HSIOM_PRT16_PRT | 0x40300100 | 0x00000008 | HSIOM Port #16           |
| 281      | PERI_MS_PPU_FX_HSIOM_PRT17_PRT | 0x40300110 | 0x00000008 | HSIOM Port #17           |
| 282      | PERI_MS_PPU_FX_HSIOM_PRT18_PRT | 0x40300120 | 0x00000008 | HSIOM Port #18           |
| 283      | PERI_MS_PPU_FX_HSIOM_PRT19_PRT | 0x40300130 | 0x00000008 | HSIOM Port #19           |
| 284      | PERI_MS_PPU_FX_HSIOM_PRT20_PRT | 0x40300140 | 0x00000008 | HSIOM Port #20           |
| 285      | PERI_MS_PPU_FX_HSIOM_PRT21_PRT | 0x40300150 | 0x00000008 | HSIOM Port #21           |
| 286      | PERI_MS_PPU_FX_HSIOM_PRT22_PRT | 0x40300160 | 0x00000008 | HSIOM Port #22           |
| 287      | PERI_MS_PPU_FX_HSIOM_PRT23_PRT | 0x40300170 | 0x00000008 | HSIOM Port #23           |
| 288      | PERI_MS_PPU_FX_HSIOM_PRT24_PRT | 0x40300180 | 0x00000008 | HSIOM Port #24           |
| 289      | PERI_MS_PPU_FX_HSIOM_PRT25_PRT | 0x40300190 | 0x00000008 | HSIOM Port #25           |
| 290      | PERI_MS_PPU_FX_HSIOM_PRT26_PRT | 0x403001A0 | 0x00000008 | HSIOM Port #26           |
| 291      | PERI_MS_PPU_FX_HSIOM_PRT27_PRT | 0x403001B0 | 0x00000008 | HSIOM Port #27           |
| 292      | PERI_MS_PPU_FX_HSIOM_PRT28_PRT | 0x403001C0 | 0x00000008 | HSIOM Port #28           |
| 293      | PERI_MS_PPU_FX_HSIOM_PRT29_PRT | 0x403001D0 | 0x00000008 | HSIOM Port #29           |
| 294      | PERI_MS_PPU_FX_HSIOM_PRT30_PRT | 0x403001E0 | 0x00000008 | HSIOM Port #30           |
| 295      | PERI_MS_PPU_FX_HSIOM_PRT31_PRT | 0x403001F0 | 0x00000008 | HSIOM Port #31           |
| 296      | PERI_MS_PPU_FX_HSIOM_PRT32_PRT | 0x40300200 | 0x00000008 | HSIOM Port #32           |
| 297      | PERI_MS_PPU_FX_HSIOM_AMUX      | 0x40302000 | 0x00000010 | HSIOM Analog multiplexer |
| 298      | PERI_MS_PPU_FX_HSIOM_MON       | 0x40302200 | 0x00000010 | HSIOM monitor            |
| 299      | PERI_MS_PPU_FX_HSIOM_ALTJTAG   | 0x40302240 | 0x00000004 | HSIOM Alternate JTAG     |
| 300      | PERI_MS_PPU_FX_GPIO_PRT0_PRT   | 0x40310000 | 0x00000040 | GPIO_ENH Port #0         |
| 301      | PERI_MS_PPU_FX_GPIO_PRT1_PRT   | 0x40310080 | 0x00000040 | GPIO_STD Port #1         |
| 302      | PERI_MS_PPU_FX_GPIO_PRT2_PRT   | 0x40310100 | 0x00000040 | GPIO_STD Port #2         |
| 303      | PERI_MS_PPU_FX_GPIO_PRT3_PRT   | 0x40310180 | 0x00000040 | GPIO_STD Port #3         |

**Table 22-1 PPU fixed structure pairs** (continued)

| Pair no. | PPU fixed structure pair      | Address    | Size       | Description                     |
|----------|-------------------------------|------------|------------|---------------------------------|
| 304      | PERI_MS_PPU_FX_GPIO_PRT4_PRT  | 0x40310200 | 0x00000040 | GPIO_STD Port #4                |
| 305      | PERI_MS_PPU_FX_GPIO_PRT5_PRT  | 0x40310280 | 0x00000040 | GPIO_STD Port #5                |
| 306      | PERI_MS_PPU_FX_GPIO_PRT6_PRT  | 0x40310300 | 0x00000040 | GPIO_STD Port #6                |
| 307      | PERI_MS_PPU_FX_GPIO_PRT7_PRT  | 0x40310380 | 0x00000040 | GPIO_STD Port #7                |
| 308      | PERI_MS_PPU_FX_GPIO_PRT8_PRT  | 0x40310400 | 0x00000040 | GPIO_STD Port #8                |
| 309      | PERI_MS_PPU_FX_GPIO_PRT9_PRT  | 0x40310480 | 0x00000040 | GPIO_STD Port #9                |
| 310      | PERI_MS_PPU_FX_GPIO_PRT10_PRT | 0x40310500 | 0x00000040 | GPIO_STD Port #10               |
| 311      | PERI_MS_PPU_FX_GPIO_PRT11_PRT | 0x40310580 | 0x00000040 | GPIO_STD Port #11               |
| 312      | PERI_MS_PPU_FX_GPIO_PRT12_PRT | 0x40310600 | 0x00000040 | GPIO_STD Port #12               |
| 313      | PERI_MS_PPU_FX_GPIO_PRT13_PRT | 0x40310680 | 0x00000040 | GPIO_STD Port #13               |
| 314      | PERI_MS_PPU_FX_GPIO_PRT14_PRT | 0x40310700 | 0x00000040 | GPIO_STD Port #14               |
| 315      | PERI_MS_PPU_FX_GPIO_PRT15_PRT | 0x40310780 | 0x00000040 | GPIO_STD Port #15               |
| 316      | PERI_MS_PPU_FX_GPIO_PRT16_PRT | 0x40310800 | 0x00000040 | GPIO_STD Port #16               |
| 317      | PERI_MS_PPU_FX_GPIO_PRT17_PRT | 0x40310880 | 0x00000040 | GPIO_STD Port #17               |
| 318      | PERI_MS_PPU_FX_GPIO_PRT18_PRT | 0x40310900 | 0x00000040 | GPIO_STD Port #18               |
| 319      | PERI_MS_PPU_FX_GPIO_PRT19_PRT | 0x40310980 | 0x00000040 | GPIO_STD Port #19               |
| 320      | PERI_MS_PPU_FX_GPIO_PRT20_PRT | 0x40310A00 | 0x00000040 | GPIO_STD Port #20               |
| 321      | PERI_MS_PPU_FX_GPIO_PRT21_PRT | 0x40310A80 | 0x00000040 | GPIO_STD Port #21               |
| 322      | PERI_MS_PPU_FX_GPIO_PRT22_PRT | 0x40310B00 | 0x00000040 | GPIO_STD Port #22               |
| 323      | PERI_MS_PPU_FX_GPIO_PRT23_PRT | 0x40310B80 | 0x00000040 | GPIO_STD Port #23               |
| 324      | PERI_MS_PPU_FX_GPIO_PRT24_PRT | 0x40310C00 | 0x00000040 | HSIO_STD Port #24               |
| 325      | PERI_MS_PPU_FX_GPIO_PRT25_PRT | 0x40310C80 | 0x00000040 | HSIO_STD Port #25               |
| 326      | PERI_MS_PPU_FX_GPIO_PRT26_PRT | 0x40310D00 | 0x00000040 | HSIO_STD Port #26               |
| 327      | PERI_MS_PPU_FX_GPIO_PRT27_PRT | 0x40310D80 | 0x00000040 | HSIO_STD Port #27               |
| 328      | PERI_MS_PPU_FX_GPIO_PRT28_PRT | 0x40310E00 | 0x00000040 | GPIO_STD Port #28               |
| 329      | PERI_MS_PPU_FX_GPIO_PRT29_PRT | 0x40310E80 | 0x00000040 | GPIO_STD Port #29               |
| 330      | PERI_MS_PPU_FX_GPIO_PRT30_PRT | 0x40310F00 | 0x00000040 | GPIO_STD Port #30               |
| 331      | PERI_MS_PPU_FX_GPIO_PRT31_PRT | 0x40310F80 | 0x00000040 | GPIO_STD Port #31               |
| 332      | PERI_MS_PPU_FX_GPIO_PRT32_PRT | 0x40311000 | 0x00000040 | GPIO_STD Port #32               |
| 333      | PERI_MS_PPU_FX_GPIO_PRT0_CFG  | 0x40310040 | 0x00000020 | GPIO_ENH Port #0 configuration  |
| 334      | PERI_MS_PPU_FX_GPIO_PRT1_CFG  | 0x403100C0 | 0x00000020 | GPIO_STD Port #1 configuration  |
| 335      | PERI_MS_PPU_FX_GPIO_PRT2_CFG  | 0x40310140 | 0x00000020 | GPIO_STD Port #2 configuration  |
| 336      | PERI_MS_PPU_FX_GPIO_PRT3_CFG  | 0x403101C0 | 0x00000020 | GPIO_STD Port #3 configuration  |
| 337      | PERI_MS_PPU_FX_GPIO_PRT4_CFG  | 0x40310240 | 0x00000020 | GPIO_STD Port #4 configuration  |
| 338      | PERI_MS_PPU_FX_GPIO_PRT5_CFG  | 0x403102C0 | 0x00000020 | GPIO_STD Port #5 configuration  |
| 339      | PERI_MS_PPU_FX_GPIO_PRT6_CFG  | 0x40310340 | 0x00000020 | GPIO_STD Port #6 configuration  |
| 340      | PERI_MS_PPU_FX_GPIO_PRT7_CFG  | 0x403103C0 | 0x00000020 | GPIO_STD Port #7 configuration  |
| 341      | PERI_MS_PPU_FX_GPIO_PRT8_CFG  | 0x40310440 | 0x00000020 | GPIO_STD Port #8 configuration  |
| 342      | PERI_MS_PPU_FX_GPIO_PRT9_CFG  | 0x403104C0 | 0x00000020 | GPIO_STD Port #9 configuration  |
| 343      | PERI_MS_PPU_FX_GPIO_PRT10_CFG | 0x40310540 | 0x00000020 | GPIO_STD Port #10 configuration |
| 344      | PERI_MS_PPU_FX_GPIO_PRT11_CFG | 0x403105C0 | 0x00000020 | GPIO_STD Port #11 configuration |
| 345      | PERI_MS_PPU_FX_GPIO_PRT12_CFG | 0x40310640 | 0x00000020 | GPIO_STD Port #12 configuration |
| 346      | PERI_MS_PPU_FX_GPIO_PRT13_CFG | 0x403106C0 | 0x00000020 | GPIO_STD Port #13 configuration |
| 347      | PERI_MS_PPU_FX_GPIO_PRT14_CFG | 0x40310740 | 0x00000020 | GPIO_STD Port #14 configuration |
| 348      | PERI_MS_PPU_FX_GPIO_PRT15_CFG | 0x403107C0 | 0x00000020 | GPIO_STD Port #15 configuration |

**Table 22-1 PPU fixed structure pairs** (continued)

| Pair no. | PPU fixed structure pair         | Address    | Size       | Description                     |
|----------|----------------------------------|------------|------------|---------------------------------|
| 349      | PERI_MS_PPU_FX_GPIO_PRT16_CFG    | 0x40310840 | 0x00000020 | GPIO_STD Port #16 configuration |
| 350      | PERI_MS_PPU_FX_GPIO_PRT17_CFG    | 0x403108C0 | 0x00000020 | GPIO_STD Port #17 configuration |
| 351      | PERI_MS_PPU_FX_GPIO_PRT18_CFG    | 0x40310940 | 0x00000020 | GPIO_STD Port #18 configuration |
| 352      | PERI_MS_PPU_FX_GPIO_PRT19_CFG    | 0x403109C0 | 0x00000020 | GPIO_STD Port #19 configuration |
| 353      | PERI_MS_PPU_FX_GPIO_PRT20_CFG    | 0x40310A40 | 0x00000020 | GPIO_STD Port #20 configuration |
| 354      | PERI_MS_PPU_FX_GPIO_PRT21_CFG    | 0x40310AC0 | 0x00000020 | GPIO_STD Port #21 configuration |
| 355      | PERI_MS_PPU_FX_GPIO_PRT22_CFG    | 0x40310B40 | 0x00000020 | GPIO_STD Port #22 configuration |
| 356      | PERI_MS_PPU_FX_GPIO_PRT23_CFG    | 0x40310BC0 | 0x00000020 | GPIO_STD Port #23 configuration |
| 357      | PERI_MS_PPU_FX_GPIO_PRT24_CFG    | 0x40310C40 | 0x00000020 | HSIO_STD Port #24 configuration |
| 358      | PERI_MS_PPU_FX_GPIO_PRT25_CFG    | 0x40310CC0 | 0x00000020 | HSIO_STD Port #25 configuration |
| 359      | PERI_MS_PPU_FX_GPIO_PRT26_CFG    | 0x40310D40 | 0x00000020 | HSIO_STD Port #26 configuration |
| 360      | PERI_MS_PPU_FX_GPIO_PRT27_CFG    | 0x40310DC0 | 0x00000020 | HSIO_STD Port #27 configuration |
| 361      | PERI_MS_PPU_FX_GPIO_PRT28_CFG    | 0x40310E40 | 0x00000020 | GPIO_STD Port #28 configuration |
| 362      | PERI_MS_PPU_FX_GPIO_PRT29_CFG    | 0x40310EC0 | 0x00000020 | GPIO_STD Port #29 configuration |
| 363      | PERI_MS_PPU_FX_GPIO_PRT30_CFG    | 0x40310F40 | 0x00000020 | GPIO_STD Port #30 configuration |
| 364      | PERI_MS_PPU_FX_GPIO_PRT31_CFG    | 0x40310FC0 | 0x00000020 | GPIO_STD Port #31 configuration |
| 365      | PERI_MS_PPU_FX_GPIO_PRT32_CFG    | 0x40311040 | 0x00000020 | GPIO_STD Port #32 configuration |
| 366      | PERI_MS_PPU_FX_GPIO_GPIO         | 0x40314000 | 0x00000040 | GPIO main                       |
| 367      | PERI_MS_PPU_FX_GPIO_TEST         | 0x40315000 | 0x00000008 | GPIO test                       |
| 368      | PERI_MS_PPU_FX_SMARTIO_PRT12_PRT | 0x40320C00 | 0x00000100 | SMART I/O #12                   |
| 369      | PERI_MS_PPU_FX_SMARTIO_PRT13_PRT | 0x40320D00 | 0x00000100 | SMART I/O #13                   |
| 370      | PERI_MS_PPU_FX_SMARTIO_PRT14_PRT | 0x40320E00 | 0x00000100 | SMART I/O #14                   |
| 371      | PERI_MS_PPU_FX_SMARTIO_PRT15_PRT | 0x40320F00 | 0x00000100 | SMART I/O #15                   |
| 372      | PERI_MS_PPU_FX_SMARTIO_PRT17_PRT | 0x40321100 | 0x00000100 | SMART I/O #17                   |
| 373      | PERI_MS_PPU_FX_EVTGEN0           | 0x403F0000 | 0x00001000 | Event generator #0              |
| 374      | PERI_MS_PPU_FX_SMIF0             | 0x40420000 | 0x00010000 | Serial Memory Interface #0      |
| 375      | PERI_MS_PPU_FX_SDHC0             | 0x40460000 | 0x00010000 | Secure Digital High Capacity #0 |
| 376      | PERI_MS_PPU_FX_ETH0              | 0x40480000 | 0x00010000 | Ethernet0                       |
| 377      | PERI_MS_PPU_FX_LIN0_MAIN         | 0x40500000 | 0x00000008 | LIN0, main                      |
| 378      | PERI_MS_PPU_FX_LIN0_CH0_CH       | 0x40508000 | 0x00000100 | LIN0, Channel #0                |
| 379      | PERI_MS_PPU_FX_LIN0_CH1_CH       | 0x40508100 | 0x00000100 | LIN0, Channel #1                |
| 380      | PERI_MS_PPU_FX_LIN0_CH2_CH       | 0x40508200 | 0x00000100 | LIN0, Channel #2                |
| 381      | PERI_MS_PPU_FX_LIN0_CH3_CH       | 0x40508300 | 0x00000100 | LIN0, Channel #3                |
| 382      | PERI_MS_PPU_FX_LIN0_CH4_CH       | 0x40508400 | 0x00000100 | LIN0, Channel #4                |
| 383      | PERI_MS_PPU_FX_LIN0_CH5_CH       | 0x40508500 | 0x00000100 | LIN0, Channel #5                |
| 384      | PERI_MS_PPU_FX_LIN0_CH6_CH       | 0x40508600 | 0x00000100 | LIN0, Channel #6                |
| 385      | PERI_MS_PPU_FX_LIN0_CH7_CH       | 0x40508700 | 0x00000100 | LIN0, Channel #7                |
| 386      | PERI_MS_PPU_FX_LIN0_CH8_CH       | 0x40508800 | 0x00000100 | LIN0, Channel #8                |
| 387      | PERI_MS_PPU_FX_LIN0_CH9_CH       | 0x40508900 | 0x00000100 | LIN0, Channel #9                |
| 388      | PERI_MS_PPU_FX_LIN0_CH10_CH      | 0x40508A00 | 0x00000100 | LIN0, Channel #10               |
| 389      | PERI_MS_PPU_FX_LIN0_CH11_CH      | 0x40508B00 | 0x00000100 | LIN0, Channel #11               |
| 390      | PERI_MS_PPU_FX_LIN0_CH12_CH      | 0x40508C00 | 0x00000100 | LIN0, Channel #12               |
| 391      | PERI_MS_PPU_FX_LIN0_CH13_CH      | 0x40508D00 | 0x00000100 | LIN0, Channel #13               |
| 392      | PERI_MS_PPU_FX_LIN0_CH14_CH      | 0x40508E00 | 0x00000100 | LIN0, Channel #14               |
| 393      | PERI_MS_PPU_FX_LIN0_CH15_CH      | 0x40508F00 | 0x00000100 | LIN0, Channel #15               |

**Table 22-1 PPU fixed structure pairs** (continued)

| Pair no. | PPU fixed structure pair             | Address    | Size       | Description                  |
|----------|--------------------------------------|------------|------------|------------------------------|
| 394      | PERI_MS_PPU_FX_CANFD0_CH0_CH         | 0x40520000 | 0x00000200 | CAN0, Channel #0             |
| 395      | PERI_MS_PPU_FX_CANFD0_CH1_CH         | 0x40520200 | 0x00000200 | CAN0, Channel #1             |
| 396      | PERI_MS_PPU_FX_CANFD0_CH2_CH         | 0x40520400 | 0x00000200 | CAN0, Channel #2             |
| 397      | PERI_MS_PPU_FX_CANFD0_CH3_CH         | 0x40520600 | 0x00000200 | CAN0, Channel #3             |
| 398      | PERI_MS_PPU_FX_CANFD1_CH0_CH         | 0x40540000 | 0x00000200 | CAN1, Channel #0             |
| 399      | PERI_MS_PPU_FX_CANFD1_CH1_CH         | 0x40540200 | 0x00000200 | CAN1, Channel #1             |
| 400      | PERI_MS_PPU_FX_CANFD1_CH2_CH         | 0x40540400 | 0x00000200 | CAN1, Channel #2             |
| 401      | PERI_MS_PPU_FX_CANFD1_CH3_CH         | 0x40540600 | 0x00000200 | CAN1, Channel #3             |
| 402      | PERI_MS_PPU_FX_CANFD0_MAIN           | 0x40521000 | 0x00000100 | CAN0 main                    |
| 403      | PERI_MS_PPU_FX_CANFD1_MAIN           | 0x40541000 | 0x00000100 | CAN1 main                    |
| 404      | PERI_MS_PPU_FX_CANFD0_BUF            | 0x40530000 | 0x00010000 | CAN0 buffer                  |
| 405      | PERI_MS_PPU_FX_CANFD1_BUF            | 0x40550000 | 0x00010000 | CAN1 buffer                  |
| 406      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT0_CNT  | 0x40580000 | 0x00000080 | TCPWM0 Group #0, Counter #0  |
| 407      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT1_CNT  | 0x40580080 | 0x00000080 | TCPWM0 Group #0, Counter #1  |
| 408      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT2_CNT  | 0x40580100 | 0x00000080 | TCPWM0 Group #0, Counter #2  |
| 409      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT3_CNT  | 0x40580180 | 0x00000080 | TCPWM0 Group #0, Counter #3  |
| 410      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT4_CNT  | 0x40580200 | 0x00000080 | TCPWM0 Group #0, Counter #4  |
| 411      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT5_CNT  | 0x40580280 | 0x00000080 | TCPWM0 Group #0, Counter #5  |
| 412      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT6_CNT  | 0x40580300 | 0x00000080 | TCPWM0 Group #0, Counter #6  |
| 413      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT7_CNT  | 0x40580380 | 0x00000080 | TCPWM0 Group #0, Counter #7  |
| 414      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT8_CNT  | 0x40580400 | 0x00000080 | TCPWM0 Group #0, Counter #8  |
| 415      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT9_CNT  | 0x40580480 | 0x00000080 | TCPWM0 Group #0, Counter #9  |
| 416      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT10_CNT | 0x40580500 | 0x00000080 | TCPWM0 Group #0, Counter #10 |
| 417      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT11_CNT | 0x40580580 | 0x00000080 | TCPWM0 Group #0, Counter #11 |
| 418      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT12_CNT | 0x40580600 | 0x00000080 | TCPWM0 Group #0, Counter #12 |
| 419      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT13_CNT | 0x40580680 | 0x00000080 | TCPWM0 Group #0, Counter #13 |
| 420      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT14_CNT | 0x40580700 | 0x00000080 | TCPWM0 Group #0, Counter #14 |
| 421      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT15_CNT | 0x40580780 | 0x00000080 | TCPWM0 Group #0, Counter #15 |
| 422      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT16_CNT | 0x40580800 | 0x00000080 | TCPWM0 Group #0, Counter #16 |
| 423      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT17_CNT | 0x40580880 | 0x00000080 | TCPWM0 Group #0, Counter #17 |
| 424      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT18_CNT | 0x40580900 | 0x00000080 | TCPWM0 Group #0, Counter #18 |
| 425      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT19_CNT | 0x40580980 | 0x00000080 | TCPWM0 Group #0, Counter #19 |
| 426      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT20_CNT | 0x40580A00 | 0x00000080 | TCPWM0 Group #0, Counter #20 |
| 427      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT21_CNT | 0x40580A80 | 0x00000080 | TCPWM0 Group #0, Counter #21 |
| 428      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT22_CNT | 0x40580B00 | 0x00000080 | TCPWM0 Group #0, Counter #22 |
| 429      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT23_CNT | 0x40580B80 | 0x00000080 | TCPWM0 Group #0, Counter #23 |
| 430      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT24_CNT | 0x40580C00 | 0x00000080 | TCPWM0 Group #0, Counter #24 |
| 431      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT25_CNT | 0x40580C80 | 0x00000080 | TCPWM0 Group #0, Counter #25 |
| 432      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT26_CNT | 0x40580D00 | 0x00000080 | TCPWM0 Group #0, Counter #26 |
| 433      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT27_CNT | 0x40580D80 | 0x00000080 | TCPWM0 Group #0, Counter #27 |
| 434      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT28_CNT | 0x40580E00 | 0x00000080 | TCPWM0 Group #0, Counter #28 |
| 435      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT29_CNT | 0x40580E80 | 0x00000080 | TCPWM0 Group #0, Counter #29 |
| 436      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT30_CNT | 0x40580F00 | 0x00000080 | TCPWM0 Group #0, Counter #30 |
| 437      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT31_CNT | 0x40580F80 | 0x00000080 | TCPWM0 Group #0, Counter #31 |
| 438      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT32_CNT | 0x40581000 | 0x00000080 | TCPWM0 Group #0, Counter #32 |

**Table 22-1 PPU fixed structure pairs** (continued)

| Pair no. | PPU fixed structure pair             | Address    | Size       | Description                  |
|----------|--------------------------------------|------------|------------|------------------------------|
| 439      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT33_CNT | 0x40581080 | 0x00000080 | TCPWM0 Group #0, Counter #33 |
| 440      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT34_CNT | 0x40581100 | 0x00000080 | TCPWM0 Group #0, Counter #34 |
| 441      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT35_CNT | 0x40581180 | 0x00000080 | TCPWM0 Group #0, Counter #35 |
| 442      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT36_CNT | 0x40581200 | 0x00000080 | TCPWM0 Group #0, Counter #36 |
| 443      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT37_CNT | 0x40581280 | 0x00000080 | TCPWM0 Group #0, Counter #37 |
| 444      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT38_CNT | 0x40581300 | 0x00000080 | TCPWM0 Group #0, Counter #38 |
| 445      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT39_CNT | 0x40581380 | 0x00000080 | TCPWM0 Group #0, Counter #39 |
| 446      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT40_CNT | 0x40581400 | 0x00000080 | TCPWM0 Group #0, Counter #40 |
| 447      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT41_CNT | 0x40581480 | 0x00000080 | TCPWM0 Group #0, Counter #41 |
| 448      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT42_CNT | 0x40581500 | 0x00000080 | TCPWM0 Group #0, Counter #42 |
| 449      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT43_CNT | 0x40581580 | 0x00000080 | TCPWM0 Group #0, Counter #43 |
| 450      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT44_CNT | 0x40581600 | 0x00000080 | TCPWM0 Group #0, Counter #44 |
| 451      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT45_CNT | 0x40581680 | 0x00000080 | TCPWM0 Group #0, Counter #45 |
| 452      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT46_CNT | 0x40581700 | 0x00000080 | TCPWM0 Group #0, Counter #46 |
| 453      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT47_CNT | 0x40581780 | 0x00000080 | TCPWM0 Group #0, Counter #47 |
| 454      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT48_CNT | 0x40581800 | 0x00000080 | TCPWM0 Group #0, Counter #48 |
| 455      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT49_CNT | 0x40581880 | 0x00000080 | TCPWM0 Group #0, Counter #49 |
| 456      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT50_CNT | 0x40581900 | 0x00000080 | TCPWM0 Group #0, Counter #50 |
| 457      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT51_CNT | 0x40581980 | 0x00000080 | TCPWM0 Group #0, Counter #51 |
| 458      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT52_CNT | 0x40581A00 | 0x00000080 | TCPWM0 Group #0, Counter #52 |
| 459      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT53_CNT | 0x40581A80 | 0x00000080 | TCPWM0 Group #0, Counter #53 |
| 460      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT54_CNT | 0x40581B00 | 0x00000080 | TCPWM0 Group #0, Counter #54 |
| 461      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT55_CNT | 0x40581B80 | 0x00000080 | TCPWM0 Group #0, Counter #55 |
| 462      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT56_CNT | 0x40581C00 | 0x00000080 | TCPWM0 Group #0, Counter #56 |
| 463      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT57_CNT | 0x40581C80 | 0x00000080 | TCPWM0 Group #0, Counter #57 |
| 464      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT58_CNT | 0x40581D00 | 0x00000080 | TCPWM0 Group #0, Counter #58 |
| 465      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT59_CNT | 0x40581D80 | 0x00000080 | TCPWM0 Group #0, Counter #59 |
| 466      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT60_CNT | 0x40581E00 | 0x00000080 | TCPWM0 Group #0, Counter #60 |
| 467      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT61_CNT | 0x40581E80 | 0x00000080 | TCPWM0 Group #0, Counter #61 |
| 468      | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT62_CNT | 0x40581F00 | 0x00000080 | TCPWM0 Group #0, Counter #62 |
| 469      | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT0_CNT  | 0x40588000 | 0x00000080 | TCPWM0 Group #1, Counter #0  |
| 470      | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT1_CNT  | 0x40588080 | 0x00000080 | TCPWM0 Group #1, Counter #1  |
| 471      | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT2_CNT  | 0x40588100 | 0x00000080 | TCPWM0 Group #1, Counter #2  |
| 472      | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT3_CNT  | 0x40588180 | 0x00000080 | TCPWM0 Group #1, Counter #3  |
| 473      | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT4_CNT  | 0x40588200 | 0x00000080 | TCPWM0 Group #1, Counter #4  |
| 474      | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT5_CNT  | 0x40588280 | 0x00000080 | TCPWM0 Group #1, Counter #5  |
| 475      | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT6_CNT  | 0x40588300 | 0x00000080 | TCPWM0 Group #1, Counter #6  |
| 476      | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT7_CNT  | 0x40588380 | 0x00000080 | TCPWM0 Group #1, Counter #7  |
| 477      | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT8_CNT  | 0x40588400 | 0x00000080 | TCPWM0 Group #1, Counter #8  |
| 478      | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT9_CNT  | 0x40588480 | 0x00000080 | TCPWM0 Group #1, Counter #9  |
| 479      | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT10_CNT | 0x40588500 | 0x00000080 | TCPWM0 Group #1, Counter #10 |
| 480      | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT11_CNT | 0x40588580 | 0x00000080 | TCPWM0 Group #1, Counter #11 |
| 481      | PERI_MS_PPU_FX_TCPWM0_GRP2_CNT0_CNT  | 0x40590000 | 0x00000080 | TCPWM0 Group #2, Counter #0  |
| 482      | PERI_MS_PPU_FX_TCPWM0_GRP2_CNT1_CNT  | 0x40590080 | 0x00000080 | TCPWM0 Group #2, Counter #1  |
| 483      | PERI_MS_PPU_FX_TCPWM0_GRP2_CNT2_CNT  | 0x40590100 | 0x00000080 | TCPWM0 Group #2, Counter #2  |

**Table 22-1 PPU fixed structure pairs** (continued)

| Pair no. | PPU fixed structure pair            | Address    | Size       | Description                 |
|----------|-------------------------------------|------------|------------|-----------------------------|
| 484      | PERI_MS_PPU_FX_TCPWM0_GRP2_CNT3_CNT | 0x40590180 | 0x00000080 | TCPWM0 Group #2, Counter #3 |
| 485      | PERI_MS_PPU_FX_TCPWM0_GRP2_CNT4_CNT | 0x40590200 | 0x00000080 | TCPWM0 Group #2, Counter #4 |
| 486      | PERI_MS_PPU_FX_TCPWM0_GRP2_CNT5_CNT | 0x40590280 | 0x00000080 | TCPWM0 Group #2, Counter #5 |
| 487      | PERI_MS_PPU_FX_TCPWM0_GRP2_CNT6_CNT | 0x40590300 | 0x00000080 | TCPWM0 Group #2, Counter #6 |
| 488      | PERI_MS_PPU_FX_TCPWM0_GRP2_CNT7_CNT | 0x40590380 | 0x00000080 | TCPWM0 Group #2, Counter #7 |
| 489      | PERI_MS_PPU_FX_SCB0                 | 0x40600000 | 0x00010000 | SCB0                        |
| 490      | PERI_MS_PPU_FX_SCB1                 | 0x40610000 | 0x00010000 | SCB1                        |
| 491      | PERI_MS_PPU_FX_SCB2                 | 0x40620000 | 0x00010000 | SCB2                        |
| 492      | PERI_MS_PPU_FX_SCB3                 | 0x40630000 | 0x00010000 | SCB3                        |
| 493      | PERI_MS_PPU_FX_SCB4                 | 0x40640000 | 0x00010000 | SCB4                        |
| 494      | PERI_MS_PPU_FX_SCB5                 | 0x40650000 | 0x00010000 | SCB5                        |
| 495      | PERI_MS_PPU_FX_SCB6                 | 0x40660000 | 0x00010000 | SCB6                        |
| 496      | PERI_MS_PPU_FX_SCB7                 | 0x40670000 | 0x00010000 | SCB7                        |
| 497      | PERI_MS_PPU_FX_SCB8                 | 0x40680000 | 0x00010000 | SCB8                        |
| 498      | PERI_MS_PPU_FX_SCB9                 | 0x40690000 | 0x00010000 | SCB9                        |
| 499      | PERI_MS_PPU_FX_SCB10                | 0x406A0000 | 0x00010000 | SCB10                       |
| 500      | PERI_MS_PPU_FX_I2S0                 | 0x40800000 | 0x00001000 | AUDIOSS I2S0                |
| 501      | PERI_MS_PPU_FX_I2S1                 | 0x40801000 | 0x00001000 | AUDIOSS I2S1                |
| 502      | PERI_MS_PPU_FX_I2S2                 | 0x40802000 | 0x00001000 | AUDIOSS I2S2                |
| 503      | PERI_MS_PPU_FX_PASS0_SAR0_SAR       | 0x40900000 | 0x00000400 | PASS SAR0                   |
| 504      | PERI_MS_PPU_FX_PASS0_SAR1_SAR       | 0x40901000 | 0x00000400 | PASS SAR1                   |
| 505      | PERI_MS_PPU_FX_PASS0_SAR2_SAR       | 0x40902000 | 0x00000400 | PASS SAR2                   |
| 506      | PERI_MS_PPU_FX_PASS0_SAR0_CH0_CH    | 0x40900800 | 0x00000040 | SAR0, Channel #0            |
| 507      | PERI_MS_PPU_FX_PASS0_SAR0_CH1_CH    | 0x40900840 | 0x00000040 | SAR0, Channel #1            |
| 508      | PERI_MS_PPU_FX_PASS0_SAR0_CH2_CH    | 0x40900880 | 0x00000040 | SAR0, Channel #2            |
| 509      | PERI_MS_PPU_FX_PASS0_SAR0_CH3_CH    | 0x409008C0 | 0x00000040 | SAR0, Channel #3            |
| 510      | PERI_MS_PPU_FX_PASS0_SAR0_CH4_CH    | 0x40900900 | 0x00000040 | SAR0, Channel #4            |
| 511      | PERI_MS_PPU_FX_PASS0_SAR0_CH5_CH    | 0x40900940 | 0x00000040 | SAR0, Channel #5            |
| 512      | PERI_MS_PPU_FX_PASS0_SAR0_CH6_CH    | 0x40900980 | 0x00000040 | SAR0, Channel #6            |
| 513      | PERI_MS_PPU_FX_PASS0_SAR0_CH7_CH    | 0x409009C0 | 0x00000040 | SAR0, Channel #7            |
| 514      | PERI_MS_PPU_FX_PASS0_SAR0_CH8_CH    | 0x40900A00 | 0x00000040 | SAR0, Channel #8            |
| 515      | PERI_MS_PPU_FX_PASS0_SAR0_CH9_CH    | 0x40900A40 | 0x00000040 | SAR0, Channel #9            |
| 516      | PERI_MS_PPU_FX_PASS0_SAR0_CH10_CH   | 0x40900A80 | 0x00000040 | SAR0, Channel #10           |
| 517      | PERI_MS_PPU_FX_PASS0_SAR0_CH11_CH   | 0x40900AC0 | 0x00000040 | SAR0, Channel #11           |
| 518      | PERI_MS_PPU_FX_PASS0_SAR0_CH12_CH   | 0x40900B00 | 0x00000040 | SAR0, Channel #12           |
| 519      | PERI_MS_PPU_FX_PASS0_SAR0_CH13_CH   | 0x40900B40 | 0x00000040 | SAR0, Channel #13           |
| 520      | PERI_MS_PPU_FX_PASS0_SAR0_CH14_CH   | 0x40900B80 | 0x00000040 | SAR0, Channel #14           |
| 521      | PERI_MS_PPU_FX_PASS0_SAR0_CH15_CH   | 0x40900BC0 | 0x00000040 | SAR0, Channel #15           |
| 522      | PERI_MS_PPU_FX_PASS0_SAR0_CH16_CH   | 0x40900C00 | 0x00000040 | SAR0, Channel #16           |
| 523      | PERI_MS_PPU_FX_PASS0_SAR0_CH17_CH   | 0x40900C40 | 0x00000040 | SAR0, Channel #17           |
| 524      | PERI_MS_PPU_FX_PASS0_SAR0_CH18_CH   | 0x40900C80 | 0x00000040 | SAR0, Channel #18           |
| 525      | PERI_MS_PPU_FX_PASS0_SAR0_CH19_CH   | 0x40900CC0 | 0x00000040 | SAR0, Channel #19           |
| 526      | PERI_MS_PPU_FX_PASS0_SAR0_CH20_CH   | 0x40900D00 | 0x00000040 | SAR0, Channel #20           |
| 527      | PERI_MS_PPU_FX_PASS0_SAR0_CH21_CH   | 0x40900D40 | 0x00000040 | SAR0, Channel #21           |
| 528      | PERI_MS_PPU_FX_PASS0_SAR0_CH22_CH   | 0x40900D80 | 0x00000040 | SAR0, Channel #22           |

**Table 22-1 PPU fixed structure pairs** (continued)

| Pair no. | PPU fixed structure pair          | Address    | Size       | Description       |
|----------|-----------------------------------|------------|------------|-------------------|
| 529      | PERI_MS_PPU_FX_PASS0_SAR0_CH23_CH | 0x40900DC0 | 0x00000040 | SAR0, Channel #23 |
| 530      | PERI_MS_PPU_FX_PASS0_SAR0_CH24_CH | 0x40900E00 | 0x00000040 | SAR0, Channel #24 |
| 531      | PERI_MS_PPU_FX_PASS0_SAR0_CH25_CH | 0x40900E40 | 0x00000040 | SAR0, Channel #25 |
| 532      | PERI_MS_PPU_FX_PASS0_SAR0_CH26_CH | 0x40900E80 | 0x00000040 | SAR0, Channel #26 |
| 533      | PERI_MS_PPU_FX_PASS0_SAR0_CH27_CH | 0x40900EC0 | 0x00000040 | SAR0, Channel #27 |
| 534      | PERI_MS_PPU_FX_PASS0_SAR0_CH28_CH | 0x40900F00 | 0x00000040 | SAR0, Channel #28 |
| 535      | PERI_MS_PPU_FX_PASS0_SAR0_CH29_CH | 0x40900F40 | 0x00000040 | SAR0, Channel #29 |
| 536      | PERI_MS_PPU_FX_PASS0_SAR0_CH30_CH | 0x40900F80 | 0x00000040 | SAR0, Channel #30 |
| 537      | PERI_MS_PPU_FX_PASS0_SAR0_CH31_CH | 0x40900FC0 | 0x00000040 | SAR0, Channel #31 |
| 538      | PERI_MS_PPU_FX_PASS0_SAR1_CH0_CH  | 0x40901800 | 0x00000040 | SAR1, Channel #0  |
| 539      | PERI_MS_PPU_FX_PASS0_SAR1_CH1_CH  | 0x40901840 | 0x00000040 | SAR1, Channel #1  |
| 540      | PERI_MS_PPU_FX_PASS0_SAR1_CH2_CH  | 0x40901880 | 0x00000040 | SAR1, Channel #2  |
| 541      | PERI_MS_PPU_FX_PASS0_SAR1_CH3_CH  | 0x409018C0 | 0x00000040 | SAR1, Channel #3  |
| 542      | PERI_MS_PPU_FX_PASS0_SAR1_CH4_CH  | 0x40901900 | 0x00000040 | SAR1, Channel #4  |
| 543      | PERI_MS_PPU_FX_PASS0_SAR1_CH5_CH  | 0x40901940 | 0x00000040 | SAR1, Channel #5  |
| 544      | PERI_MS_PPU_FX_PASS0_SAR1_CH6_CH  | 0x40901980 | 0x00000040 | SAR1, Channel #6  |
| 545      | PERI_MS_PPU_FX_PASS0_SAR1_CH7_CH  | 0x409019C0 | 0x00000040 | SAR1, Channel #7  |
| 546      | PERI_MS_PPU_FX_PASS0_SAR1_CH8_CH  | 0x40901A00 | 0x00000040 | SAR1, Channel #8  |
| 547      | PERI_MS_PPU_FX_PASS0_SAR1_CH9_CH  | 0x40901A40 | 0x00000040 | SAR1, Channel #9  |
| 548      | PERI_MS_PPU_FX_PASS0_SAR1_CH10_CH | 0x40901A80 | 0x00000040 | SAR1, Channel #10 |
| 549      | PERI_MS_PPU_FX_PASS0_SAR1_CH11_CH | 0x40901AC0 | 0x00000040 | SAR1, Channel #11 |
| 550      | PERI_MS_PPU_FX_PASS0_SAR1_CH12_CH | 0x40901B00 | 0x00000040 | SAR1, Channel #12 |
| 551      | PERI_MS_PPU_FX_PASS0_SAR1_CH13_CH | 0x40901B40 | 0x00000040 | SAR1, Channel #13 |
| 552      | PERI_MS_PPU_FX_PASS0_SAR1_CH14_CH | 0x40901B80 | 0x00000040 | SAR1, Channel #14 |
| 553      | PERI_MS_PPU_FX_PASS0_SAR1_CH15_CH | 0x40901BC0 | 0x00000040 | SAR1, Channel #15 |
| 554      | PERI_MS_PPU_FX_PASS0_SAR1_CH16_CH | 0x40901C00 | 0x00000040 | SAR1, Channel #16 |
| 555      | PERI_MS_PPU_FX_PASS0_SAR1_CH17_CH | 0x40901C40 | 0x00000040 | SAR1, Channel #17 |
| 556      | PERI_MS_PPU_FX_PASS0_SAR1_CH18_CH | 0x40901C80 | 0x00000040 | SAR1, Channel #18 |
| 557      | PERI_MS_PPU_FX_PASS0_SAR1_CH19_CH | 0x40901CC0 | 0x00000040 | SAR1, Channel #19 |
| 558      | PERI_MS_PPU_FX_PASS0_SAR1_CH20_CH | 0x40901D00 | 0x00000040 | SAR1, Channel #20 |
| 559      | PERI_MS_PPU_FX_PASS0_SAR1_CH21_CH | 0x40901D40 | 0x00000040 | SAR1, Channel #21 |
| 560      | PERI_MS_PPU_FX_PASS0_SAR1_CH22_CH | 0x40901D80 | 0x00000040 | SAR1, Channel #22 |
| 561      | PERI_MS_PPU_FX_PASS0_SAR1_CH23_CH | 0x40901DC0 | 0x00000040 | SAR1, Channel #23 |
| 562      | PERI_MS_PPU_FX_PASS0_SAR1_CH24_CH | 0x40901E00 | 0x00000040 | SAR1, Channel #24 |
| 563      | PERI_MS_PPU_FX_PASS0_SAR1_CH25_CH | 0x40901E40 | 0x00000040 | SAR1, Channel #25 |
| 564      | PERI_MS_PPU_FX_PASS0_SAR1_CH26_CH | 0x40901E80 | 0x00000040 | SAR1, Channel #26 |
| 565      | PERI_MS_PPU_FX_PASS0_SAR1_CH27_CH | 0x40901EC0 | 0x00000040 | SAR1, Channel #27 |
| 566      | PERI_MS_PPU_FX_PASS0_SAR1_CH28_CH | 0x40901F00 | 0x00000040 | SAR1, Channel #28 |
| 567      | PERI_MS_PPU_FX_PASS0_SAR1_CH29_CH | 0x40901F40 | 0x00000040 | SAR1, Channel #29 |
| 568      | PERI_MS_PPU_FX_PASS0_SAR1_CH30_CH | 0x40901F80 | 0x00000040 | SAR1, Channel #30 |
| 569      | PERI_MS_PPU_FX_PASS0_SAR1_CH31_CH | 0x40901FC0 | 0x00000040 | SAR1, Channel #31 |
| 570      | PERI_MS_PPU_FX_PASS0_SAR2_CH0_CH  | 0x40902800 | 0x00000040 | SAR2, Channel #0  |
| 571      | PERI_MS_PPU_FX_PASS0_SAR2_CH1_CH  | 0x40902840 | 0x00000040 | SAR2, Channel #1  |
| 572      | PERI_MS_PPU_FX_PASS0_SAR2_CH2_CH  | 0x40902880 | 0x00000040 | SAR2, Channel #2  |
| 573      | PERI_MS_PPU_FX_PASS0_SAR2_CH3_CH  | 0x409028C0 | 0x00000040 | SAR2, Channel #3  |

**Table 22-1 PPU fixed structure pairs** *(continued)*

| Pair no. | PPU fixed structure pair         | Address    | Size       | Description      |
|----------|----------------------------------|------------|------------|------------------|
| 574      | PERI_MS_PPU_FX_PASS0_SAR2_CH4_CH | 0x40902900 | 0x00000040 | SAR2, Channel #4 |
| 575      | PERI_MS_PPU_FX_PASS0_SAR2_CH5_CH | 0x40902940 | 0x00000040 | SAR2, Channel #5 |
| 576      | PERI_MS_PPU_FX_PASS0_SAR2_CH6_CH | 0x40902980 | 0x00000040 | SAR2, Channel #6 |
| 577      | PERI_MS_PPU_FX_PASS0_SAR2_CH7_CH | 0x409029C0 | 0x00000040 | SAR2, Channel #7 |
| 578      | PERI_MS_PPU_FX_PASS0_TOP         | 0x409F0000 | 0x00001000 | PASS0 SAR main   |

## 23 Bus masters

The Arbiter (part of flash controller) performs priority-based arbitration based on the master identifier. Each bus master has a dedicated 4-bit master identifier. This master identifier is used for bus arbitration and IPC functionality.

**Table 23-1 Bus masters for access and protection control**

| ID No. | Master ID          | Description                                     |
|--------|--------------------|-------------------------------------------------|
| 0      | CPUSS_MS_ID_CM0    | Master ID for CM0+                              |
| 1      | CPUSS_MS_ID_CRYPT0 | Master ID for Crypto                            |
| 2      | CPUSS_MS_ID_DW0    | Master ID for P-DMA0                            |
| 3      | CPUSS_MS_ID_DW1    | Master ID for P-DMA1                            |
| 4      | CPUSS_MS_ID_DM0    | Master ID for M-DMA0                            |
| 5      | CPUSS_MS_ID_SLOW0  | Master ID for External AHB-Lite Master 0 (SDHC) |
| 6      | CPUSS_MS_ID_SLOW1  | Master ID for External AHB-Lite Master 1 (ETH0) |
| 13     | CPUSS_MS_ID_CM7_1  | Master ID for CM7_1                             |
| 14     | CPUSS_MS_ID_CM7_0  | Master ID for CM7_0                             |
| 15     | CPUSS_MS_ID_TC     | Master ID for DAP Tap Controller                |

## 24 Miscellaneous configuration

**Table 24-1 Miscellaneous configuration for CYT3BB/4BB devices**

| Sl. No. | Configuration                                  | Number/instances | Description                                                                                                                                                                              |
|---------|------------------------------------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0       | SRSS_NUM_CLKPATH                               | 7                | Number of clock paths. One for each of FLL, PLL, Direct and CSV                                                                                                                          |
| 1       | SRSS_NUM_HFROOT                                | 8                | Number of CLK_HFs present                                                                                                                                                                |
| 2       | PERI_PC_NR                                     | 8                | Number of protection contexts                                                                                                                                                            |
| 3       | PERI_PERI_PCLK_PCLK_GROUP_NR                   | 2                | Number of asynchronous PCLK groups                                                                                                                                                       |
| 4       | PERI_PERI_PCLK_PCLK_GROUP_NR0_GR_DIV_8_VECT    | 3                | Group 0, Number of divide-by-8 clock dividers                                                                                                                                            |
| 5       | PERI_PERI_PCLK_PCLK_GROUP_NR0_GR_DIV_16_VECT   | 1                | Group 0, Number of divide-by-16 clock dividers                                                                                                                                           |
| 7       | PERI_PERI_PCLK_PCLK_GROUP_NR0_GR_CLOCK_VECT    | 6                | Group 0, Number of programmable clocks [1, 256]                                                                                                                                          |
| 8       | PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_DIV_8_VECT    | 16               | Group 1, Number of divide-by-8 clock dividers                                                                                                                                            |
| 9       | PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_DIV_16_VECT   | 17               | Group 1, Number of divide-by-16 clock dividers                                                                                                                                           |
| 10      | PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_DIV_24_5_VECT | 16               | Group 1, Number of divide-by-24.5 clock dividers                                                                                                                                         |
| 11      | PERI_PERI_PCLK_PCLK_GROUP_NR1_GR_CLOCK_VECT    | 121              | Group 1, Number of programmable clocks [1, 256]                                                                                                                                          |
| 12      | CPUSS_CM0P_MPU_NR                              | 8                | Number of MPU regions in CM0+                                                                                                                                                            |
| 13      | CPUSS_CM7_0_FPU_LVL                            | 2                | CM7_0 Floating point unit configuration.<br>0 - No FPU<br>1 - Single precision FPU<br>2 - Single and Double precision FPU                                                                |
| 14      | CPUSS_CM7_0_MPU_NR                             | 16               | Number of MPU regions in CM7_0                                                                                                                                                           |
| 15      | CPUSS_CM7_0_ICACHE_SIZE                        | 16               | CM7_0 Instruction cache (ICACHE) size in KB                                                                                                                                              |
| 16      | CPUSS_CM7_0_DCACHE_SIZE                        | 16               | CM7_0 Data cache size (DCACHE) in KB                                                                                                                                                     |
| 17      | CPUSS_CM7_0_ITCM_SIZE                          | 16               | CM7_0 Instruction TCM (ITCM) size in KB                                                                                                                                                  |
| 18      | CPUSS_CM7_0_DTCM_SIZE                          | 16               | CM7_0 Data TCM (DTCM) size in KB                                                                                                                                                         |
| 19      | CPUSS_CM7_1_FPU_LVL                            | 2                | CM7_1 Floating point unit configuration.<br>0 - No FPU<br>1 - Single precision FPU<br>2 - Single and Double precision FPU                                                                |
| 20      | CPUSS_CM7_1_MPU_NR                             | 16               | Number of MPU regions in CM7_1                                                                                                                                                           |
| 21      | CPUSS_CM7_1_ICACHE_SIZE                        | 16               | CM7_1 Instruction cache (ICACHE) size in KB                                                                                                                                              |
| 22      | CPUSS_CM7_1_DCACHE_SIZE                        | 16               | CM7_1 Data cache size (DCACHE) in KB                                                                                                                                                     |
| 23      | CPUSS_CM7_1_ITCM_SIZE                          | 16               | CM7_1 Instruction TCM (ITCM) size in KB                                                                                                                                                  |
| 24      | CPUSS_CM7_1_DTCM_SIZE                          | 16               | CM7_1 Data TCM (DTCM) size in KB                                                                                                                                                         |
| 25      | CPUSS_DW0_CH_NR                                | 100              | Number of P-DMA0 channels                                                                                                                                                                |
| 26      | CPUSS_DW1_CH_NR                                | 58               | Number of P-DMA1 channels                                                                                                                                                                |
| 27      | CPUSS_DMACH_CH_NR                              | 8                | Number of M-DMA0 controller channels                                                                                                                                                     |
| 28      | CPUSS_CRYPTO_BUFF_SIZE                         | 2048             | Number of 32-bit words in the IP internal memory buffer (to allow for a 256-B, 512-B, 1-KB, 2-KB, 4-KB, 8-KB, 16-KB, and 32-KB memory buffer)                                            |
| 29      | CPUSS_FAULT_FAULT_NR                           | 4                | Number of fault structures                                                                                                                                                               |
| 30      | CPUSS_IPC_IPC_NR                               | 8                | Number of IPC structures<br>0 - Reserved for CM0+ access<br>1 - Reserved for CM7_0 access<br>2 - Reserved for CM7_1 access<br>3 - Reserved for DAP access<br>Remaining for user purposes |
| 31      | CPUSS_PROT_SMPU_STRUCT_NR                      | 16               | Number of S MPU protection structures                                                                                                                                                    |
| 32      | SCB0_EZ_DATA_NR                                | 256              | Number of EZ memory bytes. This memory is used in EZ mode, CMD_RESP mode and FIFO mode.<br>Note: Only SCB0 supports EZ mode                                                              |
| 33      | TCPWM0_TR_ONE_CNT_NR                           | 3                | Number of input triggers per counter, routed to one counter                                                                                                                              |
| 34      | TCPWM0_TR_ALL_CNT_NR                           | 27               | Number of input triggers routed to all counters, based on the pin package                                                                                                                |
| 35      | TCPWM0_GRP_NR                                  | 3                | Number of TCPWM0 counter groups                                                                                                                                                          |
| 36      | TCPWM0_GRP_NR0_GRP_GRP_CNT_NR                  | 63               | Number of counters per TCPWM0 Group #0                                                                                                                                                   |

Miscellaneous configuration

**Table 24-1** Miscellaneous configuration for CYT3BB/4BB devices *(continued)*

| Sl. No. | Configuration                       | Number/instances | Description                                         |
|---------|-------------------------------------|------------------|-----------------------------------------------------|
| 37      | TCPWM0_GRP_NR0_CNT_GRP_CNT_WIDTH    | 16               | Counter width in number of bits per TCPWM0 Group #0 |
| 38      | TCPWM0_GRP_NR1_GRP_GRP_CNT_NR       | 12               | Number of counters per TCPWM0 Group #1              |
| 39      | TCPWM0_GRP_NR1_CNT_GRP_CNT_WIDTH    | 16               | Counter width in number of bits per TCPWM0 Group #1 |
| 40      | TCPWM0_GRP_NR2_GRP_GRP_CNT_NR       | 8                | Number of counters per TCPWM0 Group #2              |
| 41      | TCPWM0_GRP_NR2_CNT_GRP_CNT_WIDTH    | 32               | Counter width in number of bits per TCPWM0 Group #2 |
| 42      | CANFD0_MRAM_SIZE / CANFD1_MRAM_SIZE | 32               | Message RAM size in KB shared by all the channels   |
| 43      | EVTGEN_COMP_STRUCT_NR               | 16               | Number of Event Generator comparator structures     |

## **25 Development support**

CYT3BB/4BB has a rich set of documentation, programming tools, and online resources to assist during the development process. Visit [www.infineon.com](http://www.infineon.com) to find out more.

### **25.1 Documentation**

A suite of documentation supports CYT3BB/4BB to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

#### **25.1.1 Software user guide**

A step-by-step guide for using the sample driver library along with third-party IDEs such as IAR EWARM and GHS Multi.

#### **25.1.2 Technical reference manual**

The Technical reference manual (TRM) contains all the technical detail needed to use a CYT3BB/4BB device, including a complete description of all registers. The TRM is available in the documentation section at [www.infineon.com](http://www.infineon.com).

### **25.2 Tools**

CYT3BB/4BB is supported on third-party development tool ecosystems such as IAR and GHS. CYT3BB/4BB is also supported by Infineon programming utilities for programming, erasing, or reading using Infineon's MiniProg4 or Segger J-link. More details are available in the documentation section at [www.infineon.com](http://www.infineon.com).

## 26 Electrical specifications

### 26.1 Absolute maximum ratings

Use of this device under conditions outside the Min and Max limits listed in [Table 26-1](#) may cause permanent damage to the device. Exposure to conditions within the limits of [Table 26-1](#) but beyond those of normal operation for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When operated under conditions within the limits of [Table 26-1](#) but beyond those of normal operation, the device may not operate to specification.

#### Power considerations

The average chip-junction temperature,  $T_J$ , in °C, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Equation. 1

Where:

$T_A$  is the ambient temperature in °C.

$\theta_{JA}$  is the package junction-to-ambient thermal resistance, in °C/W.

$P_D$  is the sum of  $P_{INT}$  and  $P_{IO}$  ( $P_D = P_{INT} + P_{IO}$ ).

$P_{INT}$  is the chip internal power. ( $P_{INT} = V_{DD} \times I_{DD} + V_{DDA} \times I_A$ )

$P_{IO}$  represents the power dissipation on input and output pins; user determined.

For most applications,  $P_{IO} < P_{INT}$  and may be neglected.

On the other hand,  $P_{IO}$  may be significant if the device is configured to continuously drive external modules and/or memories.

#### WARNING:

- The recommended operating conditions are required to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are guaranteed when the device is operated under these conditions.
- Operation under any conditions other than those mentioned in the respective “Details/Conditions” may adversely affect reliability of the device and can result in device failure.
- No guarantee is made with respect to any use, operating conditions, or combinations not represented in this datasheet. If you want to operate the device under any condition other than those listed herein, contact the sales representatives.

**Table 26-1 Absolute maximum ratings**

| Spec ID | Parameter          | Description                                           | Min                 | Typ | Max                 | Units | Details/<br>conditions                                                                     |
|---------|--------------------|-------------------------------------------------------|---------------------|-----|---------------------|-------|--------------------------------------------------------------------------------------------|
| SID10   | $V_{DD\_ABS}$      | $V_{DD}$ power supply voltage <sup>[42]</sup>         | $V_{SSD} - 0.3$     | –   | $V_{SSD} + 6.0$     | V     | For ports 0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31                 |
| SID10B  | $V_{DDIO\_1\_ABS}$ | $V_{DDIO\_1}$ power supply voltage <sup>[42]</sup>    | $V_{SSD} - 0.3$     | –   | $V_{SSD} + 6.0$     | V     | For ports 6, 7, 8, 9, 32                                                                   |
| SID10C  | $V_{DDIO\_2\_ABS}$ | $V_{DDIO\_2}$ power supply voltage <sup>[42]</sup>    | $V_{SSD} - 0.3$     | –   | $V_{SSD} + 6.0$     | V     | For ports 10, 11, 12, 13, 14, 15, 26, 27                                                   |
| SID10D  | $V_{DDIO\_3\_ABS}$ | $V_{DDIO\_3}$ power supply voltage <sup>[42]</sup>    | $V_{SSIO\_3} - 0.3$ | –   | $V_{SSIO\_3} + 4.0$ | V     | For ports 24, 25                                                                           |
| SID11   | $V_{DDA\_ABS}$     | $V_{DDA}$ analog power supply voltage <sup>[42]</sup> | $V_{SSA} - 0.3$     | –   | $V_{SSA} + 6.0$     | V     | $V_{DDIO\_2} = V_{DDA}$                                                                    |
| SID12   | $V_{REFH\_ABS}$    | Analog reference voltage, HIGH <sup>[42]</sup>        | $V_{SSA} - 0.3$     | –   | $V_{SSA} + 6.0$     | V     | $V_{REFH} \leq (V_{DDA} + 0.3 \text{ V})$                                                  |
| SID12A  | $V_{REFL\_ABS}$    | Analog reference voltage, LOW <sup>[42]</sup>         | $V_{SSA} - 0.3$     | –   | $V_{SSA} + 0.3$     | V     |                                                                                            |
| SID13   | $V_{CCD\_ABS}$     | $V_{CCD}$ Power supply voltage <sup>[42]</sup>        | $V_{SSD} - 0.3$     | –   | $V_{SSD} + 1.21$    | V     |                                                                                            |
| SID15A  | $V_{I0\_ABS}$      | Input voltage <sup>[42]</sup>                         | $V_{SSD} - 0.5$     | –   | $V_{DD} + 0.5$      | V     | For ports 0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31                 |
| SID15B  | $V_{I1\_ABS}$      | Input voltage <sup>[42]</sup>                         | $V_{SSD} - 0.5$     | –   | $V_{DDIO\_1} + 0.5$ | V     | For ports 6, 7, 8, 9, 32                                                                   |
| SID15C1 | $V_{I2\_ABS}$      | Input voltage <sup>[42]</sup>                         | $V_{SSD} - 0.5$     | –   | $V_{DDIO\_2} + 0.5$ | V     | For ports 10, 11, 12, 13, 14, 15, 26, 27                                                   |
| SID15D  | $V_{I3\_ABS}$      | Input voltage <sup>[42]</sup>                         | $V_{SSIO\_3} - 0.5$ | –   | $V_{DDIO\_3} + 0.5$ | V     | For ports 24, 25                                                                           |
| SID15F  | $V_{I5\_ABS}$      | Input voltage <sup>[42]</sup>                         | $V_{SSD} - 0.5$     | –   | $V_{DD} + 0.5$      | V     | For EXT_PS_CTL0 in external PMIC/transistor mode, EXT_PS_CTL1 in external transistor mode. |
| SID16   | $V_{IA\_ABS}$      | Analog input voltage <sup>[42]</sup>                  | $V_{SSA} - 0.3$     | –   | $V_{DDA} + 0.3$     | V     |                                                                                            |
| SID17A  | $V_{O0\_ABS}$      | Output voltage <sup>[42]</sup>                        | $V_{SSD} - 0.3$     | –   | $V_{DD} + 0.3$      | V     | For ports 0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31                 |
| SID17B  | $V_{O1\_ABS}$      | Output voltage <sup>[42]</sup>                        | $V_{SSD} - 0.3$     | –   | $V_{DDIO\_1} + 0.3$ | V     | For ports 6, 7, 8, 9, 32                                                                   |
| SID17C1 | $V_{O2\_ABS}$      | Output voltage <sup>[42]</sup>                        | $V_{SSD} - 0.3$     | –   | $V_{DDIO\_2} + 0.3$ | V     | For ports 10, 11, 12, 13, 14, 15, 26, 27                                                   |
| SID17D  | $V_{O3\_ABS}$      | Output voltage <sup>[42]</sup>                        | $V_{SSIO\_3} - 0.3$ | –   | $V_{DDIO\_3} + 0.3$ | V     | For ports 24, 25                                                                           |

**Note**

<sup>42</sup>. These parameters are based on the condition that  $V_{SSD} = V_{SSA} = V_{SSIO\_3} = 0.0 \text{ V}$ .

**Table 26-1 Absolute maximum ratings** (continued)

| Spec ID | Parameter                     | Description                                                                                                                           | Min             | Typ | Max            | Units | Details/<br>conditions                                                        |
|---------|-------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|----------------|-------|-------------------------------------------------------------------------------|
| SID17F  | $V_{O4\_ABS}$                 | Output voltage <sup>[42]</sup>                                                                                                        | $V_{SSD} - 0.3$ | –   | $V_{DD} + 0.3$ | V     | For EXT_PS_CTL1/2 in external PMIC mode, DRV_VOUT in external transistor mode |
| SID18   | $ I_{CLAMP\_ABS} $            | Maximum clamp current <sup>[43, 44, 45]</sup>                                                                                         | –5              | –   | 5              | mA    |                                                                               |
| SID18A  | $I_{CLAMP\_SUPPLY\_POS\_ABS}$ | Maximum positive clamp current per I/O supply pin. Limit applies to I/O supply pin closest to the B+ injected current <sup>[46]</sup> | –               | –   | 10             | mA    | +B injected DC current is not allowed for Ports 11 and 21.                    |
| SID18B  | $I_{CLAMP\_SUPPLY\_NEG\_ABS}$ | Maximum negative clamp current per I/O ground pin. Limit applies to I/O supply pin closest to the B+ injected current <sup>[46]</sup> | –               | –   | 10             | mA    | +B injected DC current is not allowed for Ports 11 and 21.                    |
| SID18C  | $I_{CLAMP\_TOTAL\_POS\_ABS}$  | Maximum positive clamp current per I/O supply, if not limited by the per supply pin (based on SID18A).                                | –               | –   | 50             | mA    |                                                                               |
| SID18D  | $I_{CLAMP\_TOTAL\_NEG\_ABS}$  | Maximum negative clamp current per I/O ground, if not limited by the per supply pin (based on SID18B).                                | –               | –   | 50             | mA    |                                                                               |
| SID20A  | $I_{OL1A\_ABS}$               | LOW-level maximum output current <sup>[47]</sup>                                                                                      | –               | –   | 6              | mA    | GPIO_STD, configured for drive_sel<1:0>= 0b0X                                 |
| SID20B  | $I_{OL1B\_ABS}$               | LOW-level maximum output current <sup>[47]</sup>                                                                                      | –               | –   | 2              | mA    | GPIO_STD, configured for drive_sel<1:0>= 0b10                                 |
| SID20C  | $I_{OL1C\_ABS}$               | LOW-level maximum output current <sup>[47]</sup>                                                                                      | –               | –   | 1              | mA    | GPIO_STD, configured for drive_sel<1:0>= 0b11                                 |
| SID21A  | $I_{OL2A\_ABS}$               | LOW-level maximum output current <sup>[47]</sup>                                                                                      | –               | –   | 6              | mA    | GPIO_ENH, configured for drive_sel<1:0>= 0b0X                                 |

**Notes**

43. A current-limiting resistor must be provided such that the current at the I/O pin does not exceed rated values at any time, including during power transients. Refer to [Figure 26-1](#) for more information on the recommended circuit.

44.  $V_{DD}$  and  $V_{DDIO}$  must be sufficiently loaded or protected to prevent them from being pulled out of the recommended operating range by the clamp current.

45. When the conditions of [43], [44] and SID18A/B/C/D are met,  $|I_{CLAMP\_ABS}|$  supersedes  $V_{IA\_ABS}$  and  $V_{I\_ABS}$ .

46. The definition of “closer” depends on the package. In TEQFP packaging, “closest” is determined by counting pins. For example, in a 176-TEQFP package, P17.4 (pin 120) is closer to the  $V_{DD}$  on pin 110 than on pin 132. Ports 11 and 21 should not be used for injection currents. The impact of injection currents is only defined for GPIO\_STD/GPIO\_ENH type I/Os. In BGA packaging, the following I/O port groups are treated as having separate supply pins: Ports 0, 1, 2, 22, 23, and 28; Ports 3, 4, 5, 29, 30, and 31; Ports 6, 7, 8, 9, and 32; Ports 10, 12, 13, 14, 15, 26, and 27; Ports 16 and 17; Ports 18, 19, and 20.

47. The maximum output current is the peak current flowing through any one I/O.

**Table 26-1 Absolute maximum ratings** (continued)

| Spec ID | Parameter                    | Description                                       | Min | Typ | Max | Units | Details/<br>conditions                                                                                          |
|---------|------------------------------|---------------------------------------------------|-----|-----|-----|-------|-----------------------------------------------------------------------------------------------------------------|
| SID21B  | $I_{OL2B\_ABS}$              | LOW-level maximum output current <sup>[47]</sup>  | –   | –   | 2   | mA    | GPIO_ENH, configured for drive_sel<1:0>= 0b10                                                                   |
| SID21C  | $I_{OL2C\_ABS}$              | LOW-level maximum output current <sup>[47]</sup>  | –   | –   | 1   | mA    | GPIO_ENH, configured for drive_sel<1:0>= 0b11                                                                   |
| SID22A  | $I_{OL3A\_ABS}$              | LOW-level maximum output current <sup>[47]</sup>  | –   | –   | 10  | mA    | HSIO, configured for drive_sel<1:0>= 0b00                                                                       |
| SID22B  | $I_{OL3B\_ABS}$              | LOW-level maximum output current <sup>[47]</sup>  | –   | –   | 2   | mA    | HSIO, configured for drive_sel<1:0>= 0b01                                                                       |
| SID22C  | $I_{OL3C\_ABS}$              | LOW-level maximum output current <sup>[47]</sup>  | –   | –   | 1   | mA    | HSIO, configured for drive_sel<1:0>= 0b10                                                                       |
| SID22D  | $I_{OL3D\_ABS}$              | LOW-level maximum output current <sup>[48]</sup>  | –   | –   | 0.5 | mA    | HSIO, configured for drive_sel<1:0>= 0b11                                                                       |
| SID23A  | $I_{OL4A\_ABS}$              | Sink maximum current <sup>[48]</sup>              | –   | –   | 4   | mA    | For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode |
| SID23B  | $I_{OL4B\_ABS}$              | Sink average current <sup>[50]</sup>              | –   | –   | 1   | mA    | For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode |
| SID23C  | $I_{OL4C\_ABS}$              | Sink maximum current <sup>[47]</sup>              | –   | –   | 25  | mA    | For pin DRV_VOUT in external transistor mode                                                                    |
| SID26A  | $\Sigma I_{OL\_ABS\_GP\_IO}$ | LOW-level total output current <sup>[49]</sup>    | –   | –   | 50  | mA    |                                                                                                                 |
| SID26B  | $\Sigma I_{OL\_ABS\_HS\_IO}$ | LOW-level total output current <sup>[52]</sup>    | –   | –   | 85  | mA    |                                                                                                                 |
| SID27A  | $I_{OH1A\_ABS}$              | HIGH-level maximum output current <sup>[48]</sup> | –   | –   | –5  | mA    | GPIO_STD, configured for drive_sel<1:0>= 0b0X                                                                   |

**Table 26-1 Absolute maximum ratings** (continued)

| Spec ID | Parameter             | Description                                       | Min | Typ | Max  | Units | Details/<br>conditions                                                                                           |
|---------|-----------------------|---------------------------------------------------|-----|-----|------|-------|------------------------------------------------------------------------------------------------------------------|
| SID27B  | I <sub>OH1B_ABS</sub> | HIGH-level maximum output current <sup>[48]</sup> | –   | –   | –2   | mA    | GPIO_STD, configured for drive_sel<1:0>= 0b10                                                                    |
| SID27C  | I <sub>OH1C_ABS</sub> | HIGH-level maximum output current <sup>[48]</sup> | –   | –   | –1   | mA    | GPIO_STD, configured for drive_sel<1:0>= 0b11                                                                    |
| SID28A  | I <sub>OH2A_ABS</sub> | HIGH-level maximum output current <sup>[48]</sup> | –   | –   | –5   | mA    | GPIO_ENH, configured for drive_sel<1:0>= 0b0X                                                                    |
| SID28B  | I <sub>OH2B_ABS</sub> | HIGH-level maximum output current <sup>[48]</sup> | –   | –   | –2   | mA    | GPIO_ENH, configured for drive_sel<1:0>= 0b10                                                                    |
| SID28C  | I <sub>OH2C_ABS</sub> | HIGH-level maximum output current <sup>[48]</sup> | –   | –   | –1   | mA    | GPIO_ENH, configured for drive_sel<1:0>= 0b11                                                                    |
| SID29A  | I <sub>OH3A_ABS</sub> | HIGH-level maximum output current <sup>[48]</sup> | –   | –   | –10  | mA    | HSIO, configured for drive_sel<1:0>= 0b00                                                                        |
| SID29B  | I <sub>OH3B_ABS</sub> | HIGH-level maximum output current <sup>[48]</sup> | –   | –   | –2   | mA    | HSIO, configured for drive_sel<1:0>= 0b01                                                                        |
| SID29C  | I <sub>OH3C_ABS</sub> | HIGH-level maximum output current <sup>[48]</sup> | –   | –   | –1   | mA    | HSIO, configured for drive_sel<1:0>= 0b10                                                                        |
| SID29D  | I <sub>OH3D_ABS</sub> | HIGH-level maximum output current <sup>[48]</sup> | –   | –   | –0.5 | mA    | HSIO, configured for drive_sel<1:0>= 0b11                                                                        |
| SID30A  | I <sub>OH4A_ABS</sub> | Source maximum current <sup>[48]</sup>            | –   | –   | –4   | mA    | For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode. |
| SID30B  | I <sub>OH4B_ABS</sub> | Source maximum current <sup>[48]</sup>            | –   | –   | –25  | mA    | For pin DRV_VOUT in external transistor mode.                                                                    |

**Notes**

48.The maximum output current is the peak current flowing through any one I/O.

49.The total output current is the maximum current flowing through all GPIO\_STD and GPIO\_ENH I/Os.

**Table 26-1 Absolute maximum ratings (continued)**

| Spec ID | Parameter                    | Description                                                                  | Min  | Typ | Max  | Units | Details/<br>conditions                                                                                           |
|---------|------------------------------|------------------------------------------------------------------------------|------|-----|------|-------|------------------------------------------------------------------------------------------------------------------|
| SID30C  | $I_{OH4C\_ABS}$              | Source average current <sup>[50]</sup>                                       | –    | –   | –1   | mA    | For pin EXT_PS_CTL1 in external PMIC mode and internal regulator mode and pin EXT_PS_CTL2 in external PMIC mode. |
| SID30D  | $I_{OH4D\_ABS}$              | Source average current <sup>[50]</sup>                                       | –    | –   | –12  | mA    | For pin DRV_VOUT in external transistor mode.                                                                    |
| SID33A  | $\Sigma I_{OH\_ABS\_G\_PIO}$ | HIGH-level total output current <sup>[51]</sup>                              | –    | –   | –50  | mA    |                                                                                                                  |
| SID33B  | $\Sigma I_{OH\_ABS\_H\_SIO}$ | HIGH-level total output current <sup>[52]</sup>                              | –    | –   | –85  | mA    |                                                                                                                  |
| SID33D  | PIO                          | Total output power dissipation <sup>[53]</sup>                               | –    | –   | 307  | mW    |                                                                                                                  |
| SID34   | $P_D$                        | Power dissipation for external PMIC/transistor mode                          | –    | –   | 1000 | mW    | $T_J$ should not exceed 150 °C                                                                                   |
| SID34A  | $P_D$                        | Power dissipation for internal regulator mode                                | –    | –   | 2000 | mW    | $T_J$ should not exceed 150 °C                                                                                   |
| SID35   | $T_A$                        | Ambient temperature                                                          | –40  | –   | 105  | °C    | For S-grade devices                                                                                              |
| SID36   | $T_A$                        | Ambient temperature                                                          | –40  | –   | 125  | °C    | For E-grade devices                                                                                              |
| SID37   | $T_{STG}$                    | Storage temperature                                                          | –55  | –   | 150  | °C    |                                                                                                                  |
| SID38   | $T_J$                        | Operating junction temperature                                               | –40  | –   | 150  | °C    |                                                                                                                  |
| SID39A  | $V_{ESD\_HBM}$               | Electrostatic discharge human body model                                     | 2000 | –   | –    | V     |                                                                                                                  |
| SID39B1 | $V_{ESD\_CDM1}$              | Electrostatic discharge charged device model for corner pins                 | 750  | –   | –    | V     |                                                                                                                  |
| SID39B2 | $V_{ESD\_CDM2}$              | Electrostatic discharge charged device model for all other pins              | 500  | –   | –    | V     |                                                                                                                  |
| SID39C  | $I_{LU}$                     | The maximum pin current the device can tolerate before triggering a latch-up | –100 | –   | 100  | mA    |                                                                                                                  |

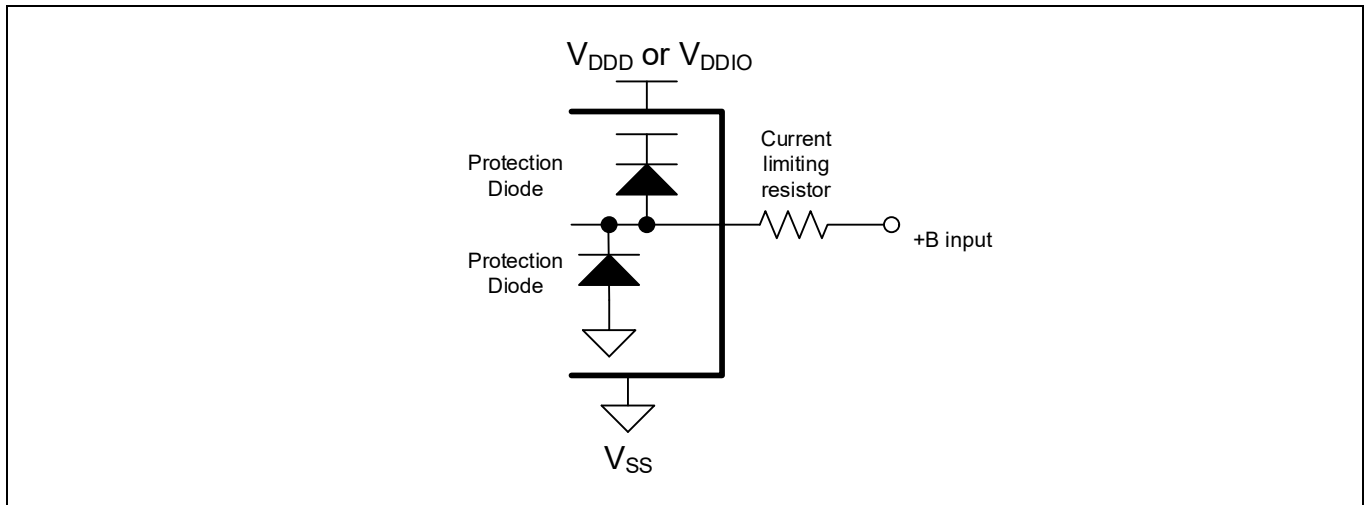
**Notes**

50. The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio. The operation current period over the average current spec should be less than 100 ns.

51. The total output current is the maximum current flowing through all GPIO\_STD and GPIO\_ENH I/Os.

52. The total output current is the maximum current flowing through all HSIO\_STD I/Os.

53. The total output power dissipation is the maximum power dissipation flowing through all I/Os.  $PIO = (V_{DD0}, V_{DDIO\_1}, V_{DDIO\_2}) \times (|\Sigma I_{OH\_ABS\_GPIO}| + |\Sigma I_{OL\_ABS\_GPIO}|) + V_{DDIO\_3} \times (|\Sigma I_{OH\_ABS\_HSIO}| + |\Sigma I_{OL\_ABS\_HSIO}|)$



**Figure 26-1** Example of a recommended circuit<sup>[54]</sup>

**WARNING:**

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current, or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

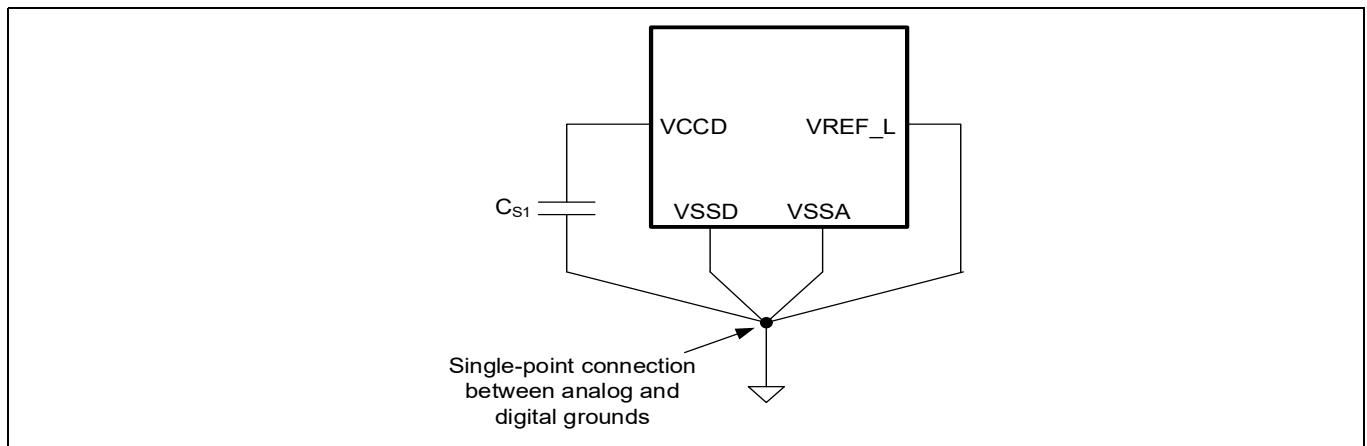
**Note**

54.+B is the positive battery voltage around 45 V.

## 26.2 Device-level specifications

**Table 26-2 Recommended operating conditions**

| Spec ID                                 | Parameter                                                   | Description                                                | Min                 | Typ  | Max                 | Units | Details/conditions                                                        |
|-----------------------------------------|-------------------------------------------------------------|------------------------------------------------------------|---------------------|------|---------------------|-------|---------------------------------------------------------------------------|
| <b>Recommended operating conditions</b> |                                                             |                                                            |                     |      |                     |       |                                                                           |
| SID40                                   | $V_{DDD}$ , $V_{DDA}$ ,<br>$V_{DDIO\_1}$ ,<br>$V_{DDIO\_2}$ | Power supply voltage <sup>[55]</sup>                       | 2.7 <sup>[56]</sup> | –    | 5.5 <sup>[57]</sup> | V     |                                                                           |
| SID40A                                  | $V_{DDIO\_1\_EFP}$                                          | Power supply voltage for eFuse programming <sup>[58]</sup> | 3                   | –    | 5.5                 | V     |                                                                           |
| SID40B                                  | $V_{DDIO\_3}$                                               | Power supply voltage                                       | 2.7                 | –    | 3.6                 | V     |                                                                           |
| SID40C                                  | $V_{CCD}$                                                   | External $V_{CCD}$ power supply                            | 1.10                | 1.15 | 1.20                | V     | External $V_{CCD}$ power supply range when externally supplying $V_{CCD}$ |
| SID41                                   | $C_{S1}$                                                    | Smoothing capacitor <sup>[59, 60]</sup>                    | 6.79                | –    | 22                  | μF    |                                                                           |


**Figure 26-2 Smoothing capacitor**

Smoothing capacitor should be placed as close as possible to the  $V_{CCD}$  pin.

### Notes

55.  $V_{DDD}$ ,  $V_{DDIO\_1}$ ,  $V_{DDIO\_2}$ ,  $V_{DDIO\_3}$ , and  $V_{DDA}$  do not have any sequencing limitation and can establish in any order. These supplies (except  $V_{DDA}$  and  $V_{DDIO\_2}$ ) are independent in voltage level. See 12-Bit SAR ADC DC Specifications when using ADC units.
56. 3.0 V  $\pm 10\%$  is supported with a lower BOD setting option for  $V_{DDD}$  and  $V_{DDA}$ . This setting provides robust protection for internal timing but BOD reset occurs at a voltage below the specified operating conditions. A higher BOD setting option is available (consistent with down to 3.0 V) and guarantees that all operating conditions are met.
57. 5.0 V  $\pm 10\%$  is supported with a higher OVD setting option for  $V_{DDD}$  and  $V_{DDA}$ . This setting provides robust protection for internal and interface timing, but OVD reset occurs at a voltage above the specified operating conditions. A lower OVD setting option is available (consistent with up to 5.0 V) and guarantees that all operating conditions are met. Voltage overshoot to a higher OVD setting range for  $V_{DDD}$  and  $V_{DDA}$  is permissible, provided the duration is less than 2 hours cumulated. Note that during overshoot voltage condition electrical parameters are not guaranteed.
58. eFuse programming must be executed with the part in a “quiet” state, with minimal activity (preferably only JTAG or a single LIN/CAN channel on  $V_{DDD}$  domain, no activity on  $V_{DDIO\_1}$ ).
59. Smoothing capacitor,  $C_{S1}$  is required per chip (not per  $V_{CCD}$  pin). The  $V_{CCD}$  pins must be connected together to ensure a low-impedance connection (see the requirement in [Figure 26-2](#)).
60. Capacitors used for power supply decoupling or filtering are operated under a continuous DC-bias. Many capacitors used with DC power across them provide less than their target capacitance, and their capacitance is not constant across their working voltage range. When selecting capacitors for use with this device, ensure that the selected components provide the required capacitance under the specific operating conditions of temperature and voltage used in your design. While the temperature coefficient is normally found within a part’s catalog (such as, X7R, C0G, Y5V), the matching voltage coefficient may only be available on the component datasheet or direct from the manufacturer. Use of components that do not provide the required capacitance under the actual operating conditions may cause the device to operate to less than datasheet specifications.

## 26.3 DC specifications

**Table 26-3 DC specifications, CPU current, and transition time specifications**

 All specifications are valid for  $-40\text{ °C} \leq T_A \leq 125\text{ °C}$  and for 2.7 V to 5.5 V except where noted.

| Spec ID                  | Parameter                      | Description                                                                                                                     | Min | Typ | Max | Units | Details/conditions                                                                                                                                                                                                                                                                                                                                                                                                                               |
|--------------------------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Active/sleep mode</b> |                                |                                                                                                                                 |     |     |     |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| SID49C14                 | $I_{DD\_VDDD\_CM07\_8\_1\_4M}$ | $V_{DDD}$ current in internal regulator mode, LPACTIVE mode (CM0+ and CM7_0 at 8 MHz, all peripherals are disabled)             | –   | 9   | 13  | mA    | CM0+ and CM7_0 clocked at 8 MHz with IMO. CM7_1 powered off.<br>All peripherals are disabled. No IO toggling. CM0+ and CM7_0 executing Dhrystone from flash with cache enabled.<br>Typ: $T_A = 25\text{ °C}$ ,<br>$V_{DDD} = 5.0\text{ V}$ ,<br>process typ (TT)<br>Max: $T_A = 25\text{ °C}$ ,<br>$V_{DDD} = 5.5\text{ V}$ ,<br>process worst (FF)                                                                                              |
| SID49C4                  | $I_{DD\_VDDD\_CM07\_8\_4M}$    | $V_{DDD}$ current in internal regulator mode, LPACTIVE mode (CM0+ and CM7_0 at 8 MHz, all peripherals are enabled)              | –   | 10  | 141 | mA    | CM0+ and CM7_0 clocked at 8 MHz with IMO. CM7_1 powered off. All peripherals are enabled. No IO toggling.<br>CM0+ and CM7_0 executing Dhrystone from flash with cache enabled. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity.<br>Typ: $T_A = 25\text{ °C}$ ,<br>$V_{DDD} = 5.0\text{ V}$ ,<br>process typ (TT)<br>Max: $T_A = 105\text{ °C}$ ,<br>$V_{DDD} = 5.5\text{ V}$ ,<br>process worst (FF)  |
| SID49G1                  | $I_{DD1\_VCCD\_CM7\_250}$      | $V_{CCD}$ current in external PMIC/transistor mode, Active mode (CM7_0 at 250 MHz, CM0+ at 80 MHz, all peripherals are enabled) | –   | 82  | 240 | mA    | PLL enabled at 250 MHz with ECO reference. All peripherals are enabled. No IO toggling. CM7_1 powered off. CM7_0 and CM0+ executing Dhrystone from flash with cache enabled.<br>M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity.<br>Typ: $T_A = 25\text{ °C}$ ,<br>$V_{DDD} = 5.0\text{ V}$ ,<br>process typ (TT)<br>Max: $T_A = 125\text{ °C}$ ,<br>$V_{DDD} = 5.5\text{ V}$ ,<br>process worst (FF) |

Electrical specifications

**Table 26-3 DC specifications, CPU current, and transition time specifications** (continued)

All specifications are valid for  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$  and for 2.7 V to 5.5 V except where noted.

| Spec ID | Parameter                 | Description                                                                                                                        | Min | Typ | Max | Units | Details/conditions                                                                                                                                                                                                                                                                                                                                                                                                                      |
|---------|---------------------------|------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID49G2 | $I_{DD1\_VDDD\_CM7\_250}$ | $V_{DDD}$ current in external PMIC/transistor mode, Active mode (CM7_0 at 250 MHz, CM0+ at 80 MHz, all peripherals are enabled)    | –   | 7   | 9   | mA    | PLL enabled at 250 MHz with ECO reference. All peripherals are enabled. No IO toggling. CM7_1 powered off. CM7_0 and CM0+ executing Dhrystone from flash with cache enabled. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. Typ: $T_A = 25^{\circ}\text{C}$ , $V_{DDD} = 5.0\text{ V}$ , process typ (TT) Max: $T_A = 125^{\circ}\text{C}$ , $V_{DDD} = 5.5\text{ V}$ , process worst (FF) |
| SID50G1 | $I_{DD1\_VCCD\_F250}$     | $V_{CCD}$ current in external PMIC/transistor mode, Active mode (CM7 CPUs at 250 MHz, CM0+ at 80 MHz, all peripherals are enabled) | –   | 124 | 287 | mA    | PLL enabled at 250 MHz with ECO reference. All peripherals are enabled. No IO toggling. CM7 CPUs and CM0+ executing Dhrystone from flash with cache enabled. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. Typ: $T_A = 25^{\circ}\text{C}$ , $V_{DDD} = 5.0\text{ V}$ , process typ (TT) Max: $T_A = 125^{\circ}\text{C}$ , $V_{DDD} = 5.5\text{ V}$ , process worst (FF)                 |
| SID50G2 | $I_{DD1\_VDDD\_F250}$     | $V_{DDD}$ current in external PMIC/transistor mode, Active mode (CM7 CPUs at 250 MHz, CM0+ at 80 MHz, all peripherals are enabled) | –   | 7   | 9.3 | mA    | PLL enabled at 250 MHz with ECO reference. All peripherals are enabled. No IO toggling. CM7 CPUs and CM0+ executing Dhrystone from flash with cache enabled. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. Typ: $T_A = 25^{\circ}\text{C}$ , $V_{DDD} = 5.0\text{ V}$ , process typ (TT) Max: $T_A = 125^{\circ}\text{C}$ , $V_{DDD} = 5.5\text{ V}$ , process worst (FF)                 |
| SID53A4 | $I_{DD2\_8\_VDDD\_4M}$    | $V_{DDD}$ current in internal regulator mode. CM7_1=OFF, Other CPUs in Sleep                                                       | –   | 7   | 140 | mA    | IMO clocked at 8 MHz. All peripherals, PLL, FLL, peripheral clocks, interrupts, CSV, DMA are disabled. No IO toggling. Typ: $T_A = 25^{\circ}\text{C}$ , $V_{DDD} = 5.0\text{ V}$ , process typ (TT) Max: $T_A = 105^{\circ}\text{C}$ , $V_{DDD} = 5.5\text{ V}$ , process worst (FF)                                                                                                                                                   |

## Electrical specifications

**Table 26-3 DC specifications, CPU current, and transition time specifications** (continued)

 All specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$  and for 2.7 V to 5.5 V except where noted.

| Spec ID               | Parameter        | Description                                                                                                                                                             | Min | Typ | Max | Units         | Details/conditions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----------------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID58A                | $I_{DD\_CWU2}$   | Average current for cyclic wake-up operation. This is the average current for the specified LPACTIVE mode and DeepSleep mode (RTC, WDT, and Event Generator operating). | –   | 60  | 198 | $\mu\text{A}$ | $T_A = 25\text{ }^{\circ}\text{C}$ , 64-KB SRAM retention, Event generator operates with ILO0 in DeepSleep and LP Active, Smart I/O operates with ILO0, CM0+, CM7_0: Retain, CM7_1: OFF.<br>Typ: $V_{DD} = 5.0\text{ V}$ , process typ (TT)<br>Max: $V_{DD} = 5.5\text{ V}$ , process worst (FF)<br>This average current is achieved under the following conditions.<br>1. MCU repetitively goes from DeepSleep to LP Active with a period of 32 ms.<br>2. One of the I/Os is toggled using Smart I/O to activate an external sensor connected to an analog input of A/D in DeepSleep<br>3. After 200 $\mu\text{s}$ delay, the CM7_0 wakes up by Event generator trigger to LP Active mode with IMO and A/D conversion is triggered by software.<br>4. Group A/D conversion is performed on 5 channels with the sampling time of 1 $\mu\text{s}$ each.<br>5. Once the group A/D conversion is finished, and the results fit in the window of the range comparator, the I/O is toggled back by software to de-activate the sensor and the CM7_0 goes back to DeepSleep. |
| <b>DeepSleep mode</b> |                  |                                                                                                                                                                         |     |     |     |               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| SID64A4               | $I_{DD\_DS64A4}$ | 64-KB SRAM retention, ILO0 operation                                                                                                                                    | –   | 50  | 138 | $\mu\text{A}$ | DeepSleep Mode (RTC, WDT and event generator operating, all other peripherals are off except for retention registers)<br>CM0+, CM7_0: Retained<br>$T_A = 25\text{ }^{\circ}\text{C}$<br>Typ: $V_{DD} = 5.0\text{ V}$ , process typ (TT)<br>Max: $V_{DD} = 5.5\text{ V}$ , process worst (FF)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| SID64C                | $I_{DD\_DS64C}$  | 64 KB SRAM retention, ILO0 operation                                                                                                                                    | –   | 1.4 | 5.5 | mA            | DeepSleep Mode steady state at $T_A = 125\text{ }^{\circ}\text{C}$ (RTC, WDT, and event generator operating, all other peripherals are off except for retention registers), CM0+, CM7_0: Retained<br>Typ: $V_{DD} = 5.0\text{ V}$ process worst (TT)<br>Max: $V_{DD} = 5.5\text{ V}$ process worst (FF)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <b>Hibernate mode</b> |                  |                                                                                                                                                                         |     |     |     |               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| SID66                 | $I_{DD\_HIB1}$   | Hibernate Mode                                                                                                                                                          | –   | 8   | –   | $\mu\text{A}$ | ILO0/WDT operating. All other peripherals, and all CPUs are off.<br>$T_A = 25\text{ }^{\circ}\text{C}$ , $V_{DD} = 5.0\text{ V}$ , Process typ (TT)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| SID66A                | $I_{DD\_HIB2}$   | Hibernate Mode                                                                                                                                                          | –   | –   | 180 | $\mu\text{A}$ | ILO0/WDT operating. All other peripherals, and all CPUs are off.<br>$T_A = 125\text{ }^{\circ}\text{C}$ , $V_{DD} = 5.5\text{ V}$ , Process worst (FF)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

## Electrical specifications

**Table 26-3 DC specifications, CPU current, and transition time specifications (continued)**

 All specifications are valid for  $-40\text{ °C} \leq T_A \leq 125\text{ °C}$  and for 2.7 V to 5.5 V except where noted.

| Spec ID                            | Parameter           | Description                                                                                                                       | Min | Typ | Max                | Units | Details/conditions                                                                                                                                                                                                                                                          |
|------------------------------------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------|-----|-----|--------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Power mode transition times</b> |                     |                                                                                                                                   |     |     |                    |       |                                                                                                                                                                                                                                                                             |
| SID69                              | $t_{ACT\_DS}$       | Power down time from Active to DeepSleep                                                                                          | –   | –   | 2.5                | μs    | When the IMO is already running and all HFCLK roots are at least 8 MHz. HFCLK roots that are slower than this will require additional time to turn off.                                                                                                                     |
| SID67                              | $t_{DS\_ACT}$       | DeepSleep to Active transition time (IMO clock)                                                                                   | –   | –   | 10 <sup>[61]</sup> | μs    | When using the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until wakeup.                                                                                                                                                                                     |
| SID67C                             | $t_{DS\_ACT1}$      | DeepSleep to Active transition time (IMO clock, flash execution)                                                                  | –   | –   | 26 <sup>[61]</sup> | μs    | When using the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until flash execution.                                                                                                                                                                            |
| SID67A                             | $t_{DS\_ACT\_FLL}$  | DeepSleep to Active transition time (FLL clock)                                                                                   | –   | –   | 15 <sup>[61]</sup> | μs    | When using the FLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until the FLL locks.                                                                                                                                              |
| SID67D                             | $t_{DS\_ACT\_FLL1}$ | DeepSleep to Active transition time (FLL clock, flash execution)                                                                  | –   | –   | 26 <sup>[61]</sup> | μs    | When using the FLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until flash execution.                                                                                                                                            |
| SID67B                             | $t_{DS\_ACT\_PLL}$  | DeepSleep to Active transition time (PLL clock)                                                                                   | –   | –   | 60 <sup>[61]</sup> | μs    | When using the PLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until the PLL locks.                                                                                                                                              |
| SID68                              | $t_{HVR\_ACT}$      | Release time from HV reset (POR, BOD, OVD, OCD, WDT, Hibernate wakeup, or XRES_L) release until CM0+ begins executing ROM boot    | –   | –   | 265                | μs    | Without boot runtime, guaranteed by design                                                                                                                                                                                                                                  |
| SID68A                             | $t_{LVR\_ACT}$      | Release time from LV reset (Fault, Internal system reset, MCWDT, or CSV) during Active/Sleep until CM0+ begins executing ROM boot | –   | –   | 10                 | μs    | Without boot runtime. Guaranteed by design                                                                                                                                                                                                                                  |
| SID68B                             | $t_{LVR\_DS}$       | Release time from LV reset (Fault, or MCWDT) during DeepSleep until CM0+ begins executing ROM boot                                | –   | –   | 15                 | μs    | Without boot runtime. Guaranteed by design                                                                                                                                                                                                                                  |
| SID80A                             | $t_{RB\_N}$         | ROM boot startup time or wakeup time from hibernate in NORMAL protection state                                                    | –   | –   | 1640               | μs    | Guaranteed by Design, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.554 and later)                                                                                                                                                                                      |
| SID80B                             | $t_{RB\_S}$         | ROM boot startup time or wakeup time from hibernate in SECURE protection state                                                    | –   | –   | 2330               | μs    | Guaranteed by Design, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.554 and later)                                                                                                                                                                                      |
| SID81A                             | $t_{FB}$            | Flash boot startup time or wakeup time from hibernate in NORMAL/SECURE protection state                                           | –   | –   | 80                 | μs    | Guaranteed by Design, TOC2_FLAGS=0x2CF, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.554 and later), Listen window = 0 ms                                                                                                                                              |
| SID81B                             | $t_{FB\_A}$         | Flash boot with app authentication time in NORMAL/SECURE protection state                                                         | –   | –   | 5000               | μs    | Guaranteed by Design, TOC2_FLAGS=0x24F, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.554 and later), Listen window = 0 ms, Public key exponent e = 0x010001, App size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA2K. |

**Note**

 61. At cold temperature  $-5\text{ °C}$  to  $-40\text{ °C}$ , the DeepSleep to Active transition time can be higher than the max time indicated by as much as 20 μs.

## Electrical specifications

**Table 26-3 DC specifications, CPU current, and transition time specifications** *(continued)*

 All specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$  and for 2.7 V to 5.5 V except where noted.

| Spec ID  | Parameter      | Description                                                                             | Min | Typ | Max   | Units         | Details/conditions                                                                                                                                                                                                                                                            |
|----------|----------------|-----------------------------------------------------------------------------------------|-----|-----|-------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID80A_2 | $t_{RB\_N\_2}$ | ROM boot startup time or wakeup time from hibernate in NORMAL protection state          | –   | –   | 2640  | $\mu\text{s}$ | Guaranteed by Design, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.554)                                                                                                                                                                                      |
| SID80B_2 | $t_{RB\_S\_2}$ | ROM boot startup time or wakeup time from hibernate in SECURE protection state          | –   | –   | 3890  | $\mu\text{s}$ | Guaranteed by Design, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.554)                                                                                                                                                                                      |
| SID81A_2 | $t_{FB\_2}$    | Flash boot startup time or wakeup time from hibernate in NORMAL/SECURE protection state | –   | –   | 200   | $\mu\text{s}$ | Guaranteed by Design, TOC2_FLAGS=0x2CF, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.554), Listen window = 0 ms                                                                                                                                              |
| SID81B_2 | $t_{FB\_A\_2}$ | Flash boot with app authentication time in NORMAL/SECURE protection state               | –   | –   | 10000 | $\mu\text{s}$ | Guaranteed by Design, TOC2_FLAGS=0x24F, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.554), Listen window = 0 ms, Public key exponent e = 0x010001, App size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA2K. |

**Regulator specifications**

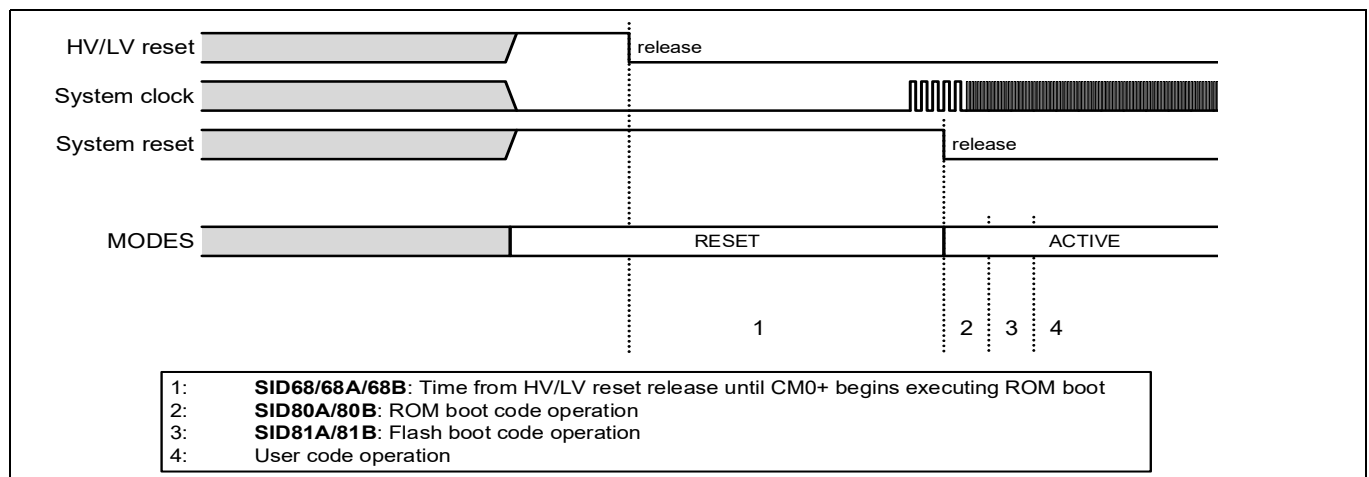
|         |                  |                                                                             |                       |     |                      |               |                                                                                                                      |
|---------|------------------|-----------------------------------------------------------------------------|-----------------------|-----|----------------------|---------------|----------------------------------------------------------------------------------------------------------------------|
| SID600  | $V_{CCD}$        | Core supply voltage (transient range)                                       | 1.05                  | 1.1 | 1.15                 | V             |                                                                                                                      |
| SID600A | $V_{CCD\_S}$     | Core supply voltage (static range, no load)                                 | 1.075                 | 1.1 | 1.125                | V             | Guaranteed by design                                                                                                 |
| SID601  | $I_{DDD\_ACT}$   | Regulator operating current in Active/Sleep mode                            | –                     | 900 | 1500                 | $\mu\text{A}$ | Guaranteed by design                                                                                                 |
| SID602  | $I_{DDD\_DPSLP}$ | Regulator operating current in DeepSleep mode                               | –                     | 1.5 | 20                   | $\mu\text{A}$ | Guaranteed by design                                                                                                 |
| SID603  | $I_{RUSH}$       | In-rush current                                                             | –                     | –   | 850                  | mA            | Average $V_{DDP}$ current until $C_{S1}$ (connected to $V_{CCD}$ pin) is charged after Active regulator is turned on |
| SID604  | $I_{ILDOUT}$     | Internal regulator output current for operation                             | –                     | –   | 300                  | mA            |                                                                                                                      |
| SID605  | $I_{HCROUT}$     | High current regulator output current for operation                         | –                     | –   | 600                  | mA            | Using an external pass transistor                                                                                    |
| SID606  | $V_{OL\_HCR}$    | Output voltage LOW level for external PMIC enable output (EXT_PS_CTL1)      | –                     | –   | 0.5                  | V             | $I_{OL} = 1\text{ mA}$                                                                                               |
| SID606A | $V_{OH\_HCR}$    | Output voltage HIGH level for external PMIC enable output (EXT_PS_CTL1)     | $V_{DDP} - 0.5$       | –   | –                    | V             | $I_{OH} = -1\text{ mA}$                                                                                              |
| SID607  | $V_{IH\_HCR}$    | Input voltage HIGH threshold for external PMIC power OK input (EXT_PS_CTL0) | $0.7 \times V_{DDP}$  | –   | –                    | V             |                                                                                                                      |
| SID607A | $V_{IL\_HCR}$    | Input voltage LOW threshold for external PMIC power OK input (EXT_PS_CTL0)  | –                     | –   | $0.3 \times V_{DDP}$ | V             |                                                                                                                      |
| SID607B | $V_{HYS\_HCR}$   | Hysteresis for external PMIC power OK input (EXT_PS_CTL0)                   | $0.05 \times V_{DDP}$ | –   | –                    | V             |                                                                                                                      |
| SID608  | $I_{DRV\_OUT}$   | DRV_VOUT pin output current to external NPN base current                    | –                     | –   | 9                    | mA            | See Architecture TRM for external NPN transistor selection                                                           |

## 26.4 Reset specifications

All specifications are valid for  $-40\text{ °C} \leq T_A \leq 125\text{ °C}$  and for 2.7 V to 5.5 V except where noted.

**Table 26-4 XRES\_L reset**

| Spec ID                         | Parameter       | Description                                 | Min                  | Typ | Max                 | Units | Details/conditions                                                                                             |
|---------------------------------|-----------------|---------------------------------------------|----------------------|-----|---------------------|-------|----------------------------------------------------------------------------------------------------------------|
| <b>XRES_L DC specifications</b> |                 |                                             |                      |     |                     |       |                                                                                                                |
| SID73                           | $I_{DD\_XRES}$  | $I_{DD}$ when XRES_L asserted               | –                    | –   | 2.5                 | mA    | Max: $T_A = 125\text{ °C}$ ,<br>$V_{DD} = 5.5\text{ V}$ ,<br>$V_{CCD} = 1.15\text{ V}$ ,<br>process worst (FF) |
| SID74                           | $V_{IH}$        | Input voltage HIGH threshold                | $0.7 \times V_{DD}$  | –   | –                   | V     | CMOS Input                                                                                                     |
| SID75                           | $V_{IL}$        | Input voltage LOW threshold                 | –                    | –   | $0.3 \times V_{DD}$ | V     | CMOS Input                                                                                                     |
| SID76                           | $R_{PULLUP}$    | Pull-up resistor                            | 7                    | –   | 20                  | kΩ    |                                                                                                                |
| SID77                           | $C_{IN}$        | Input capacitance                           | –                    | –   | 5                   | pF    |                                                                                                                |
| SID78                           | $V_{HYSXRES}$   | Input voltage hysteresis                    | $0.05 \times V_{DD}$ | –   | –                   | V     |                                                                                                                |
| <b>XRES_L AC specifications</b> |                 |                                             |                      |     |                     |       |                                                                                                                |
| SID70                           | $t_{XRES\_ACT}$ | XRES_L deasserted to Active transition time | –                    | –   | 265                 | μs    | Without boot runtime<br>Guaranteed by design                                                                   |
| SID71                           | $t_{XRES\_PW}$  | XRES_L pulse width                          | 5                    | –   | –                   | μs    |                                                                                                                |
| SID72                           | $t_{XRES\_FT}$  | Pulse suppression width                     | 100                  | –   | –                   | ns    |                                                                                                                |


**Figure 26-3 Reset sequence**

## Electrical specifications

## 26.5 I/O

 All specifications are valid for  $-40\text{ °C} \leq T_A \leq 125\text{ °C}$  and for 2.7 V to 5.5 V except where noted.

**Table 26-5 I/O specifications**

| Spec ID                                                             | Parameter                 | Description                               | Min                                                         | Typ | Max | Units      | Details/conditions                                                                                                                                    |
|---------------------------------------------------------------------|---------------------------|-------------------------------------------|-------------------------------------------------------------|-----|-----|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>GPIO_STD specifications for ports P1 through P23, P26 to P32</b> |                           |                                           |                                                             |     |     |            |                                                                                                                                                       |
| SID650                                                              | $V_{OL1\_GPIO\_STD}$      | Output voltage LOW level                  | –                                                           | –   | 0.6 | V          | $I_{OL} = 6\text{ mA}$<br>$drive\_sel<1:0> = 0b0X$ ,<br>$4.5\text{ V} \leq V_{DD} \text{ or } V_{DDIO\_1} \text{ or } V_{DDIO\_2} \leq 5.5\text{ V}$  |
| SID650C                                                             | $V_{OL1C\_GPIO\_STD}$     | Output voltage LOW level                  | –                                                           | –   | 0.4 | V          | $I_{OL} = 5\text{ mA}$<br>$drive\_sel<1:0> = 0b0X$ ,<br>$4.5\text{ V} \leq V_{DD} \text{ or } V_{DDIO\_1} \text{ or } V_{DDIO\_2} \leq 5.5\text{ V}$  |
| SID651                                                              | $V_{OL2\_GPIO\_STD}$      | Output voltage LOW level                  | –                                                           | –   | 0.4 | V          | $I_{OL} = 2\text{ mA}$<br>$drive\_sel<1:0> = 0b0X$ ,<br>$2.7\text{ V} \leq V_{DD} \text{ or } V_{DDIO\_1} \text{ or } V_{DDIO\_2} < 4.5\text{ V}$     |
| SID652                                                              | $V_{OL3\_GPIO\_STD}$      | Output voltage LOW level                  | –                                                           | –   | 0.4 | V          | $I_{OL} = 1\text{ mA}$<br>$drive\_sel<1:0> = 0b10$ ,<br>$2.7\text{ V} \leq V_{DD} \text{ or } V_{DDIO\_1} \text{ or } V_{DDIO\_2} < 4.5\text{ V}$     |
| SID652C                                                             | $V_{OL3C\_GPIO\_STD}$     | Output voltage LOW level                  | –                                                           | –   | 0.4 | V          | $I_{OL} = 2\text{ mA}$<br>$drive\_sel<1:0> = 0b10$ ,<br>$4.5\text{ V} \leq V_{DD} \text{ or } V_{DDIO\_1} \text{ or } V_{DDIO\_2} \leq 5.5\text{ V}$  |
| SID653                                                              | $V_{OL4\_GPIO\_STD}$      | Output voltage LOW level                  | –                                                           | –   | 0.4 | V          | $I_{OL} = 0.5\text{ mA}$<br>$drive\_sel<1:0> = 0b11$ ,<br>$2.7\text{ V} \leq V_{DD} \text{ or } V_{DDIO\_1} \text{ or } V_{DDIO\_2} < 4.5\text{ V}$   |
| SID653C                                                             | $V_{OL4C\_GPIO\_STD}$     | Output voltage LOW level                  | –                                                           | –   | 0.4 | V          | $I_{OL} = 1\text{ mA}$<br>$drive\_sel<1:0> = 0b11$ ,<br>$4.5\text{ V} \leq V_{DD} \text{ or } V_{DDIO\_1} \text{ or } V_{DDIO\_2} \leq 5.5\text{ V}$  |
| SID654                                                              | $V_{OH1\_GPIO\_STD}$      | Output voltage HIGH level                 | $(V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2}) - 0.5$      | –   | –   | V          | $I_{OH} = -2\text{ mA}$<br>$drive\_sel<1:0> = 0b0X$ ,<br>$2.7\text{ V} \leq V_{DD} \text{ or } V_{DDIO\_1} \text{ or } V_{DDIO\_2} < 4.5\text{ V}$    |
| SID655                                                              | $V_{OH2\_GPIO\_STD}$      | Output voltage HIGH level                 | $(V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2}) - 0.5$      | –   | –   | V          | $I_{OH} = -5\text{ mA}$<br>$drive\_sel<1:0> = 0b0X$ ,<br>$4.5\text{ V} \leq V_{DD} \text{ or } V_{DDIO\_1} \text{ or } V_{DDIO\_2} \leq 5.5\text{ V}$ |
| SID656                                                              | $V_{OH3\_GPIO\_STD}$      | Output voltage HIGH level                 | $(V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2}) - 0.5$      | –   | –   | V          | $I_{OH} = -1\text{ mA}$<br>$drive\_sel<1:0> = 0b10$ ,<br>$2.7\text{ V} \leq (V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2}) < 4.5\text{ V}$            |
| SID656C                                                             | $V_{OH3C\_GPIO\_STD}$     | Output voltage HIGH level                 | $(V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2}) - 0.5$      | –   | –   | V          | $I_{OH} = -2\text{ mA}$<br>$drive\_sel<1:0> = 0b10$ ,<br>$4.5\text{ V} \leq (V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2}) \leq 5.5\text{ V}$         |
| SID657                                                              | $V_{OH4\_GPIO\_STD}$      | Output voltage HIGH level                 | $(V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2}) - 0.5$      | –   | –   | V          | $I_{OH} = -0.5\text{ mA}$<br>$drive\_sel<1:0> = 0b11$ ,<br>$2.7\text{ V} \leq (V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2}) < 4.5\text{ V}$          |
| SID657C                                                             | $V_{OH4C\_GPIO\_STD}$     | Output voltage HIGH level                 | $(V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2}) - 0.5$      | –   | –   | V          | $I_{OH} = -1\text{ mA}$<br>$drive\_sel<1:0> = 0b11$ ,<br>$4.5\text{ V} \leq (V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2}) \leq 5.5\text{ V}$         |
| SID658                                                              | $R_{PD\_GPIO\_STD}$       | Pull-down resistance                      | 25                                                          | 50  | 100 | k $\Omega$ |                                                                                                                                                       |
| SID659                                                              | $R_{PU\_GPIO\_STD}$       | Pull-up resistance                        | 25                                                          | 50  | 100 | k $\Omega$ |                                                                                                                                                       |
| SID660                                                              | $V_{IH\_CMOS\_GPIO\_STD}$ | Input voltage HIGH threshold in CMOS mode | $0.7 \times (V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2})$ | –   | –   | V          |                                                                                                                                                       |
| SID661                                                              | $V_{IH\_TTL\_GPIO\_STD}$  | Input voltage HIGH threshold in TTL mode  | 2.0                                                         | –   | –   | V          |                                                                                                                                                       |
| SID662                                                              | $V_{IH\_AUTO\_GPIO\_STD}$ | Input voltage HIGH threshold in AUTO mode | $0.8 \times (V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2})$ | –   | –   | V          |                                                                                                                                                       |

## Electrical specifications

**Table 26-5 I/O specifications (continued)**

| Spec ID | Parameter                                                 | Description                                        | Min                                                          | Typ  | Max                                                         | Units | Details/conditions                                                                                                                                                                                                                                                                                                                                                                                       |
|---------|-----------------------------------------------------------|----------------------------------------------------|--------------------------------------------------------------|------|-------------------------------------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID663  | $V_{IL\_CMOS\_GPIO\_STD}$                                 | Input voltage LOW threshold in CMOS mode           | –                                                            | –    | $0.3 \times (V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2})$ | V     |                                                                                                                                                                                                                                                                                                                                                                                                          |
| SID664  | $V_{IL\_TTL\_GPIO\_STD}$                                  | Input voltage LOW threshold in TTL mode            | –                                                            | –    | 0.8                                                         | V     |                                                                                                                                                                                                                                                                                                                                                                                                          |
| SID665  | $V_{IL\_AUTO\_GPIO\_STD}$                                 | Input voltage LOW threshold in AUTO mode           | –                                                            | –    | $0.5 \times (V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2})$ | V     |                                                                                                                                                                                                                                                                                                                                                                                                          |
| SID666  | $V_{HYST\_CMOS\_GPIO\_STD}$                               | Hysteresis in CMOS mode                            | $0.05 \times (V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2})$ | –    | –                                                           | V     |                                                                                                                                                                                                                                                                                                                                                                                                          |
| SID668  | $V_{HYST\_AUTO\_GPIO\_STD}$                               | Hysteresis in AUTO mode                            | $0.05 \times (V_{DD}, V_{DDIO\_1}, \text{ or } V_{DDIO\_2})$ | –    | –                                                           | V     |                                                                                                                                                                                                                                                                                                                                                                                                          |
| SID669  | $C_{in\_GPIO\_STD}$                                       | Input pin capacitance                              | –                                                            | –    | 5                                                           | pF    | For 10 MHz and 100 MHz                                                                                                                                                                                                                                                                                                                                                                                   |
| SID670  | $I_{IL\_GPIO\_STD}$                                       | Input leakage current                              | –250                                                         | 0.02 | 250                                                         | nA    | For GPIO_STD except P21.0, P21.1, P21.2, P21.3, P21.4, P22.1, P22.2, P22.3, P23.3, P23.4.<br>$V_{DDIO\_1} = V_{DDIO\_2} = V_{DD} = V_{DDA} = 5.5\text{ V}$ ,<br>$V_{SSD} < V_I < V_{DD}, V_{DDIO\_1}, V_{DDIO\_2}$<br>$-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$<br>Typ: $T_A = 25\text{ }^{\circ}\text{C}$ , $V_{DDIO\_1} = V_{DDIO\_2} = V_{DD} = V_{DDA} = 5.0\text{ V}$ |
| SID670C | $I_{IL\_GPIO\_STD\_B}$                                    | Input leakage current                              | –700                                                         | 0.02 | 700                                                         | nA    | Only for P21.0, P21.1, P21.2, P21.3, P21.4, P22.1, P22.2, P22.3, P23.3, P23.4.<br>$V_{DDIO\_1} = V_{DDIO\_2} = V_{DD} = V_{DDA} = 5.5\text{ V}$ ,<br>$V_{SSD} < V_I < V_{DD}, V_{DDIO\_1}, V_{DDIO\_2}$<br>$-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$<br>Typ: $T_A = 25\text{ }^{\circ}\text{C}$ , $V_{DDIO\_1} = V_{DDIO\_2} = V_{DD} = V_{DDA} = 5.0\text{ V}$            |
| SID671  | $t_R \text{ or } t_F \text{ (fast)}_{\_20\_0\_GPIO\_STD}$ | Rise time or fall time (10% to 90% of $V_{DDIO}$ ) | 1                                                            | –    | 10                                                          | ns    | 20-pF load, drive_sel<1:0> = 0b00                                                                                                                                                                                                                                                                                                                                                                        |
| SID672  | $t_R \text{ or } t_F \text{ (fast)}_{\_50\_0\_GPIO\_STD}$ | Rise time or fall time (10% to 90% of $V_{DDIO}$ ) | 1                                                            | –    | 20                                                          | ns    | 50-pF load, drive_sel<1:0> = 0b00                                                                                                                                                                                                                                                                                                                                                                        |
| SID673  | $t_R \text{ or } t_F \text{ (fast)}_{\_20\_1\_GPIO\_STD}$ | Rise time or fall time (10% to 90% of $V_{DDIO}$ ) | 1                                                            | –    | 20                                                          | ns    | 20-pF load, drive_sel<1:0> = 0b01                                                                                                                                                                                                                                                                                                                                                                        |
| SID674  | $t_R \text{ or } t_F \text{ (fast)}_{\_10\_2\_GPIO\_STD}$ | Rise time or fall time (10% to 90% of $V_{DDIO}$ ) | 1                                                            | –    | 20                                                          | ns    | 10-pF load, drive_sel<1:0> = 0b10                                                                                                                                                                                                                                                                                                                                                                        |
| SID675  | $t_R \text{ or } t_F \text{ (fast)}_{\_6\_3\_GPIO\_STD}$  | Rise time or fall time (10% to 90% of $V_{DDIO}$ ) | 1                                                            | –    | 20                                                          | ns    | 6-pF load, drive_sel<1:0> = 0b11                                                                                                                                                                                                                                                                                                                                                                         |
| SID676  | $t_F \text{ (fast)}_{\_100\_GPIO\_STD}$                   | Fall time (30% to 70% of $V_{DDIO}$ )              | 0.35                                                         | –    | 250                                                         | ns    | 10-pF to 400-pF load, $R_{PU} = 767\text{ }\Omega$ , drive_sel<1:0> = 0b00, Freq = 100 kHz                                                                                                                                                                                                                                                                                                               |
| SID677  | $t_F \text{ (fast)}_{\_400\_GPIO\_STD}$                   | Fall time (30% to 70% of $V_{DDIO}$ )              | 0.35                                                         | –    | 250                                                         | ns    | 10-pF to 400-pF load, $R_{PU} = 350\text{ }\Omega$ , drive_sel<1:0> = 0b00, Freq = 400 kHz                                                                                                                                                                                                                                                                                                               |
| SID678  | $f_{IN\_GPIO\_STD}$                                       | Input frequency                                    | –                                                            | –    | 100                                                         | MHz   |                                                                                                                                                                                                                                                                                                                                                                                                          |
| SID679  | $f_{OUT\_GPIO\_STD0H}$                                    | Output frequency                                   | –                                                            | –    | 50                                                          | MHz   | 20-pF load, drive_sel<1:0> = 00, $4.5\text{ V} \leq V_{DD} \text{ or } V_{DDIO\_1} \text{ or } V_{DDIO\_2} \leq 5.5\text{ V}$                                                                                                                                                                                                                                                                            |
| SID680  | $f_{OUT\_GPIO\_STD0L}$                                    | Output frequency                                   | –                                                            | –    | 32                                                          | MHz   | 20-pF load, drive_sel<1:0> = 00, $2.7\text{ V} \leq V_{DD} \text{ or } V_{DDIO\_1} \text{ or } V_{DDIO\_2} < 4.5\text{ V}$                                                                                                                                                                                                                                                                               |

Electrical specifications

**Table 26-5 I/O specifications (continued)**

| Spec ID                               | Parameter                  | Description               | Min                   | Typ | Max | Units | Details/conditions                                                                                                  |
|---------------------------------------|----------------------------|---------------------------|-----------------------|-----|-----|-------|---------------------------------------------------------------------------------------------------------------------|
| SID681                                | $f_{OUT\_GPIO\_STD1H}$     | Output frequency          | –                     | –   | 25  | MHz   | 20-pF load,<br>drive_sel<1:0>= 01,<br>4.5 V ≤ V <sub>DD</sub> or V <sub>DDIO_1</sub> or V <sub>DDIO_2</sub> ≤ 5.5 V |
| SID682                                | $f_{OUT\_GPIO\_STD1L}$     | Output frequency          | –                     | –   | 15  | MHz   | 20-pF load,<br>drive_sel<1:0>= 01,<br>2.7 V ≤ V <sub>DD</sub> or V <sub>DDIO_1</sub> or V <sub>DDIO_2</sub> < 4.5 V |
| SID683                                | $f_{OUT\_GPIO\_STD2H}$     | Output frequency          | –                     | –   | 25  | MHz   | 10-pF load,<br>drive_sel<1:0>= 10,<br>4.5 V ≤ V <sub>DD</sub> or V <sub>DDIO_1</sub> or V <sub>DDIO_2</sub> ≤ 5.5 V |
| SID684                                | $f_{OUT\_GPIO\_STD2L}$     | Output frequency          | –                     | –   | 15  | MHz   | 10-pF load,<br>drive_sel<1:0>= 10,<br>2.7 V ≤ V <sub>DD</sub> or V <sub>DDIO_1</sub> or V <sub>DDIO_2</sub> < 4.5 V |
| SID685                                | $f_{OUT\_GPIO\_STD3H}$     | Output frequency          | –                     | –   | 15  | MHz   | 6-pF load,<br>drive_sel<1:0>= 11,<br>4.5 V ≤ V <sub>DD</sub> or V <sub>DDIO_1</sub> or V <sub>DDIO_2</sub> ≤ 5.5 V  |
| SID686                                | $f_{OUT\_GPIO\_STD3L}$     | Output frequency          | –                     | –   | 10  | MHz   | 6-pF load,<br>drive_sel<1:0>= 11,<br>2.7 V ≤ V <sub>DD</sub> or V <sub>DDIO_1</sub> or V <sub>DDIO_2</sub> < 4.5 V  |
| <b>GPIO_ENH specifications for P0</b> |                            |                           |                       |     |     |       |                                                                                                                     |
| SID650A                               | V <sub>OL1_GPIO_ENH</sub>  | Output voltage LOW level  | –                     | –   | 0.6 | V     | I <sub>OL</sub> = 6 mA<br>drive_sel<1:0>= 0b0X,<br>2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V                                  |
| SID650D                               | V <sub>OL1D_GPIO_ENH</sub> | Output voltage LOW level  | –                     | –   | 0.4 | V     | I <sub>OL</sub> = 5 mA<br>drive_sel<1:0>= 0b0X,<br>4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V                                  |
| SID651A                               | V <sub>OL2_GPIO_ENH</sub>  | Output voltage LOW level  | –                     | –   | 0.4 | V     | I <sub>OL</sub> = 2 mA<br>drive_sel<1:0>= 0b0X,<br>2.7 V ≤ V <sub>DD</sub> < 4.5 V                                  |
| SID652A                               | V <sub>OL3_GPIO_ENH</sub>  | Output voltage LOW level  | –                     | –   | 0.4 | V     | I <sub>OL</sub> = 1 mA<br>drive_sel<1:0>= 0b10,<br>2.7 V ≤ V <sub>DD</sub> < 4.5 V                                  |
| SID652D                               | V <sub>OL3D_GPIO_ENH</sub> | Output voltage LOW level  | –                     | –   | 0.4 | V     | I <sub>OL</sub> = 2 mA<br>drive_sel<1:0>= 0b10,<br>4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V                                  |
| SID653A                               | V <sub>OL4_GPIO_ENH</sub>  | Output voltage LOW level  | –                     | –   | 0.4 | V     | I <sub>OL</sub> = 0.5 mA<br>drive_sel<1:0>= 0b11,<br>2.7 V ≤ V <sub>DD</sub> < 4.5 V                                |
| SID653D                               | V <sub>OL4D_GPIO_ENH</sub> | Output voltage LOW level  | –                     | –   | 0.4 | V     | I <sub>OL</sub> = 1 mA<br>drive_sel<1:0>= 0b11,<br>4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V                                  |
| SID654A                               | V <sub>OH1_GPIO_ENH</sub>  | Output voltage HIGH level | V <sub>DD</sub> – 0.5 | –   | –   | V     | I <sub>OH</sub> = –2 mA<br>drive_sel<1:0>= 0b0X,<br>2.7 V ≤ V <sub>DD</sub> < 4.5 V                                 |
| SID655A                               | V <sub>OH2_GPIO_ENH</sub>  | Output voltage HIGH level | V <sub>DD</sub> – 0.5 | –   | –   | V     | I <sub>OH</sub> = –5 mA<br>drive_sel<1:0>= 0b0X,<br>4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V                                 |
| SID656A                               | V <sub>OH3_GPIO_ENH</sub>  | Output voltage HIGH level | V <sub>DD</sub> – 0.5 | –   | –   | V     | I <sub>OH</sub> = –1 mA<br>drive_sel<1:0>= 0b10,<br>2.7 V ≤ V <sub>DD</sub> < 4.5 V                                 |
| SID656D                               | V <sub>OH3D_GPIO_ENH</sub> | Output voltage HIGH level | V <sub>DD</sub> – 0.5 | –   | –   | V     | I <sub>OH</sub> = –2 mA<br>drive_sel<1:0>= 0b10,<br>4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V                                 |
| SID657A                               | V <sub>OH4_GPIO_ENH</sub>  | Output voltage HIGH level | V <sub>DD</sub> – 0.5 | –   | –   | V     | I <sub>OH</sub> = –0.5 mA<br>drive_sel<1:0>= 0b11,<br>2.7 V ≤ V <sub>DD</sub> < 4.5 V                               |
| SID657D                               | V <sub>OH4D_GPIO_ENH</sub> | Output voltage HIGH level | V <sub>DD</sub> – 0.5 | –   | –   | V     | I <sub>OH</sub> = –1 mA<br>drive_sel<1:0>= 0b11,<br>4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V                                 |
| SID658A                               | R <sub>PD_GPIO_ENH</sub>   | Pull-down resistance      | 25                    | 50  | 100 | kΩ    |                                                                                                                     |

## Electrical specifications

**Table 26-5 I/O specifications (continued)**

| Spec ID | Parameter                                                          | Description                                               | Min                        | Typ   | Max                 | Units | Details/conditions                                                                                                                                                                                                   |
|---------|--------------------------------------------------------------------|-----------------------------------------------------------|----------------------------|-------|---------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID659A | R <sub>PU_GPIO_ENH</sub>                                           | Pull-up resistance                                        | 25                         | 50    | 100                 | kΩ    |                                                                                                                                                                                                                      |
| SID660A | V <sub>IH_CMOS_GPIO_ENH</sub>                                      | Input voltage HIGH threshold in CMOS mode                 | $0.7 \times V_{DD}$        | –     | –                   | V     |                                                                                                                                                                                                                      |
| SID661A | V <sub>IH_TTL_GPIO_ENH</sub>                                       | Input voltage HIGH threshold in TTL mode                  | 2.0                        | –     | –                   | V     |                                                                                                                                                                                                                      |
| SID662A | V <sub>IH_AUTO_GPIO_ENH</sub>                                      | Input voltage HIGH threshold in AUTO mode                 | $0.8 \times V_{DD}$        | –     | –                   | V     |                                                                                                                                                                                                                      |
| SID663A | V <sub>IL_CMOS_GPIO_ENH</sub>                                      | Input voltage LOW threshold in CMOS mode                  | –                          | –     | $0.3 \times V_{DD}$ | V     |                                                                                                                                                                                                                      |
| SID664A | V <sub>IL_TTL_GPIO_ENH</sub>                                       | Input voltage LOW threshold in TTL mode                   | –                          | –     | 0.8                 | V     |                                                                                                                                                                                                                      |
| SID665A | V <sub>IL_AUTO_GPIO_ENH</sub>                                      | Input voltage LOW threshold in AUTO mode                  | –                          | –     | $0.5 \times V_{DD}$ | V     |                                                                                                                                                                                                                      |
| SID666A | V <sub>HYST_CMOS_GPIO_ENH</sub>                                    | Hysteresis in CMOS mode                                   | $0.05 \times V_{DD}$       | –     | –                   | V     |                                                                                                                                                                                                                      |
| SID668A | V <sub>HYST_AUTO_GPIO_ENH</sub>                                    | Hysteresis in AUTO mode                                   | $0.05 \times V_{DD}$       | –     | –                   | V     |                                                                                                                                                                                                                      |
| SID669A | C <sub>in_GPIO_ENH</sub>                                           | Input pin capacitance                                     | –                          | –     | 5                   | pF    | For 10 MHz and 100 MHz                                                                                                                                                                                               |
| SID670A | I <sub>IL_GPIO_ENH</sub>                                           | Input leakage current                                     | –350                       | 0.055 | 350                 | nA    | V <sub>DD</sub> = V <sub>DDA</sub> = 5.5 V,<br>V <sub>SSD</sub> < V <sub>I</sub> < V <sub>DD</sub><br>–40 °C ≤ T <sub>A</sub> ≤ 125 °C<br>Typ: T <sub>A</sub> = 25 °C,<br>V <sub>DD</sub> = V <sub>DDA</sub> = 5.0 V |
| SID671A | t <sub>R</sub> or t <sub>F</sub> (fast) <sub>_20_0_G-PIO_ENH</sub> | Rise time or fall time (10% to 90% of V <sub>DDIO</sub> ) | 1                          | –     | 10                  | ns    | 20-pF load, drive_sel<1:0> = 0b00, slow = 0                                                                                                                                                                          |
| SID672A | t <sub>R</sub> or t <sub>F</sub> (fast) <sub>_50_0_G-PIO_ENH</sub> | Rise time or fall time (10% to 90% of V <sub>DDIO</sub> ) | 1                          | –     | 20                  | ns    | 50-pF load, drive_sel<1:0> = 0b00, slow = 0                                                                                                                                                                          |
| SID673A | t <sub>R</sub> or t <sub>F</sub> (fast) <sub>_20_1_G-PIO_ENH</sub> | Rise time or fall time (10% to 90% of V <sub>DDIO</sub> ) | 1                          | –     | 20                  | ns    | 20-pF load, drive_sel<1:0> = 0b01, slow = 0                                                                                                                                                                          |
| SID674A | t <sub>R</sub> or t <sub>F</sub> (fast) <sub>_10_2_G-PIO_ENH</sub> | Rise time or fall time (10% to 90% of V <sub>DDIO</sub> ) | 1                          | –     | 20                  | ns    | 10-pF load, drive_sel<1:0> = 0b10, slow = 0                                                                                                                                                                          |
| SID675A | t <sub>R</sub> or t <sub>F</sub> (fast) <sub>_6_3_G-PIO_ENH</sub>  | Rise time or fall time (10% to 90% of V <sub>DDIO</sub> ) | 1                          | –     | 20                  | ns    | 6-pF load, drive_sel<1:0> = 0b11, slow = 0                                                                                                                                                                           |
| SID676A | t <sub>F</sub> <sub>I2C</sub> (slow) <sub>_GPIO_ENH</sub>          | Fall time (30% to 70% of V <sub>DDIO</sub> )              | $20 \times (V_{DD} / 5.5)$ | –     | 250                 | ns    | 10-pF to 400-pF load,<br>drive_sel<1:0> = 0b00,<br>slow = 1,<br>minimum R <sub>PU</sub> = 400 Ω                                                                                                                      |
| SID677A | t <sub>R</sub> or t <sub>F</sub> (slow) <sub>_20_G-PIO_ENH</sub>   | Rise time or fall time (10% to 90% of V <sub>DDIO</sub> ) | $20 \times (V_{DD} / 5.5)$ | –     | 160                 | ns    | 20-pF load, drive_sel<1:0> = 0b00, slow = 1,<br>output frequency = 1 MHz                                                                                                                                             |
| SID678A | t <sub>R</sub> or t <sub>F</sub> (slow) <sub>_400_G-PIO_ENH</sub>  | Rise time or fall time (10% to 90% of V <sub>DDIO</sub> ) | $20 \times (V_{DD} / 5.5)$ | –     | 250                 | ns    | 400-pF load, drive_sel<1:0> = 0b00, slow = 1, output frequency = 400 kHz                                                                                                                                             |
| SID679A | f <sub>IN_GPIO_ENH</sub>                                           | Input frequency                                           | –                          | –     | 100                 | MHz   |                                                                                                                                                                                                                      |
| SID680A | f <sub>OUT_GPIO_ENH0H</sub>                                        | Output frequency                                          | –                          | –     | 50                  | MHz   | 20-pF load,<br>drive_sel<1:0> = 0b00,<br>4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V                                                                                                                                             |
| SID681A | f <sub>OUT_GPIO_ENH0L</sub>                                        | Output frequency                                          | –                          | –     | 32                  | MHz   | 20-pF load,<br>drive_sel<1:0> = 0b00,<br>2.7 V ≤ V <sub>DD</sub> < 4.5 V                                                                                                                                             |
| SID682A | f <sub>OUT_GPIO_ENH1H</sub>                                        | Output frequency                                          | –                          | –     | 25                  | MHz   | 20-pF load,<br>drive_sel<1:0> = 0b01,<br>4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V                                                                                                                                             |
| SID683A | f <sub>OUT_GPIO_ENH1L</sub>                                        | Output frequency                                          | –                          | –     | 15                  | MHz   | 20-pF load,<br>drive_sel<1:0> = 0b01,<br>2.7 V ≤ V <sub>DD</sub> < 4.5 V                                                                                                                                             |
| SID684A | f <sub>OUT_GPIO_ENH2H</sub>                                        | Output frequency                                          | –                          | –     | 25                  | MHz   | 10-pF load,<br>drive_sel<1:0> = 0b10,<br>4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V                                                                                                                                             |

Electrical specifications

**Table 26-5 I/O specifications (continued)**

| Spec ID                                       | Parameter                | Description                                                   | Min                                                 | Typ | Max                         | Units | Details/conditions                                                                |
|-----------------------------------------------|--------------------------|---------------------------------------------------------------|-----------------------------------------------------|-----|-----------------------------|-------|-----------------------------------------------------------------------------------|
| SID685A                                       | $f_{OUT\_GPIO\_ENH2L}$   | Output frequency                                              | –                                                   | –   | 15                          | MHz   | 10-pF load,<br>drive_sel<1:0>= 0b10,<br>2.7 V ≤ V <sub>DD</sub> < 4.5 V           |
| SID686A                                       | $f_{OUT\_GPIO\_ENH3H}$   | Output frequency                                              | –                                                   | –   | 15                          | MHz   | 6-pF load,<br>drive_sel<1:0>= 0b11,<br>4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V            |
| SID687A                                       | $f_{OUT\_GPIO\_ENH3L}$   | Output frequency                                              | –                                                   | –   | 10                          | MHz   | 6-pF load,<br>drive_sel<1:0>= 0b11,<br>2.7 V ≤ V <sub>DD</sub> < 4.5 V            |
| <b>HSIO specifications for ports P24, P25</b> |                          |                                                               |                                                     |     |                             |       |                                                                                   |
| SID651B                                       | V <sub>OL_HB_HSSPI</sub> | Output LOW voltage                                            | –                                                   | –   | 0.2                         | V     | I <sub>OL</sub> = 0.1 mA,<br>drive_sel<1:0>= 0b00                                 |
| SID652B                                       | V <sub>OL_eMMC</sub>     | Output LOW voltage                                            | –                                                   | –   | 0.125 × V <sub>DDIO_3</sub> | V     | I <sub>OL</sub> = 0.1 mA,<br>drive_sel<1:0>= 0b00                                 |
| SID653B                                       | V <sub>OL_SD</sub>       | Output LOW voltage                                            | –                                                   | –   | 0.125 × V <sub>DDIO_3</sub> | V     | I <sub>OL</sub> = 2 mA,<br>drive_sel<1:0>= 0b00                                   |
| SID654B                                       | V <sub>OL1</sub>         | Output LOW voltage                                            | –                                                   | –   | 0.4                         | V     | I <sub>OL</sub> = 10 mA,<br>drive_sel<1:0>= 0b00,<br>V <sub>DDIO_3</sub> = 2.7 V  |
| SID655B                                       | V <sub>OL2</sub>         | Output LOW voltage                                            | –                                                   | –   | 0.4                         | V     | I <sub>OL</sub> = 2 mA,<br>drive_sel<1:0>= 0b01,<br>V <sub>DDIO_3</sub> = 2.7 V   |
| SID656B                                       | V <sub>OL3</sub>         | Output LOW voltage                                            | –                                                   | –   | 0.4                         | V     | I <sub>OL</sub> = 1 mA,<br>drive_sel<1:0>= 0b10,<br>V <sub>DDIO_3</sub> = 2.7 V   |
| SID656E                                       | V <sub>OL4</sub>         | Output LOW voltage                                            | –                                                   | –   | 0.4                         | V     | I <sub>OL</sub> = 0.5 mA,<br>drive_sel<1:0>= 0b11,<br>V <sub>DDIO_3</sub> = 2.7 V |
| SID658B                                       | V <sub>OH_HB_HSSPI</sub> | Output HIGH voltage                                           | V <sub>DDIO_3</sub> – 0.2                           | –   | –                           | V     | I <sub>OH</sub> = –0.1 mA<br>drive_sel<1:0>= 0b00                                 |
| SID659B                                       | V <sub>OH_eMMC</sub>     | Output HIGH voltage                                           | V <sub>DDIO_3</sub> – (0.25 × V <sub>DDIO_3</sub> ) | –   | –                           | V     | I <sub>OH</sub> = –0.1 mA<br>drive_sel<1:0>= 0b00                                 |
| SID660B                                       | V <sub>OH_SD</sub>       | Output HIGH voltage                                           | V <sub>DDIO_3</sub> – (0.25 × V <sub>DDIO_3</sub> ) | –   | –                           | V     | I <sub>OH</sub> = –2 mA<br>drive_sel<1:0>= 0b00                                   |
| SID661B                                       | V <sub>OH1</sub>         | Output HIGH voltage                                           | V <sub>DDIO_3</sub> – 0.5                           | –   | –                           | V     | I <sub>OH</sub> = –10 mA<br>drive_sel<1:0>= 0b00,<br>V <sub>DDIO_3</sub> = 2.7 V  |
| SID662B                                       | V <sub>OH2</sub>         | Output HIGH voltage                                           | V <sub>DDIO_3</sub> – 0.5                           | –   | –                           | V     | I <sub>OH</sub> = –2 mA<br>drive_sel<1:0>= 0b01,<br>V <sub>DDIO_3</sub> = 2.7 V   |
| SID663B                                       | V <sub>OH3</sub>         | Output HIGH voltage                                           | V <sub>DDIO_3</sub> – 0.5                           | –   | –                           | V     | I <sub>OH</sub> = –1 mA<br>drive_sel<1:0>= 0b10,<br>V <sub>DDIO_3</sub> = 2.7 V   |
| SID663E                                       | V <sub>OH4</sub>         | Output HIGH voltage                                           | V <sub>DDIO_3</sub> – 0.5                           | –   | –                           | V     | I <sub>OH</sub> = –0.5 mA<br>drive_sel<1:0>= 0b11,<br>V <sub>DDIO_3</sub> = 2.7 V |
| SID664B                                       | R <sub>PD</sub>          | Pull-down resistance                                          | 25                                                  | 50  | 100                         | kΩ    |                                                                                   |
| SID665B                                       | R <sub>PU</sub>          | Pull-up resistance                                            | 25                                                  | 50  | 100                         | kΩ    |                                                                                   |
| SID666B                                       | V <sub>IH_CMOS</sub>     | Input HIGH voltage for<br>HYPERBUS™ and HSSPI in<br>CMOS mode | 0.7 × V <sub>DDIO_3</sub>                           | –   | –                           | V     | vtrip_sel<1:0>= 0b00                                                              |
| SID668E                                       | V <sub>IH_TTL</sub>      | Input Voltage HIGH<br>threshold for TTL mode                  | 2                                                   | –   | –                           | V     | vtrip_sel<1:0>= 0b01                                                              |
| SID669B                                       | V <sub>IH_SD_eMMC</sub>  | Input HIGH voltage for SD<br>and eMMC in CMOS mode            | 0.625 × V <sub>DDIO_3</sub>                         | –   | –                           | V     | vtrip_sel<1:0>= 0b00                                                              |
| SID669E                                       | V <sub>IH_AUTO</sub>     | Input Voltage HIGH<br>threshold in AUTO mode                  | 0.8 × V <sub>DDIO_3</sub>                           | –   | –                           | V     | vtrip_sel<1:0>= 0b10                                                              |
| SID670B                                       | V <sub>IL_CMOS</sub>     | Input LOW voltage for<br>HYPERBUS™ and HSSPI in<br>CMOS mode  | –                                                   | –   | 0.3 × V <sub>DDIO_3</sub>   | V     | vtrip_sel<1:0>= 0b00                                                              |

## Electrical specifications

**Table 26-5 I/O specifications (continued)**

| Spec ID                          | Parameter            | Description                                    | Min                       | Typ  | Max                       | Units | Details/conditions                                                                                                                                                                                                          |
|----------------------------------|----------------------|------------------------------------------------|---------------------------|------|---------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID672E                          | $V_{IL\_TTL}$        | Input Voltage LOW threshold for TTL mode       | –                         | –    | 0.8                       | V     | $vtrip\_sel<1:0> = 0b01$                                                                                                                                                                                                    |
| SID673B                          | $V_{IL\_SD\_eMMC}$   | Input LOW voltage for SD and eMMC in CMOS mode | –                         | –    | $0.25 \times V_{DDIO\_3}$ | V     | $vtrip\_sel<1:0> = 0b00$                                                                                                                                                                                                    |
| SID673E                          | $V_{IL\_AUTO}$       | Input Voltage LOW threshold in AUTO mode       | –                         | –    | $0.5 \times V_{DDIO\_3}$  | V     | $vtrip\_sel<1:0> = 0b10$                                                                                                                                                                                                    |
| SID674B                          | $V_{HYST\_CMOS}$     | Hysteresis in CMOS mode                        | $0.05 \times V_{DDIO\_3}$ | –    | –                         | V     | $vtrip\_sel<1:0> = 0b00$                                                                                                                                                                                                    |
| SID674F                          | $V_{HYST\_AUTO}$     | Hysteresis in AUTO mode                        | $0.05 \times V_{DDIO\_3}$ | –    | –                         | V     | $vtrip\_sel<1:0> = 0b10$                                                                                                                                                                                                    |
| SID675B                          | $C_{IN}$             | Input pin capacitance                          | –                         | –    | 5                         | pF    | For 10 MHz and 100 MHz                                                                                                                                                                                                      |
| SID676B                          | $I_{IL}$             | Input leakage current                          | –450                      | 1.02 | 450                       | nA    | $V_{DDIO\_3} = 3.6\text{ V}$ ,<br>$V_{SSIO\_3} < V_I < V_{DDIO\_3}$<br>$-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$<br>Typ: $T_A = 25\text{ }^{\circ}\text{C}$ ,<br>$V_{DDIO\_3} = 3.3\text{ V}$ |
| SID679B                          | $f_{IN\_HB\_HSSPI}$  | Input frequency                                | –                         | –    | 100                       | MHz   |                                                                                                                                                                                                                             |
| SID680B                          | $f_{IN\_eMMC}$       | Input frequency                                | –                         | –    | 52                        | MHz   |                                                                                                                                                                                                                             |
| SID681B                          | $f_{IN\_SD}$         | Input frequency                                | –                         | –    | 50                        | MHz   |                                                                                                                                                                                                                             |
| SID683B                          | $f_{OUT\_HB\_HSSPI}$ | Output frequency                               | –                         | –    | 100                       | MHz   |                                                                                                                                                                                                                             |
| SID684B                          | $f_{OUT\_eMMC}$      | Output frequency                               | –                         | –    | 52                        | MHz   |                                                                                                                                                                                                                             |
| SID685B                          | $f_{OUT\_SD}$        | Output frequency                               | –                         | –    | 50                        | MHz   |                                                                                                                                                                                                                             |
| <b>GPIO input specifications</b> |                      |                                                |                           |      |                           |       |                                                                                                                                                                                                                             |
| SID98                            | $t_{FT}$             | Analog glitch filter (pulse suppression width) | –                         | –    | 50 <sup>[62]</sup>        | ns    | One filter per port                                                                                                                                                                                                         |
| SID99                            | $t_{INT}$            | Minimum pulse width for GPIO interrupt         | 160                       | –    | –                         | ns    |                                                                                                                                                                                                                             |

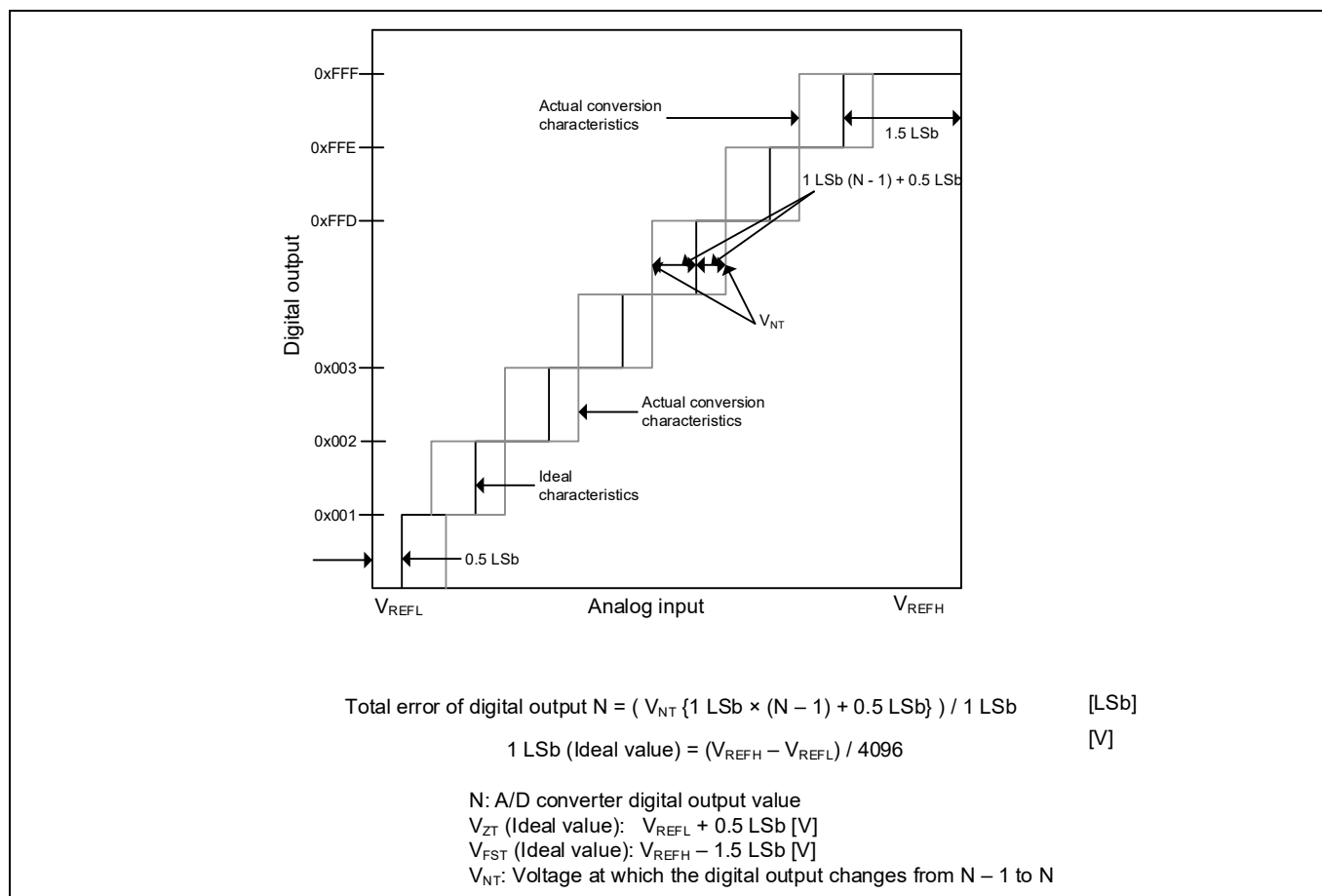
**Note**

62.If a longer pulse suppression width is necessary, use Smart I/O.

## 26.6 Analog peripherals

All specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$  and for 2.7 V to 5.5 V except where noted.

### 26.6.1 SAR ADC



**Figure 26-4 ADC characteristics and error descriptions**

**Table 26-6 12-Bit SAR ADC DC specifications**

| Spec ID | Parameter                                      | Description                                                                                 | Min               | Typ | Max                          | Units | Details/conditions                                                                                 |
|---------|------------------------------------------------|---------------------------------------------------------------------------------------------|-------------------|-----|------------------------------|-------|----------------------------------------------------------------------------------------------------|
| SID100  | A_RES                                          | SAR ADC resolution                                                                          | –                 | –   | 12                           | bits  |                                                                                                    |
| SID101  | A_V <sub>INS</sub>                             | Input voltage range                                                                         | V <sub>REFL</sub> | –   | V <sub>REFH</sub>            | V     |                                                                                                    |
| SID102A | A_V <sub>D<sub>DDA</sub></sub> <sup>[63]</sup> | V <sub>D<sub>DDA</sub></sub> voltage range                                                  | 2.7               | –   | 5.5                          | V     |                                                                                                    |
| SID102  | A_V <sub>REFH</sub>                            | V <sub>REFH</sub> voltage range                                                             | 2.7               | –   | V <sub>D<sub>DDA</sub></sub> | V     | ADC performance degrades when high reference is higher than supply (V <sub>D<sub>DDA</sub></sub> ) |
| SID103  | A_V <sub>REFL</sub>                            | V <sub>REFL</sub> voltage range                                                             | V <sub>SSA</sub>  | –   | V <sub>SSA</sub>             | V     | ADC performance degrades when low reference is lower than ground                                   |
| SID103A | V <sub>band_gap</sub>                          | Internal band gap reference voltage                                                         | 0.882             | 0.9 | 0.918                        | V     |                                                                                                    |
| SID19A  | CLAMP_COUPLING_RATIO_POS                       | Ratio of current collected on a pin to the positive current injected into a neighboring pin | –                 | –   | 0.1                          | %     |                                                                                                    |
| SID19B  | CLAMP_COUPLING_RATIO_NEG                       | Ratio of current collected on a pin to the negative current injected into a neighboring pin | –                 | –   | 1.2                          | %     |                                                                                                    |
| SID19C  | R <sub>CLAMP_INTERNAL</sub>                    | Internal pin resistance to current collection point                                         | –                 | –   | 50                           | Ω     |                                                                                                    |

## 26.6.2 Calculating the impact of neighboring pins

The three ADC specifications based on SID19A, SID19B, and SID19C, can be used to calculate the pin leakage and resulting ADC offset caused by injection current using the below formula:

$$I_{\text{LEAK}} = I_{\text{INJECTED}} \times \text{CLAMP\_COUPLING\_RATIO}$$

$$V_{\text{ERROR}} = I_{\text{LEAK}} \times (R_{\text{CLAMP\_INTERNAL}} + R_{\text{SOURCE}})$$

$$\text{Code Error} = V_{\text{ERROR}} \times 2^{12} / V_{\text{REF}}$$

Where:

I<sub>INJECTED</sub> is the injected current in mA.

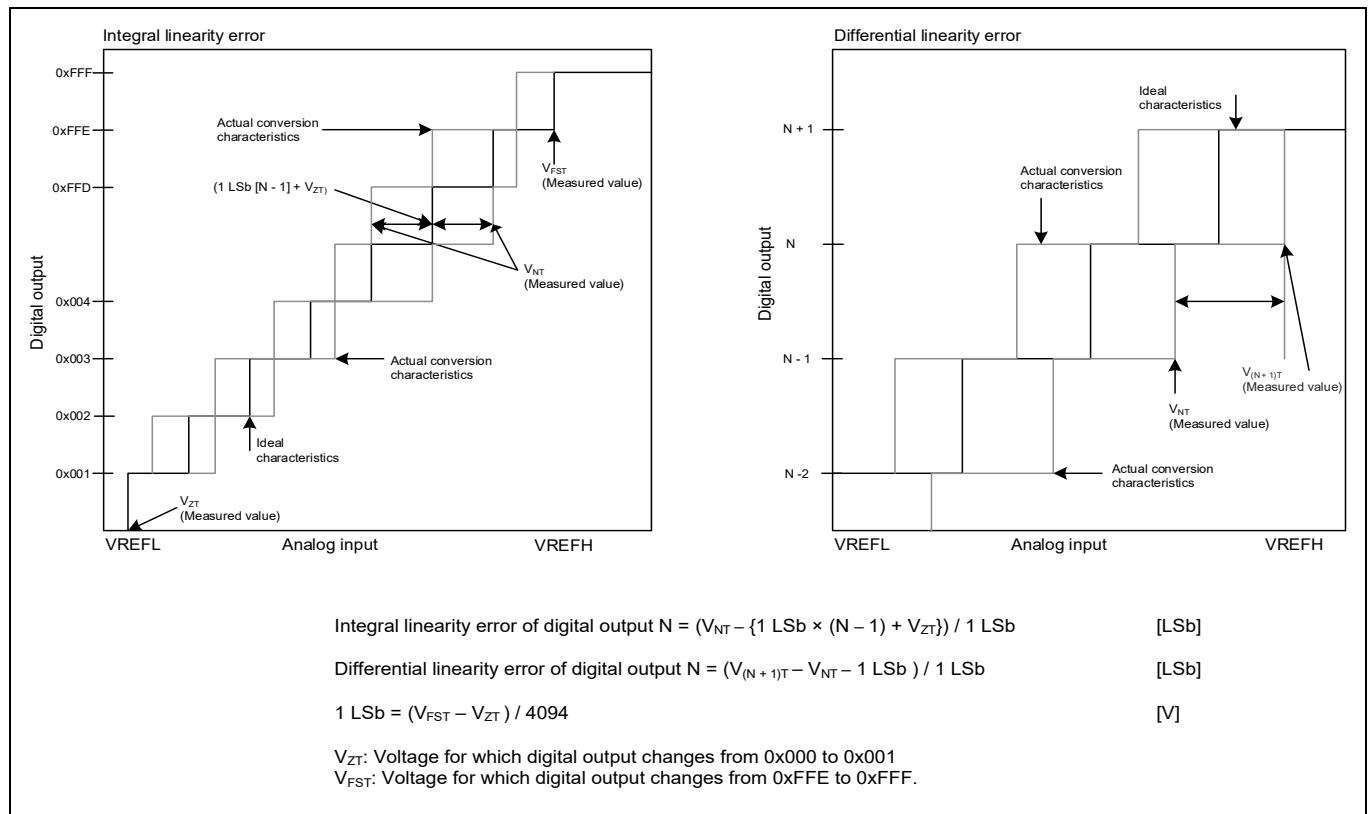
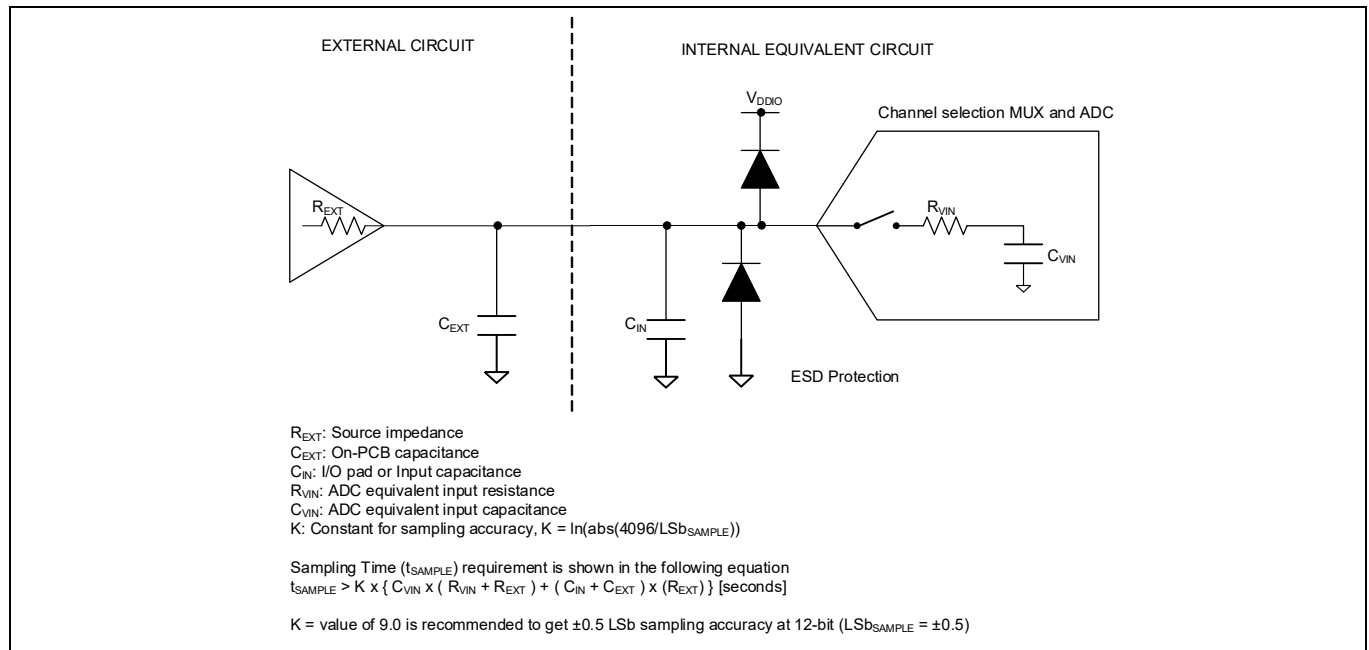
I<sub>LEAK</sub> is the calculated leakage current in mA.

V<sub>ERROR</sub> is the voltage error calculated due to leakage currents in V.

V<sub>REF</sub> is the ADC reference voltage in V.

### Note

63.V<sub>DD<sub>DD</sub></sub> must be greater than 0.8 × V<sub>D<sub>DDA</sub></sub> when ADC[2] is enabled. V<sub>D<sub>DIO\_1</sub></sub> must be greater than 0.8 × V<sub>D<sub>DDA</sub></sub> when ADC[0] is enabled.


**Figure 26-5 Integral and differential linearity errors**

**Figure 26-6 ADC equivalent circuit for analog input**

**Table 26-7 SAR ADC AC specifications**

| Spec ID | Parameter        | Description                                                                                             | Min | Typ | Max   | Units | Details/conditions                                                                                                                                                                                                   |
|---------|------------------|---------------------------------------------------------------------------------------------------------|-----|-----|-------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID104  | $V_{ZT}$         | Zero transition voltage                                                                                 | -20 | -   | 20    | mV    | $V_{DDA} = 2.7 \text{ V to } 5.5 \text{ V}$ ,<br>$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$<br>before offset adjustment                                                                                     |
| SID105  | $V_{FST}$        | Full-scale transition voltage                                                                           | -20 | -   | 20    | mV    | $V_{DDA} = 2.7 \text{ V to } 5.5 \text{ V}$ ,<br>$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$<br>before offset adjustment                                                                                     |
| SID114  | $f_{ADC\_4P5}$   | ADC operating frequency                                                                                 | 2   | -   | 26.67 | MHz   | $4.5 \text{ V} \leq V_{DDA} \leq 5.5 \text{ V}$                                                                                                                                                                      |
| SID114A | $f_{ADC\_2P7}$   | ADC operating frequency                                                                                 | 2   | -   | 13.34 | MHz   | $2.7 \text{ V} \leq V_{DDA} \leq 4.5 \text{ V}$                                                                                                                                                                      |
| SID113  | $t_{S\_4P5}$     | Analog input sample time<br>( $4.5 \text{ V} \leq V_{DDA}$ )                                            | 412 | -   | -     | ns    | $4.5 \text{ V} \leq V_{DDA} \leq 5.5 \text{ V}$ ,<br>guaranteed by design                                                                                                                                            |
| SID113A | $t_{S\_2P7}$     | Analog input sample time<br>( $2.7 \text{ V} \leq V_{DDA}$ )                                            | 600 | -   | -     | ns    | $2.7 \text{ V} \leq V_{DDA} \leq 4.5 \text{ V}$ ,<br>guaranteed by design                                                                                                                                            |
| SID113B | $t_{S\_DR\_4P5}$ | Analog input sample time<br>when input is from<br>diagnostic reference ( $4.5 \text{ V} \leq V_{DDA}$ ) | 2   | -   | -     | μs    | $4.5 \text{ V} \leq V_{DDA} \leq 5.5 \text{ V}$ ,<br>guaranteed by design                                                                                                                                            |
| SID113C | $t_{S\_DR\_2P7}$ | Analog input sample time<br>when input is from<br>diagnostic reference ( $2.7 \text{ V} \leq V_{DDA}$ ) | 2.5 | -   | -     | μs    | $2.7 \text{ V} \leq V_{DDA} \leq 4.5 \text{ V}$ ,<br>guaranteed by design                                                                                                                                            |
| SID113D | $t_{S\_TS}$      | Analog input sample time<br>for temperature sensor                                                      | 7   | -   | -     | μs    | $2.7 \text{ V} \leq V_{DDA} \leq 5.5 \text{ V}$<br>Guaranteed by design                                                                                                                                              |
| SID106  | $t_{ST\_4P5}$    | Max Throughput (samples<br>per second)                                                                  | -   | -   | 1     | Msp/s | $4.5 \text{ V} \leq V_{DDA} \leq 5.5 \text{ V}$ ,<br>80 MHz / 3 = 26.67 MHz,<br>11 sampling cycles,<br>15 conversion cycles                                                                                          |
| SID106A | $t_{ST\_2P7}$    | Max Throughput (samples<br>per second)                                                                  | -   | -   | 0.5   | Msp/s | $2.7 \text{ V} \leq V_{DDA} < 4.5 \text{ V}$<br>80 MHz / 6 = 13.3 MHz,<br>11 sampling cycles,<br>15 conversion cycles                                                                                                |
| SID107  | $C_{VIN}$        | ADC input sampling<br>capacitance                                                                       | -   | -   | 4.8   | pF    | Guaranteed by design                                                                                                                                                                                                 |
| SID108  | $R_{VIN1}$       | Input path ON resistance<br>( $4.5 \text{ V to } 5.5 \text{ V}$ )                                       | -   | -   | 9.4   | kΩ    | Guaranteed by design                                                                                                                                                                                                 |
| SID108A | $R_{VIN2}$       | Input path ON resistance<br>( $2.7 \text{ V to } 4.5 \text{ V}$ )                                       | -   | -   | 13.9  | kΩ    | Guaranteed by design                                                                                                                                                                                                 |
| SID108B | $R_{DREF1}$      | Diagnostic path ON resis-<br>tance ( $4.5 \text{ V to } 5.5 \text{ V}$ )                                | -   | -   | 40    | kΩ    | Guaranteed by design                                                                                                                                                                                                 |
| SID108C | $R_{DREF2}$      | Diagnostic path ON resis-<br>tance ( $2.7 \text{ V to } 4.5 \text{ V}$ )                                | -   | -   | 50    | kΩ    | Guaranteed by design                                                                                                                                                                                                 |
| SID119  | ACC_RLAD         | Diagnostic reference<br>resistor ladder accuracy                                                        | -4  | -   | 4     | %     |                                                                                                                                                                                                                      |
| SID109  | $A_{TE}$         | Total error                                                                                             | -5  | -   | 5     | LSb   | $V_{DDA} = V_{REFH} = 2.7 \text{ V to } 5.5 \text{ V}$ , $V_{REFL} = V_{SSA}$<br>$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$<br>Total Error after offset<br>and gain adjustment at<br>12-bit resolution mode |

**Table 26-7 SAR ADC AC specifications (continued)**

| Spec ID | Parameter        | Description                                                       | Min   | Typ | Max | Units         | Details/conditions                                                                                                                                                                                               |
|---------|------------------|-------------------------------------------------------------------|-------|-----|-----|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID109A | A_TEB            | Total error                                                       | -12   | -   | 12  | LSb           | $V_{DDA} = V_{REFH} = 2.7 \text{ V}$ to $5.5 \text{ V}$ , $V_{REFL} = V_{SSA}$<br>$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$<br>Total error before offset and gain adjustment at 12 bit resolution mode |
| SID110  | A_INL            | Integral nonlinearity                                             | -2.5  | -   | 2.5 | LSb           | $V_{DDA} = 2.7 \text{ V}$ to $5.5 \text{ V}$ ,<br>$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$                                                                                                            |
| SID111  | A_DNL            | Differential nonlinearity                                         | -0.99 | -   | 1.9 | LSb           | $V_{DDA} = 2.7 \text{ V}$ to $5.5 \text{ V}$ ,<br>$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$                                                                                                            |
| SID112  | A_CE             | Channel to channel variation (for channels connected to same ADC) | -1    | -   | 1   | LSb           | $V_{DDA} = 2.7 \text{ V}$ to $5.5 \text{ V}$ ,<br>$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$                                                                                                            |
| SID115  | $I_{AIC}$        | Analog input leakage current                                      | -350  | 70  | 350 | nA            | When input pad is selected for conversion                                                                                                                                                                        |
| SID116  | $I_{DIAGREF}$    | Diagnostic reference current                                      | -     | -   | 70  | $\mu\text{A}$ |                                                                                                                                                                                                                  |
| SID117  | $I_{VDDA}$       | Analog power supply current while ADC is operating                | -     | 360 | 550 | $\mu\text{A}$ | Per enabled ADC                                                                                                                                                                                                  |
| SID117A | $I_{VDDA\_DS}$   | Analog power supply current while ADC is not operating            | -     | 1   | 21  | $\mu\text{A}$ | Per enabled ADC                                                                                                                                                                                                  |
| SID118  | $I_{VREF}$       | Analog reference voltage current while ADC is operating           | -     | 360 | 550 | $\mu\text{A}$ | Per enabled ADC                                                                                                                                                                                                  |
| SID118A | $I_{VREF\_LEAK}$ | Analog reference voltage current while ADC is not operating       | -     | 1.8 | 5   | $\mu\text{A}$ | Per enabled ADC                                                                                                                                                                                                  |

**Table 26-8 Temperature sensor specifications**

| Spec ID | Parameter      | Description                   | Min | Typ | Max | Units            | Details/conditions                                                                                                                                                                                                                                                                                                                                                                                                     |
|---------|----------------|-------------------------------|-----|-----|-----|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID201  | $T_{SENSACC2}$ | Temperature sensor accuracy 2 | -5  | -   | 5   | $^\circ\text{C}$ | $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$<br>This spec is valid when using ADC[0] ( $V_{DDIO\_1}$ ), ADC[1] ( $V_{DDIO\_2}$ ) or ADC[2] ( $V_{DDD}$ ) with the following conditions:<br>a. $3.0 \text{ V} \leq V_{DDD}, V_{DDIO\_1}$ or $V_{DDIO\_2} = V_{DDA} = V_{REFH} \leq 3.6 \text{ V}$<br>or<br>b. $4.5 \text{ V} \leq V_{DDD}, V_{DDIO\_1}$ or $V_{DDIO\_2} = V_{DDA} = V_{REFH} \leq 5.5 \text{ V}$ |
| SID201A | $T_{SENSACC3}$ | Temperature sensor accuracy 3 | -10 | -   | 10  | $^\circ\text{C}$ | $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$<br>This spec is valid when using ADC[0] ( $V_{DDIO\_1}$ ) or ADC[2] ( $V_{DDD}$ ) with the following condition:<br>$2.7 \text{ V} \leq V_{DDD}$ or $V_{DDIO\_1} \leq 5.5 \text{ V}$ and $2.7 \text{ V} \leq V_{DDA} = V_{REFH} \leq 5.5 \text{ V}$ and $0.8 \times V_{DDA} < V_{DDD}$ or $V_{DDIO\_1}$                                                             |

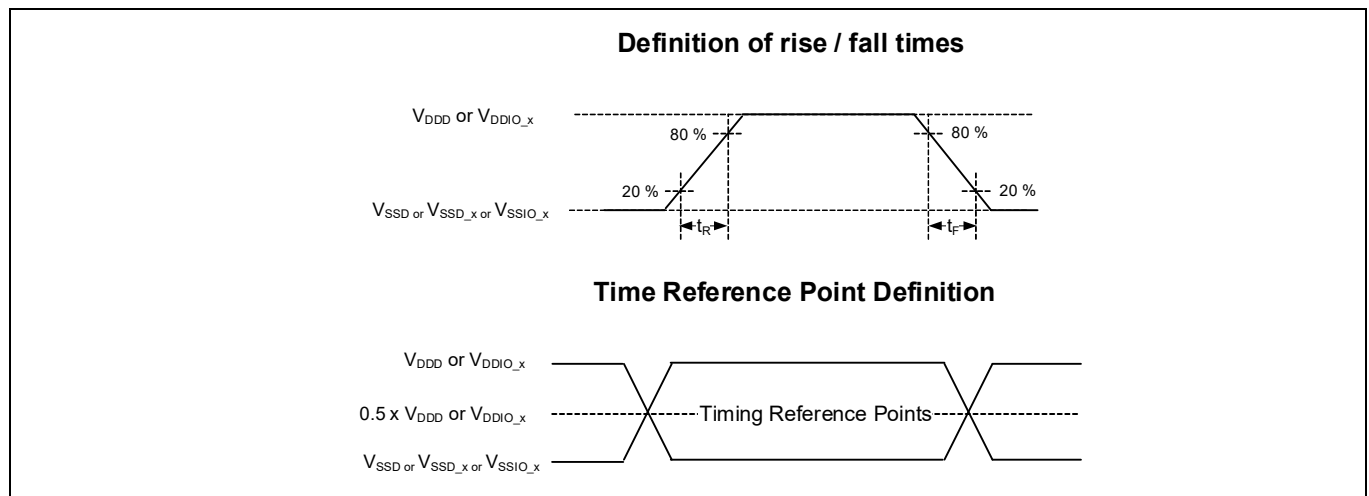
### 26.6.3 Voltage divider accuracy

**Table 26-9 Voltage divider accuracy**

| Spec ID | Parameter    | Description                                                                                | Min | Typ | Max | Units | Details/conditions                                   |
|---------|--------------|--------------------------------------------------------------------------------------------|-----|-----|-----|-------|------------------------------------------------------|
| SID202  | $V_{MONDIV}$ | Uncorrected monitor voltage divider accuracy (measured by ADC), compared to ideal supply/2 | -20 | 2   | 20  | %     | Any HV supply pad within 2.7 V–5.5 V operating range |

### 26.7 AC specifications

Unless otherwise noted, the timings are defined with the guidelines mentioned in the [Figure 26-7](#)



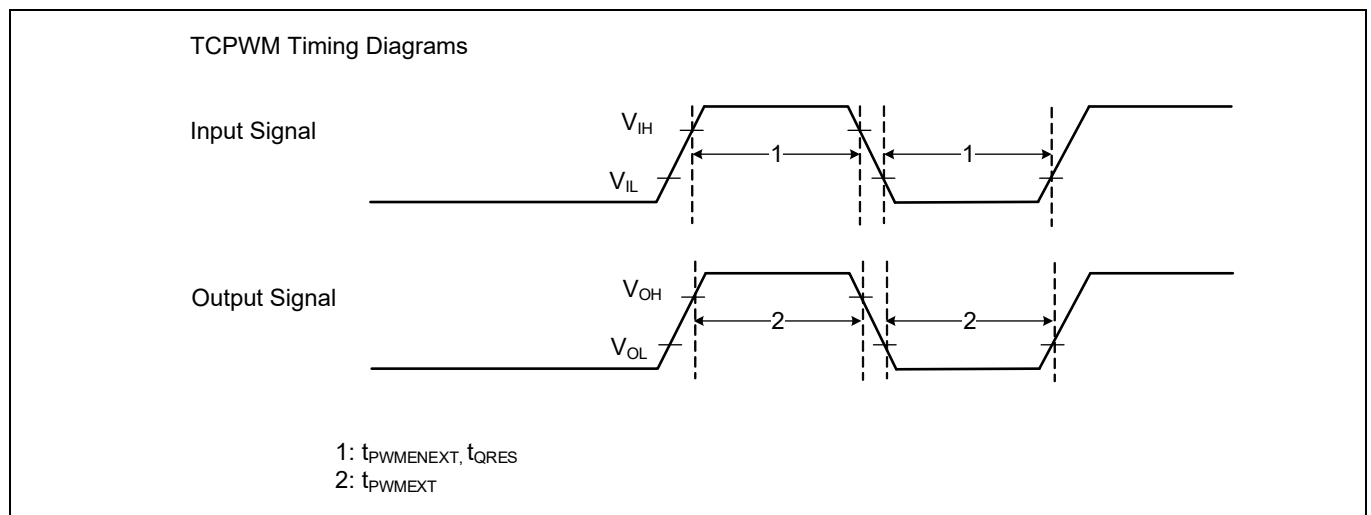
**Figure 26-7 AC timings specifications**

## 26.8 Digital peripherals

All specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$  and for 2.7 V to 5.5 V except where noted.

**Table 26-10 Timer/counter/PWM (TCPWM) specifications**

| Spec ID | Parameter              | Description                                      | Min       | Typ | Max | Units | Details/conditions                                                                                                   |
|---------|------------------------|--------------------------------------------------|-----------|-----|-----|-------|----------------------------------------------------------------------------------------------------------------------|
| SID120  | $f_C$                  | TCPWM operating frequency                        | –         | –   | 100 | MHz   | $f_C$ = peripheral clock                                                                                             |
| SID121  | $t_{\text{PWMENTEXT}}$ | Input trigger pulse width for all trigger events | $2 / f_C$ | –   | –   | ns    | Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. |
| SID122  | $t_{\text{PWMENTEXT}}$ | Output trigger pulse widths                      | $2 / f_C$ | –   | –   | ns    | Minimum possible width of Overflow, Underflow, and Counter = Compare (CC) value trigger outputs                      |
| SID123  | $t_{\text{CRES}}$      | Resolution of counter                            | $1 / f_C$ | –   | –   | ns    | Minimum time between successive counts                                                                               |
| SID124  | $t_{\text{PWMRES}}$    | PWM resolution                                   | $1 / f_C$ | –   | –   | ns    | Minimum pulse width of PWM output                                                                                    |
| SID125  | $t_{\text{QRES}}$      | Quadrature inputs resolution                     | $2 / f_C$ | –   | –   | ns    | Minimum pulse width between Quadrature phase inputs.                                                                 |



**Figure 26-8 TCPWM timing diagrams**

**Table 26-11 Serial communication block (SCB) specifications**

| Spec ID                                       | Parameter              | Description                                     | Min                               | Typ | Max  | Units | Details/conditions                                                                                                                                                        |
|-----------------------------------------------|------------------------|-------------------------------------------------|-----------------------------------|-----|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID129                                        | $f_{\text{SCB}}$       | SCB operating frequency                         | –                                 | –   | 100  | MHz   |                                                                                                                                                                           |
| <b>I<sup>2</sup>C interface-standard-mode</b> |                        |                                                 |                                   |     |      |       |                                                                                                                                                                           |
| SID130                                        | $f_{\text{SCL}}$       | SCL clock frequency                             | –                                 | –   | 100  | kHz   |                                                                                                                                                                           |
| SID131                                        | $t_{\text{HD;STA}}$    | Hold time, START condition                      | 4000                              | –   | –    | ns    |                                                                                                                                                                           |
| SID132                                        | $t_{\text{LOW}}$       | Low period of SCL                               | 4700                              | –   | –    | ns    |                                                                                                                                                                           |
| SID133                                        | $t_{\text{HIGH}}$      | High period of SCL                              | 4000                              | –   | –    | ns    |                                                                                                                                                                           |
| SID134                                        | $t_{\text{SU;STA}}$    | Setup time for a repeated START                 | 4700                              | –   | –    | ns    |                                                                                                                                                                           |
| SID135                                        | $t_{\text{HD;DAT}}$    | Data hold time, for receiver                    | 0                                 | –   | –    | ns    |                                                                                                                                                                           |
| SID136                                        | $t_{\text{SU;DAT}}$    | Data setup time                                 | 250                               | –   | –    | ns    |                                                                                                                                                                           |
| SID138                                        | $t_{\text{F}}$         | Fall time of SCL and SDA                        | –                                 | –   | 300  | ns    | Input and output                                                                                                                                                          |
| SID139                                        | $t_{\text{SU;STO}}$    | Setup time for STOP                             | 4000                              | –   | –    | ns    |                                                                                                                                                                           |
| SID140                                        | $t_{\text{BUF}}$       | Bus-free time between START and STOP            | 4700                              | –   | –    | ns    |                                                                                                                                                                           |
| SID141                                        | $C_{\text{B}}$         | Capacitive load for each bus line               | –                                 | –   | 400  | pF    |                                                                                                                                                                           |
| SID142                                        | $t_{\text{VD;DAT}}$    | Time for data signal from SCL LOW to SDA output | –                                 | –   | 3450 | ns    |                                                                                                                                                                           |
| SID143                                        | $t_{\text{VD;ACK}}$    | Data valid acknowledge time                     | –                                 | –   | 3450 | ns    |                                                                                                                                                                           |
| SID144                                        | $V_{\text{OL}}$        | LOW level output voltage                        | 0                                 | –   | 0.4  | V     | Open drain at 3-mA sink current                                                                                                                                           |
| SID145                                        | $I_{\text{OL}}$        | LOW level output current                        | 3                                 | –   | –    | mA    | $V_{\text{OL}} = 0.4 \text{ V}$                                                                                                                                           |
| <b>I<sup>2</sup>C interface-fast-mode</b>     |                        |                                                 |                                   |     |      |       |                                                                                                                                                                           |
| SID150                                        | $f_{\text{SCL\_F}}$    | SCL clock frequency                             | –                                 | –   | 400  | kHz   |                                                                                                                                                                           |
| SID151                                        | $t_{\text{HD;STA\_F}}$ | Hold time, START condition                      | 600                               | –   | –    | ns    |                                                                                                                                                                           |
| SID152                                        | $t_{\text{LOW\_F}}$    | Low period of SCL                               | 1300                              | –   | –    | ns    |                                                                                                                                                                           |
| SID153                                        | $t_{\text{HIGH\_F}}$   | High period of SCL                              | 600                               | –   | –    | ns    |                                                                                                                                                                           |
| SID154                                        | $t_{\text{SU;STA\_F}}$ | Setup time for a repeated START                 | 600                               | –   | –    | ns    |                                                                                                                                                                           |
| SID155                                        | $t_{\text{HD;DAT\_F}}$ | Data hold time, for receiver                    | 0                                 | –   | –    | ns    |                                                                                                                                                                           |
| SID156                                        | $t_{\text{SU;DAT\_F}}$ | Data setup time                                 | 100                               | –   | –    | ns    |                                                                                                                                                                           |
| SID158                                        | $t_{\text{F\_F}}$      | Fall time of SCL and SDA                        | $20 \times (V_{\text{DD}} / 5.5)$ | –   | 300  | ns    | Input and output, GPIO_ENH: slow mode, 400 pF load                                                                                                                        |
| SID158A                                       | $t_{\text{FA\_F}}$     | Fall time of SCL and SDA                        | 0.35                              | –   | 300  | ns    | Input and output<br>GPIO_STD:<br>drive_sel<1:0>= 0b00<br>MIN: 10 pF load,<br>$R_{\text{PU}} = 35.41 \text{ k}\Omega$<br>Max: 400 pF load,<br>$R_{\text{PU}} = 350 \Omega$ |
| SID159                                        | $t_{\text{SU;STO\_F}}$ | Setup time for STOP                             | 600                               | –   | –    | ns    | Input and output                                                                                                                                                          |
| SID160                                        | $t_{\text{BUF\_F}}$    | Bus free time between START and STOP            | 1300                              | –   | –    | ns    |                                                                                                                                                                           |
| SID161                                        | $C_{\text{B\_F}}$      | Capacitive load for each bus line               | –                                 | –   | 400  | pF    |                                                                                                                                                                           |

**Table 26-11 Serial communication block (SCB) specifications** *(continued)*

| Spec ID | Parameter       | Description                                                       | Min | Typ | Max | Units | Details/conditions              |
|---------|-----------------|-------------------------------------------------------------------|-----|-----|-----|-------|---------------------------------|
| SID162  | $t_{VD;DAT\_F}$ | Time for data signal from SCL LOW to SDA output                   | –   | –   | 900 | ns    |                                 |
| SID163  | $t_{VD;ACK\_F}$ | Data valid acknowledge time                                       | –   | –   | 900 | ns    |                                 |
| SID164  | $t_{SP\_F}$     | Pulse width of spikes that must be suppressed by the input filter | –   | –   | 50  | ns    |                                 |
| SID165  | $V_{OL\_F}$     | LOW level output voltage                                          | 0   | –   | 0.4 | V     | Open-drain at 3 mA sink current |
| SID165  | $I_{OL\_F}$     | LOW level output current                                          | 3   | –   | –   | mA    | $V_{OL} = 0.4\text{ V}$         |
| SID167  | $I_{OL2\_F}$    | LOW level output current                                          | 6   | –   | –   | mA    | $V_{OL} = 0.6\text{ V}^{[64]}$  |

**I<sup>2</sup>C interface-fast-plus mode**

|        |                  |                                                                   |                          |   |     |     |                                                    |
|--------|------------------|-------------------------------------------------------------------|--------------------------|---|-----|-----|----------------------------------------------------|
| SID170 | $f_{SCL\_FP}$    | SCL clock frequency                                               | –                        | – | 1   | MHz |                                                    |
| SID171 | $t_{HD;STA\_FP}$ | Hold time, START condition                                        | 260                      | – | –   | ns  |                                                    |
| SID172 | $t_{LOW\_FP}$    | Low period of SCL                                                 | 500                      | – | –   | ns  |                                                    |
| SID173 | $t_{HIGH\_FP}$   | High period of SCL                                                | 260                      | – | –   | ns  |                                                    |
| SID174 | $t_{SU;STA\_FP}$ | Setup time for a repeated START                                   | 260                      | – | –   | ns  |                                                    |
| SID175 | $t_{HD;DAT\_FP}$ | Data hold time, for receiver                                      | 0                        | – | –   | ns  |                                                    |
| SID176 | $t_{SU;DAT\_FP}$ | Data setup time                                                   | 50                       | – | –   | ns  |                                                    |
| SID178 | $t_{F\_FP}$      | Fall time of SCL and SDA                                          | $20 \times (V_{DD}/5.5)$ | – | 160 | ns  | Input and output 20-pF load<br>GPIO_ENH: slow mode |
| SID179 | $t_{SU;STO\_FP}$ | Setup time for STOP                                               | 260                      | – | –   | ns  | Input and output                                   |
| SID180 | $t_{BUF\_FP}$    | Bus free time between START and STOP                              | 500                      | – | –   | ns  |                                                    |
| SID181 | $C_{B\_FP}$      | Capacitive load for each bus line                                 | –                        | – | 20  | pF  |                                                    |
| SID182 | $t_{VD;DAT\_FP}$ | Time for data signal from SCL LOW to SDA output                   | –                        | – | 450 | ns  |                                                    |
| SID183 | $t_{VD;ACK\_FP}$ | Data valid acknowledge time                                       | –                        | – | 450 | ns  |                                                    |
| SID184 | $t_{SP\_FP}$     | Pulse width of spikes that must be suppressed by the input filter | –                        | – | 50  | ns  |                                                    |
| SID186 | $V_{OL\_FP}$     | LOW level output voltage                                          | 0                        | – | 0.4 | V   | Open-drain at 3 mA sink current                    |
| SID187 | $I_{OL\_FP}$     | LOW level output current                                          | $3^{[65]}$               | – | –   | mA  | $V_{OL} = 0.4\text{ V}^{[65]}$                     |

**SPI interface master (Full-clock mode: LATE\_MISO\_SAMPLE = 1) [Conditions: drive\_sel<1:0>= 0x]**

|        |           |                                                |   |   |      |     |                                                     |
|--------|-----------|------------------------------------------------|---|---|------|-----|-----------------------------------------------------|
| SID190 | $f_{SPI}$ | SPI operating frequency                        | – | – | 12.5 | MHz | Do not use half-clock mode:<br>LATE_MISO_SAMPLE = 0 |
| SID191 | $t_{DMO}$ | SPI Master: MOSI valid after SCLK driving edge | – | – | 15   | ns  |                                                     |

**Notes**

64. In order to drive full bus load at 400 kHz, 6 mA  $I_{OL}$  is required at 0.6 V  $V_{OL}$ .

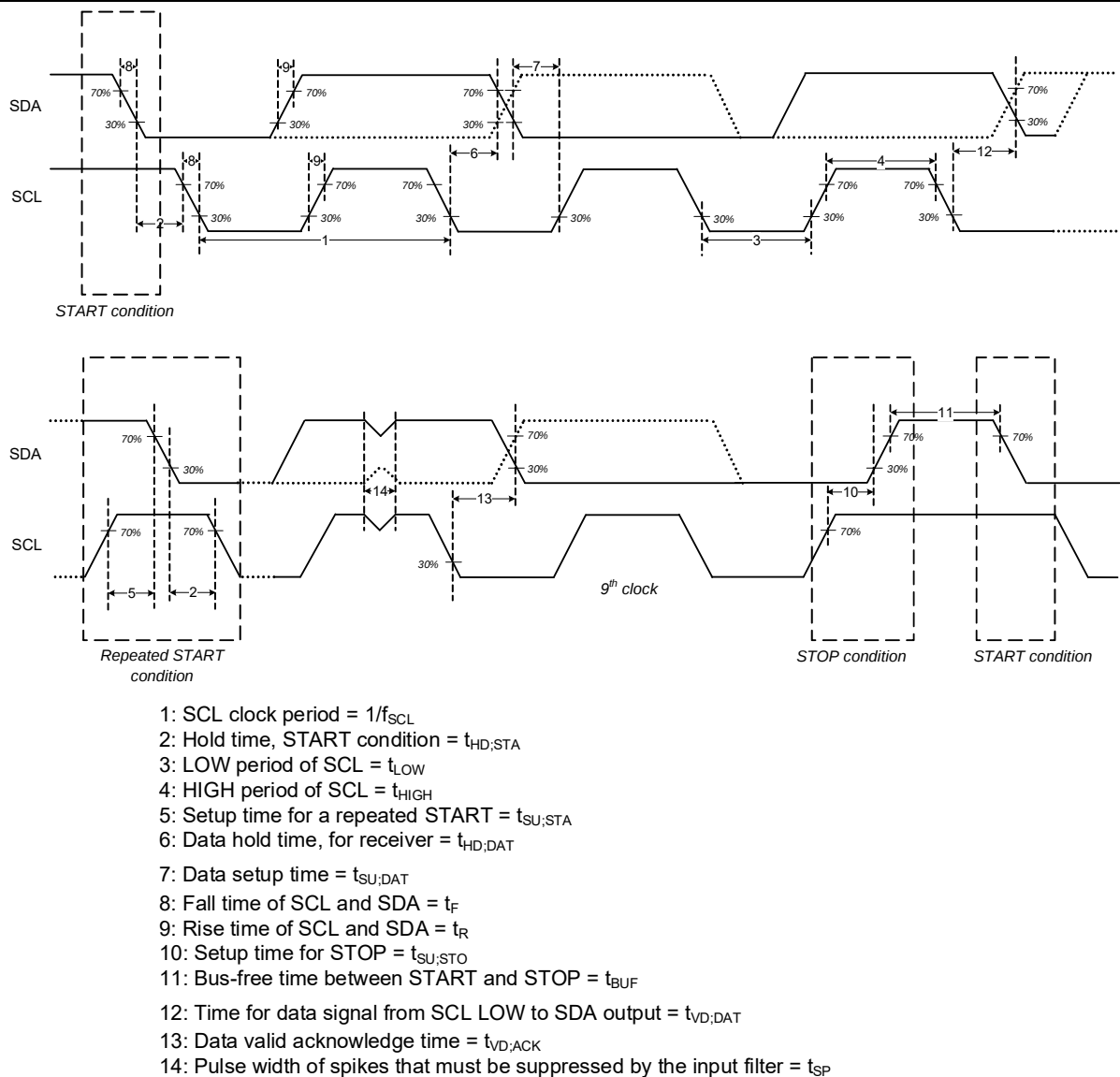
65. In order to drive full bus load at 1 MHz, 20 mA  $I_{OL}$  is required at 0.4 V  $V_{OL}$ . However, this device does not support it.

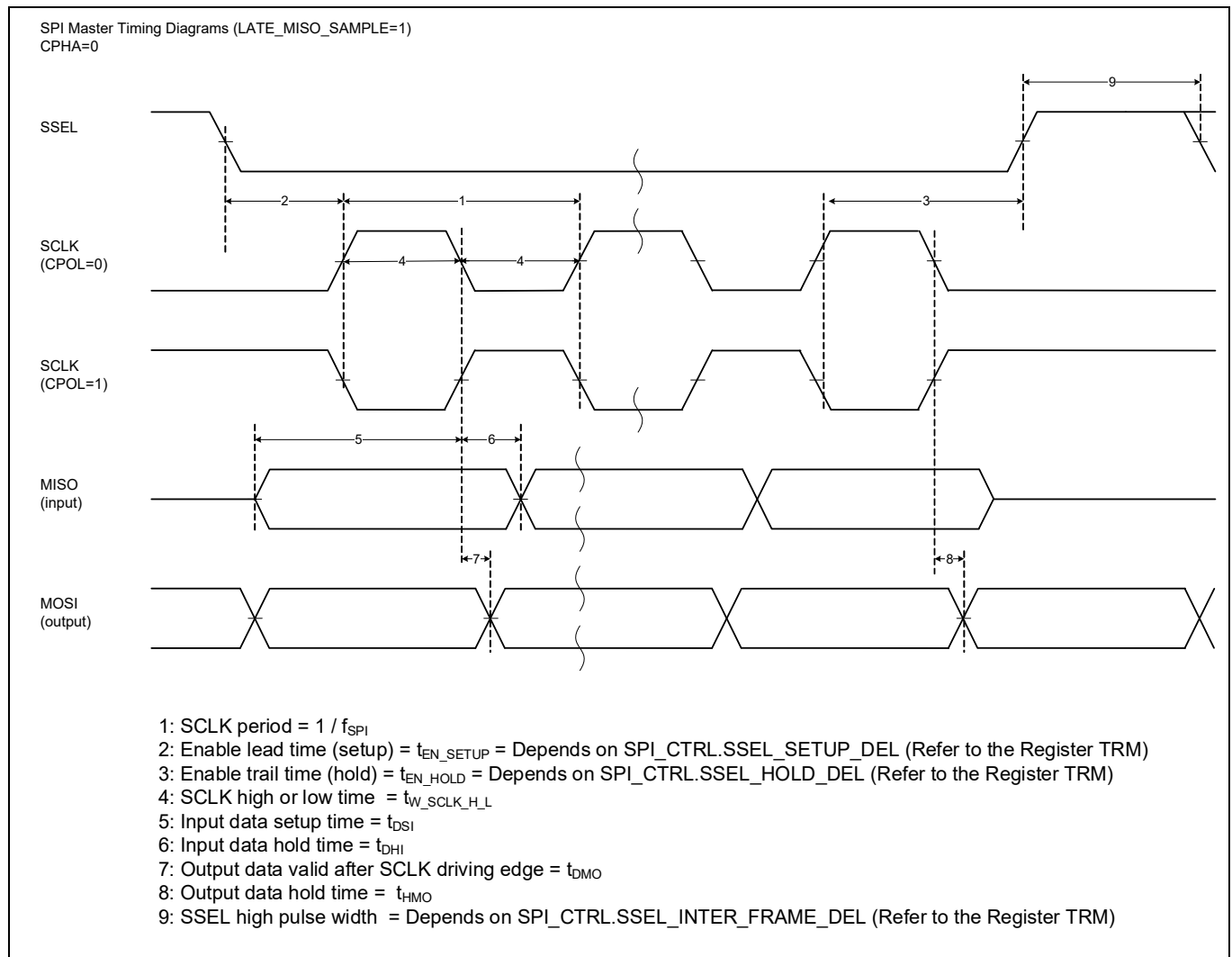
**Table 26-11 Serial communication block (SCB) specifications** *(continued)*

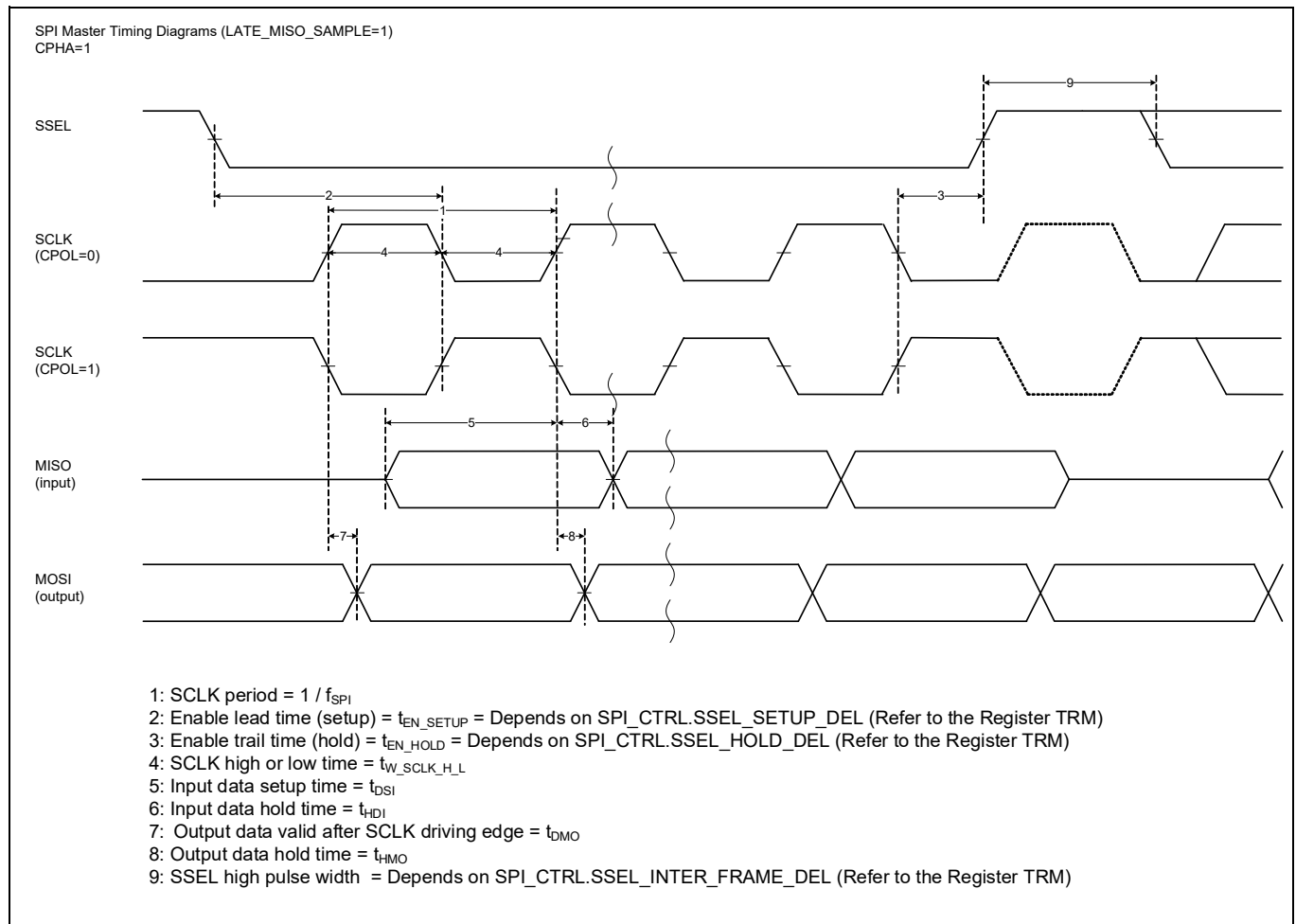
| Spec ID                                                                                | Parameter            | Description                                                                    | Min                      | Typ                        | Max  | Units | Details/conditions       |
|----------------------------------------------------------------------------------------|----------------------|--------------------------------------------------------------------------------|--------------------------|----------------------------|------|-------|--------------------------|
| SID192                                                                                 | $t_{DSI}$            | SPI Master: MISO valid before SCLK capturing edge                              | 40                       | –                          | –    | ns    |                          |
| SID193                                                                                 | $t_{HMO}$            | SPI Master: Previous MOSI data hold time                                       | 0                        | –                          | –    | ns    |                          |
| SID194                                                                                 | $t_{W\_SCLK\_H\_L}$  | SPI SCLK pulse width HIGH or LOW                                               | –                        | $0.4 \times (1 / f_{SPI})$ | –    | ns    |                          |
| SID196                                                                                 | $t_{DHI}$            | SPI Master: MISO hold time after SCLK capturing edge                           | 0                        | –                          | –    | ns    |                          |
| SID198                                                                                 | $t_{EN\_SETUP}$      | SSEL valid, before the first SCK capturing edge                                | $0.5 \times (1/f_{SPI})$ | –                          | –    | ns    | Min is half clock period |
| SID199                                                                                 | $t_{EN\_SHOLD}$      | SSEL hold, after the last SCK capturing edge                                   | $0.5 \times (1/f_{SPI})$ | –                          | –    | ns    | Min is half clock period |
| SID195                                                                                 | $C_{SPIM\_MS}$       | SPI capacitive load                                                            | –                        | –                          | 10   | pF    |                          |
| <b>SPI interface slave (internally clocked) [Conditions: drive_sel&lt;1:0&gt;= 0x]</b> |                      |                                                                                |                          |                            |      |       |                          |
| SID205                                                                                 | $f_{SPI\_INT}$       | SPI operating frequency                                                        | –                        | –                          | 10   | MHz   |                          |
| SID206                                                                                 | $t_{DMI\_INT}$       | SPI Slave: MOSI Valid before Scklock capturing edge                            | 5                        | –                          | –    | ns    |                          |
| SID207                                                                                 | $t_{DSO\_INT}$       | SPI Slave: MISO Valid after Scklock driving edge, in the internal-clocked mode | –                        | –                          | 62   | ns    |                          |
| SID208                                                                                 | $t_{HSP}$            | SPI Slave: Previous MISO data hold time                                        | 3                        | –                          | –    | ns    |                          |
| SID209                                                                                 | $t_{EN\_SETUP\_INT}$ | SPI Slave: SSEL valid to first SCK valid edge                                  | 33                       | –                          | –    | ns    |                          |
| SID210                                                                                 | $t_{EN\_HOLD\_INT}$  | SPI Slave Select active (LOW) from last SCLK hold                              | 33                       | –                          | –    | ns    |                          |
| SID211                                                                                 | $t_{EN\_SETUP\_PRE}$ | SPI Slave: from SSEL valid, to SCK falling edge before the first data bit      | 20                       | –                          | –    | ns    |                          |
| SID212                                                                                 | $t_{EN\_HOLD\_PRE}$  | SPI Slave: from SCK falling edge before the first data bit, to SSEL invalid    | 20                       | –                          | –    | ns    |                          |
| SID213                                                                                 | $t_{EN\_SETUP\_CO}$  | SPI Slave: from SSEL valid, to SCK falling edge in the first data bit          | 20                       | –                          | –    | ns    |                          |
| SID214                                                                                 | $t_{EN\_HOLD\_CO}$   | SPI Slave: from SCK falling edge in the first data bit, to SSEL invalid        | 20                       | –                          | –    | ns    |                          |
| SID215                                                                                 | $t_{W\_DIS\_INT}$    | SPI Slave Select inactive time                                                 | 40                       | –                          | –    | ns    |                          |
| SID216                                                                                 | $t_{W\_SCLKH\_INT}$  | SPI SCLK pulse width HIGH                                                      | 20                       | –                          | –    | ns    |                          |
| SID217                                                                                 | $t_{W\_SCLKL\_INT}$  | SPI SCLK pulse width LOW                                                       | 20                       | –                          | –    | ns    |                          |
| SID218                                                                                 | $t_{SIH\_INT}$       | SPI MOSI hold from SCLK                                                        | 12                       | –                          | –    | ns    |                          |
| SID219                                                                                 | $C_{SPIS\_INT}$      | SPI Capacitive Load                                                            | –                        | –                          | 10   | pF    |                          |
| <b>SPI interface slave (externally clocked) [Conditions: drive_sel&lt;1:0&gt;= 0x]</b> |                      |                                                                                |                          |                            |      |       |                          |
| SID220                                                                                 | $f_{SPI\_EXT}$       | SPI operating frequency                                                        | –                        | –                          | 12.5 | MHz   |                          |

**Table 26-11 Serial communication block (SCB) specifications** *(continued)*

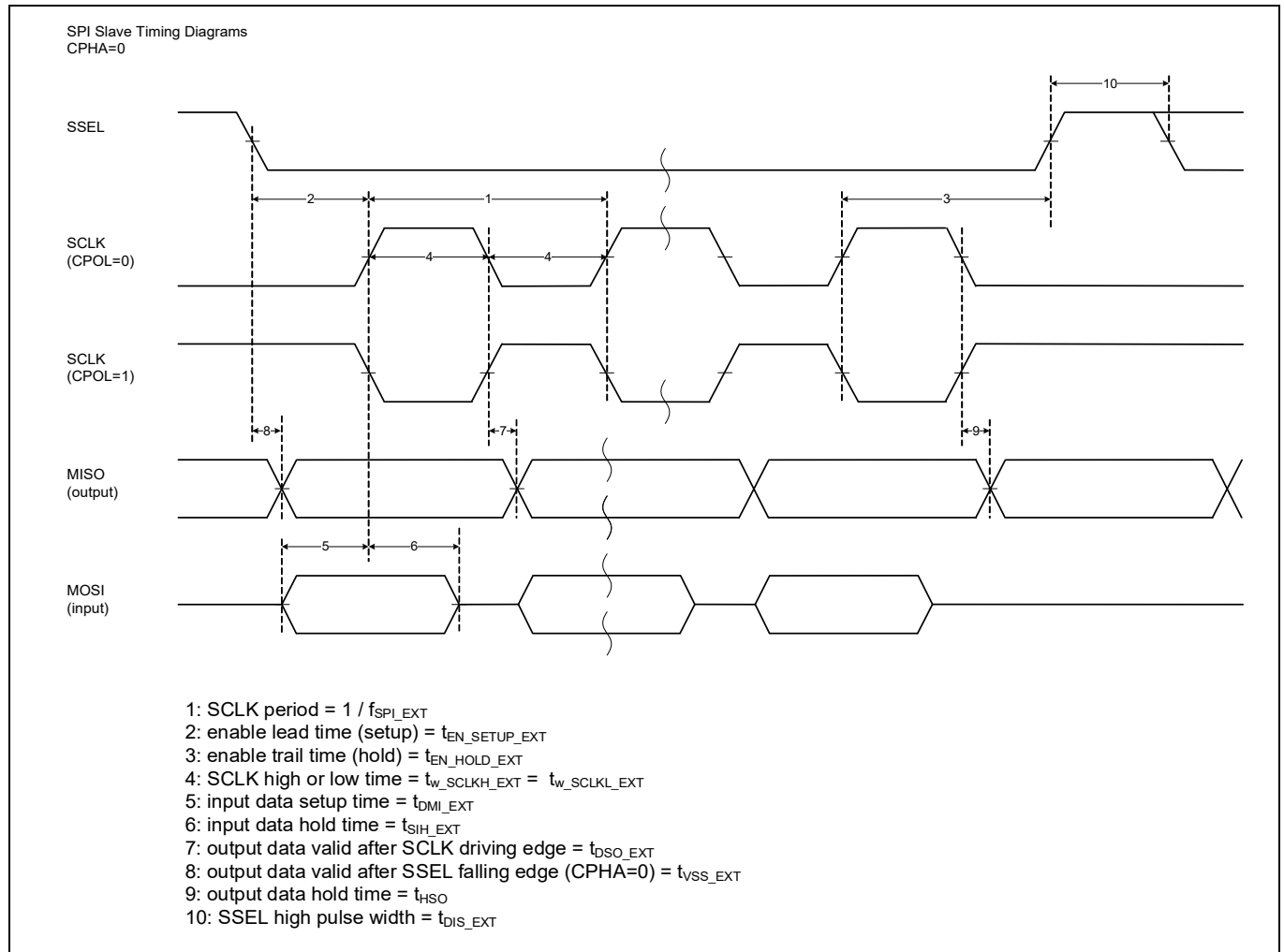
| Spec ID               | Parameter             | Description                                                                    | Min | Typ | Max | Units | Details/conditions |
|-----------------------|-----------------------|--------------------------------------------------------------------------------|-----|-----|-----|-------|--------------------|
| SID221                | $t_{DMI\_EXT}$        | SPI Slave: MOSI Valid before Scklock capturing edge                            | 5   | –   | –   | ns    |                    |
| SID222                | $t_{DSO\_EXT}$        | SPI Slave: MISO Valid after Scklock driving edge, in the external-clocked mode | –   | –   | 32  | ns    |                    |
| SID223                | $t_{HSO\_EXT}$        | SPI Slave: Previous MISO data hold time                                        | 3   | –   | –   | ns    |                    |
| SID224                | $t_{EN\_SET-UP\_EXT}$ | SPI Slave: SSEL valid to first SCK valid edge                                  | 40  | –   | –   | ns    |                    |
| SID225                | $t_{EN\_HOLD\_EXT}$   | SPI Slave Select active (LOW) from last SCLK hold                              | 40  | –   | –   | ns    |                    |
| SID226                | $t_{W\_DIS\_EXT}$     | SPI Slave Select inactive time                                                 | 80  | –   | –   | ns    |                    |
| SID227                | $t_{W\_SCLKH\_EXT}$   | SPI SCLK pulse width HIGH                                                      | 34  | –   | –   | ns    |                    |
| SID228                | $t_{W\_SCLKL\_EXT}$   | SPI SCLK pulse width LOW                                                       | 34  | –   | –   | ns    |                    |
| SID229                | $t_{SIH\_EXT}$        | SPI MOSI hold from SCLK                                                        | 20  | –   | –   | ns    |                    |
| SID230                | $C_{SPIS\_EXT}$       | SPI Capacitive Load                                                            | –   | –   | 10  | pF    |                    |
| SID231                | $t_{VSS\_EXT}$        | SPI Slave: MISO valid after SSEL falling edge (CPHA = 0)                       | –   | –   | 33  | ns    |                    |
| <b>UART interface</b> |                       |                                                                                |     |     |     |       |                    |
| SID240                | $f_{BPS}$             | Data rate                                                                      | –   | –   | 10  | Mbps  |                    |


**Figure 26-9 I<sup>2</sup>C timing diagrams**

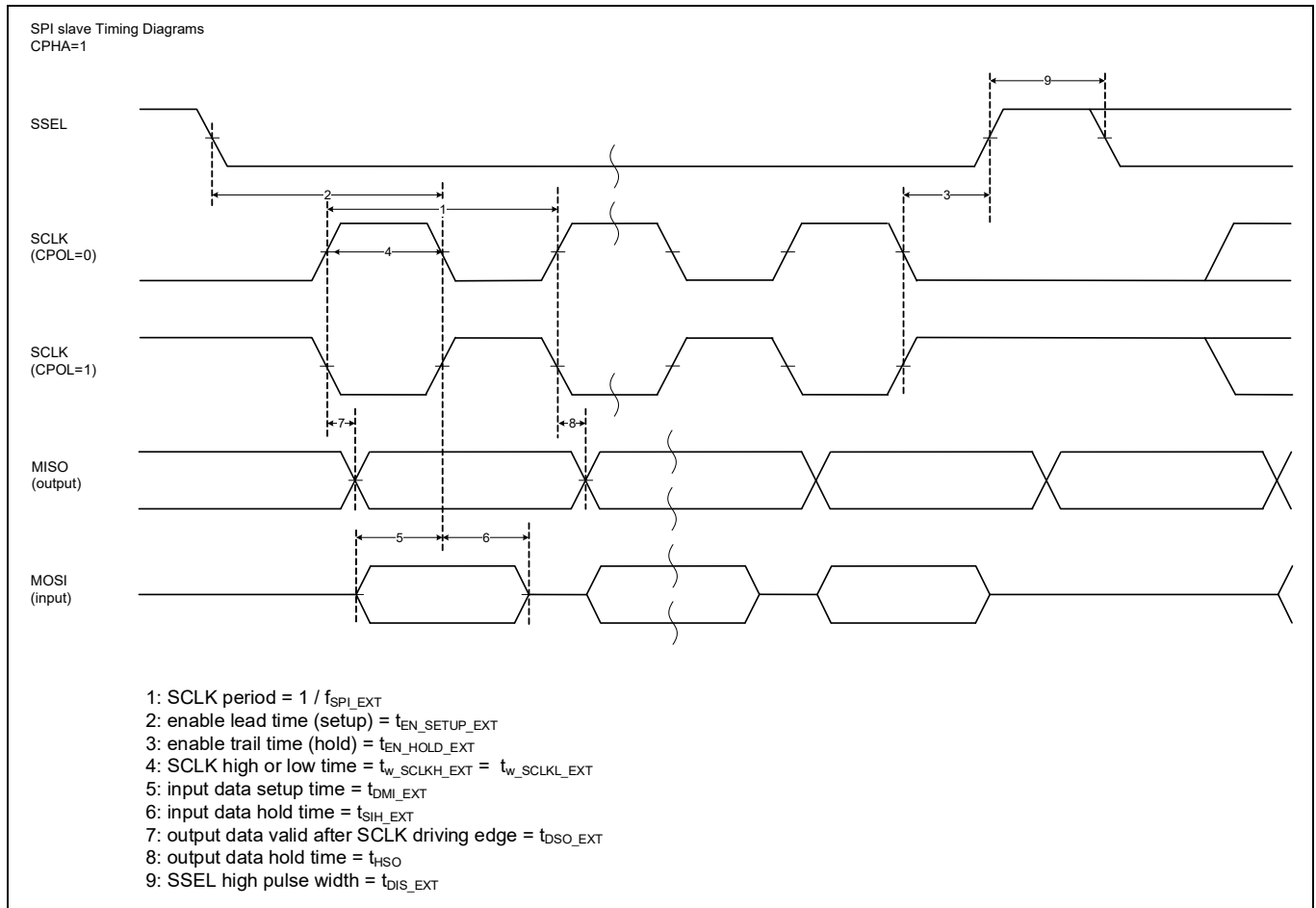

**Figure 26-10 SPI master timing diagrams with LOW clock phase**



**Figure 26-11 SPI master timing diagrams with HIGH clock phase**



**Figure 26-12 SPI slave timing diagrams with LOW clock phase**


**Figure 26-13 SPI slave timing diagrams with HIGH clock phase**
**Table 26-12 CAN FD specifications**

| Spec ID | Parameter         | Description            | Min | Typ | Max | Units | Details/conditions                                            |
|---------|-------------------|------------------------|-----|-----|-----|-------|---------------------------------------------------------------|
| SID630  | $f_{\text{HCLK}}$ | System clock frequency | –   | –   | 100 | MHz   | $f_{\text{CCLK}} \leq f_{\text{HCLK}}$ , guaranteed by design |
| SID631  | $f_{\text{CCLK}}$ | CAN clock frequency    | –   | –   | 100 | MHz   | $f_{\text{CCLK}} \leq f_{\text{HCLK}}$ , guaranteed by design |

**Table 26-13 LIN specifications**

| Spec ID | Parameter        | Description                                                                                   | Min | Typ | Max   | Units | Details/conditions   |
|---------|------------------|-----------------------------------------------------------------------------------------------|-----|-----|-------|-------|----------------------|
| SID249  | $f_{\text{LIN}}$ | Internal clock frequency to the LIN block                                                     | –   | –   | 100   | MHz   |                      |
| SID250  | BR_NOM           | Bit rate on the LIN bus                                                                       | 1   | –   | 20    | kbps  | Guaranteed by design |
| SID250A | BR_REF           | Bit rate on the LIN bus (not in standard LIN specification) for re-flashing in LIN slave mode | 1   | –   | 115.2 | kbps  | Guaranteed by design |

## 26.9 Memory

All specifications are valid for  $-40\text{ °C} \leq T_A \leq 125\text{ °C}$  and for 2.7 V to 5.5 V except where noted.

**Table 26-14 Flash DC specifications**

| Spec ID | Parameter       | Description               | Min | Typ | Max | Units | Details/conditions |
|---------|-----------------|---------------------------|-----|-----|-----|-------|--------------------|
| SID260  | V <sub>PE</sub> | Erase and program voltage | 2.7 | –   | 5.5 | V     |                    |

**Table 26-15 Flash AC specifications**

| Spec ID | Parameter                 | Description                                                          | Min | Typ | Max          | Units | Details/conditions                                                                                   |
|---------|---------------------------|----------------------------------------------------------------------|-----|-----|--------------|-------|------------------------------------------------------------------------------------------------------|
| SID257  | f <sub>FO</sub>           | Maximum flash memory operation frequency                             | –   | –   | 100          | MHz   | Zero wait access to code-flash memory up to 100 MHz<br>Zero wait access with cache hit up to 250 MHz |
| SID254  | t <sub>ERS_SUS</sub>      | Maximum time from erase suspend command till erase is indeed suspend | –   | –   | 37.5         | µs    |                                                                                                      |
| SID255  | t <sub>ERS_RES_SUS</sub>  | Minimum time allowed from erase resume to erase suspend              | 250 | –   | –            | µs    | Guaranteed by design                                                                                 |
| SID258  | t <sub>BC_WF</sub>        | Blank check time for N-bytes of work-flash                           | –   | –   | 10 + 0.3 × N | µs    | At 100 MHz, N ≥ 4 and multiple of 4, excludes system overhead time                                   |
| SID259  | t <sub>SECTORERASE1</sub> | Sector erase time (code-flash: 32 KB)                                | –   | 45  | 90           | ms    | Includes internal preprogramming time                                                                |
| SID259A | t <sub>SECTORERASE2</sub> | Sector erase time (code-flash: 8 KB)                                 | –   | 15  | 30           | ms    | Includes internal preprogramming time                                                                |
| SID261  | t <sub>SECTORERASE3</sub> | Sector erase time (work-flash, 2 KB)                                 | –   | 80  | 160          | ms    | Includes internal preprogramming time                                                                |
| SID262  | t <sub>SECTORERASE4</sub> | Sector erase time (work-flash, 128 B)                                | –   | 5   | 15           | ms    | Includes internal preprogramming time                                                                |
| SID263  | t <sub>WRITE1</sub>       | 64-bit write time (code-flash)                                       | –   | 30  | 60           | µs    | Excludes system overhead time                                                                        |
| SID264  | t <sub>WRITE2</sub>       | 256-bit write time (code-flash)                                      | –   | 40  | 70           | µs    | Excludes system overhead time                                                                        |
| SID265  | t <sub>WRITE3</sub>       | 4096-bit write time (code-flash) <sup>[66]</sup>                     | –   | 320 | 1200         | µs    | Excludes system overhead time                                                                        |
| SID266  | t <sub>WRITE4</sub>       | 32-bit write time (work-flash)                                       | –   | 30  | 60           | µs    | Excludes system overhead time                                                                        |
| SID267  | t <sub>FRET1</sub>        | Code-flash retention. 1000 program/erase cycles                      | 20  | –   | –            | years | T <sub>A</sub> (power on and off) ≤ 85 °C average                                                    |
| SID268  | t <sub>FRET3</sub>        | Work-flash retention. 125,000 program/erase cycles                   | 20  | –   | –            | years | T <sub>A</sub> (power on and off) ≤ 85 °C average                                                    |
| SID269  | t <sub>FRET4</sub>        | Work-flash retention. 250,000 program/erase cycles                   | 10  | –   | –            | years | T <sub>A</sub> (power on and off) ≤ 85 °C average                                                    |

**Note**

66. The code-flash includes a 'Write Buffer' of 4096-bit. If the application software writes this buffer multiple times, to get the overall write time multiply one sector write time with the corresponding factor (say for factor 64, example, 64 × 512 B = 32 KB [one sector]).

**Table 26-15 Flash AC specifications** (continued)

| Spec ID | Parameter       | Description                                              | Min | Typ | Max | Units | Details/conditions                                                                                                                                                                                                                           |
|---------|-----------------|----------------------------------------------------------|-----|-----|-----|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID612  | $I_{CC\_ACT2}$  | Program operating $V_{CCD}$ current (code or work-flash) | –   | 7   | 58  | mA    | Typ: $T_A = 25^\circ\text{C}$ , $V_{DDD} = 5.0\text{ V}$ , $V_{CCD} = 1.15\text{ V}$ , process typ (TT)<br>Max: $T_A = 125^\circ\text{C}$ , $V_{DDD} = 5.5\text{ V}$ , $V_{CCD} = 1.2\text{ V}$ , process worst (FF)<br>Guaranteed by design |
| SID613  | $I_{CC\_ACT3}$  | Erase operating $V_{CCD}$ current (code- or work-flash)  | –   | 7   | 52  | mA    | Typ: $T_A = 25^\circ\text{C}$ , $V_{DDD} = 5.0\text{ V}$ , $V_{CCD} = 1.15\text{ V}$ , process typ (TT)<br>Max: $T_A = 125^\circ\text{C}$ , $V_{DDD} = 5.5\text{ V}$ , $V_{CCD} = 1.2\text{ V}$ , process worst (FF)<br>Guaranteed by design |
| SID612A | $I_{CC\_ACT2A}$ | Program operating $V_{DDD}$ current (code or work-flash) | –   | 8   | 10  | mA    | Typ: $T_A = 25^\circ\text{C}$ , $V_{DDD} = 5.0\text{ V}$ , $V_{CCD} = 1.15\text{ V}$ , process typ (TT)<br>Max: $T_A = 125^\circ\text{C}$ , $V_{DDD} = 5.5\text{ V}$ , $V_{CCD} = 1.2\text{ V}$ , process worst (FF)<br>Guaranteed by design |
| SID613A | $I_{CC\_ACT3A}$ | Erase operating $V_{DDD}$ current (code- or work-flash)  | –   | 8   | 16  | mA    | Typ: $T_A = 25^\circ\text{C}$ , $V_{DDD} = 5.0\text{ V}$ , $V_{CCD} = 1.15\text{ V}$ , process typ (TT)<br>Max: $T_A = 125^\circ\text{C}$ , $V_{DDD} = 5.5\text{ V}$ , $V_{CCD} = 1.2\text{ V}$ , process worst (FF)<br>Guaranteed by design |

## 26.10 System resources

All specifications are valid for  $-40\text{ °C} \leq T_A \leq 125\text{ °C}$  and for 2.7 V to 5.5 V except where noted.

**Table 26-16 System resources**

| Spec ID                                         | Parameter                  | Description                                                                                                                                                                           | Min   | Typ   | Max   | Units | Details/conditions                                                            |
|-------------------------------------------------|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-------|-------|-------------------------------------------------------------------------------|
| <b>Power-on reset specifications</b>            |                            |                                                                                                                                                                                       |       |       |       |       |                                                                               |
| SID270                                          | V <sub>POR_D</sub>         | V <sub>DDD</sub> rising voltage to de assert POR                                                                                                                                      | 1.5   | –     | 2.35  | V     | Guaranteed by design                                                          |
| SID276                                          | V <sub>POR_A</sub>         | V <sub>DDD</sub> falling voltage to assert POR                                                                                                                                        | 1.45  | –     | 2.1   | V     |                                                                               |
| SID271                                          | V <sub>POR_H</sub>         | Level detection hysteresis                                                                                                                                                            | 20    | –     | 300   | mV    |                                                                               |
| SID272                                          | t <sub>DLY_POR</sub>       | Delay between V <sub>DDD</sub> rising through 2.3 V and internal deassertion of POR                                                                                                   | –     | –     | 3     | μs    | Guaranteed by design                                                          |
| SID273                                          | t <sub>POFF</sub>          | V <sub>DDD</sub> Power off time                                                                                                                                                       | 100   | –     | –     | μs    | V <sub>DDD</sub> < 1.45 V                                                     |
| SID274                                          | POR_RR1                    | V <sub>DDD</sub> power ramp rate with robust BOD (BOD operation is guaranteed)                                                                                                        | –     | –     | 100   | mV/μs | This ramp supports robust BOD                                                 |
| SID275                                          | POR_RR2                    | V <sub>DDD</sub> power ramp rate without robust BOD                                                                                                                                   | –     | –     | 1000  | mV/μs | This ramp does not support robust BOD<br>t <sub>POFF</sub> must be satisfied. |
| <b>High-voltage BOD (HV BOD) specifications</b> |                            |                                                                                                                                                                                       |       |       |       |       |                                                                               |
| SID500                                          | V <sub>TR_2P7_R</sub>      | HV BOD 2.7 V rising detection point for V <sub>DDD</sub> and V <sub>DDA</sub> (default)                                                                                               | 2.474 | 2.55  | 2.627 | V     |                                                                               |
| SID501                                          | V <sub>TR_2P7_F</sub>      | HV BOD 2.7 V falling detection point for V <sub>DDD</sub> and V <sub>DDA</sub> (default)                                                                                              | 2.449 | 2.525 | 2.601 | V     |                                                                               |
| SID502                                          | V <sub>TR_3P0_R</sub>      | HV BOD 3.0 V rising detection point for V <sub>DDD</sub> and V <sub>DDA</sub>                                                                                                         | 2.765 | 2.85  | 2.936 | V     |                                                                               |
| SID503                                          | V <sub>TR_3P0_F</sub>      | HV BOD 3.0 V falling detection point for V <sub>DDD</sub> and V <sub>DDA</sub>                                                                                                        | 2.74  | 2.825 | 2.91  | V     |                                                                               |
| SID505                                          | HVBOD_RR_A                 | Power ramp rate: V <sub>DDD</sub> and V <sub>DDA</sub> (Active)                                                                                                                       | –     | –     | 100   | mV/μs |                                                                               |
| SID506                                          | HVBOD_RR_DS                | Power ramp rate: V <sub>DDD</sub> and V <sub>DDA</sub> (DeepSleep)                                                                                                                    | –     | –     | 10    | mV/μs |                                                                               |
| SID507                                          | t <sub>DLY_ACT_HVBOD</sub> | Active mode delay between V <sub>DDD</sub> falling/rising through V <sub>TR_2P7_F/R</sub> or V <sub>TR_3P0_F/R</sub> and an internal HV BOD signal transitioning                      | –     | –     | 0.5   | μs    | Guaranteed by design                                                          |
| SID507A                                         | t <sub>DLY_ACT_HVBOD</sub> | Active mode delay between V <sub>DDA</sub> falling/rising through V <sub>TR_2P7_F/R</sub> or V <sub>TR_3P0_F/R</sub> and internal HV BOD signal transitioning                         | –     | –     | 1     | μs    | Guaranteed by design                                                          |
| SID507B                                         | t <sub>DLY_DS_HVBOD</sub>  | DeepSleep mode delay between V <sub>DDD</sub> /V <sub>DDA</sub> falling/rising through V <sub>TR_2P7_F/R</sub> or V <sub>TR_3P0_F/R</sub> and an internal HV BOD signal transitioning | –     | –     | 4     | μs    | Guaranteed by design                                                          |
| SID508                                          | t <sub>RES_HVBOD</sub>     | Response time of HV BOD, V <sub>DDD</sub> /V <sub>DDA</sub> supply. (For falling-then-rising supply at max ramp rate; threshold is V <sub>TR_2P7_F</sub> or V <sub>TR_3P0_F</sub> )   | 100   | –     | –     | ns    | Guaranteed by design                                                          |
| <b>Low-voltage BOD (LV BOD) specifications</b>  |                            |                                                                                                                                                                                       |       |       |       |       |                                                                               |
| SID510                                          | V <sub>TR_R_LVBOD</sub>    | LV BOD rising detection point for V <sub>CCD</sub>                                                                                                                                    | 0.917 | 0.945 | 0.973 | V     |                                                                               |
| SID511                                          | V <sub>TR_F_LVBOD</sub>    | LV BOD falling detection point for V <sub>CCD</sub>                                                                                                                                   | 0.892 | 0.920 | 0.948 | V     |                                                                               |
| SID515                                          | t <sub>DLY_ACT_LVBOD</sub> | Active delay between V <sub>CCD</sub> falling/rising through V <sub>TR_R/F_LVBOD</sub> and an internal LV BOD signal transitioning                                                    | –     | –     | 1     | μs    | Guaranteed by design                                                          |
| SID515A                                         | t <sub>DLY_DS_LVBOD</sub>  | DeepSleep mode delay between V <sub>CCD</sub> falling/rising through V <sub>TR_R/F_LVBOD</sub> and an internal LV BOD signal transitioning                                            | –     | –     | 12    | μs    | Guaranteed by design                                                          |
| SID516                                          | t <sub>RES_LVBOD</sub>     | Response time of LV BOD (for falling-then-rising supply at max ramp rate; threshold is V <sub>TR_F_LVBOD</sub> )                                                                      | 100   | –     | –     | ns    | Guaranteed by design                                                          |

## Electrical specifications

**Table 26-16 System resources** (continued)

| Spec ID                                             | Parameter             | Description                                            | Min      | Typ  | Max      | Units | Details/conditions                    |
|-----------------------------------------------------|-----------------------|--------------------------------------------------------|----------|------|----------|-------|---------------------------------------|
| <b>Low-voltage detector (LVD) DC specifications</b> |                       |                                                        |          |      |          |       |                                       |
| SID520                                              | V <sub>TR_2P8_F</sub> | LVD 2.8 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 2800 | Typ + 4% | mV    |                                       |
| SID521                                              | V <sub>TR_2P9_F</sub> | LVD 2.9 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 2900 | Typ + 4% | mV    |                                       |
| SID522                                              | V <sub>TR_3P0_F</sub> | LVD 3.0 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 3000 | Typ + 4% | mV    |                                       |
| SID523                                              | V <sub>TR_3P1_F</sub> | LVD 3.1 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 3100 | Typ + 4% | mV    |                                       |
| SID524                                              | V <sub>TR_3P2_F</sub> | LVD 3.2 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 3200 | Typ + 4% | mV    |                                       |
| SID525                                              | V <sub>TR_3P3_F</sub> | LVD 3.3 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 3300 | Typ + 4% | mV    |                                       |
| SID526                                              | V <sub>TR_3P4_F</sub> | LVD 3.4 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 3400 | Typ + 4% | mV    |                                       |
| SID527                                              | V <sub>TR_3P5_F</sub> | LVD 3.5 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 3500 | Typ + 4% | mV    |                                       |
| SID528                                              | V <sub>TR_3P6_F</sub> | LVD 3.6 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 3600 | Typ + 4% | mV    |                                       |
| SID529                                              | V <sub>TR_3P7_F</sub> | LVD 3.7 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 3700 | Typ + 4% | mV    |                                       |
| SID530                                              | V <sub>TR_3P8_F</sub> | LVD 3.8 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 3800 | Typ + 4% | mV    |                                       |
| SID531                                              | V <sub>TR_3P9_F</sub> | LVD 3.9 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 3900 | Typ + 4% | mV    |                                       |
| SID532                                              | V <sub>TR_4P0_F</sub> | LVD 4.0 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 4000 | Typ + 4% | mV    |                                       |
| SID533                                              | V <sub>TR_4P1_F</sub> | LVD 4.1 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 4100 | Typ + 4% | mV    |                                       |
| SID534                                              | V <sub>TR_4P2_F</sub> | LVD 4.2 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 4200 | Typ + 4% | mV    |                                       |
| SID535                                              | V <sub>TR_4P3_F</sub> | LVD 4.3 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 4300 | Typ + 4% | mV    |                                       |
| SID536                                              | V <sub>TR_4P4_F</sub> | LVD 4.4 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 4400 | Typ + 4% | mV    |                                       |
| SID537                                              | V <sub>TR_4P5_F</sub> | LVD 4.5 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 4500 | Typ + 4% | mV    |                                       |
| SID538                                              | V <sub>TR_4P6_F</sub> | LVD 4.6 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 4600 | Typ + 4% | mV    |                                       |
| SID539                                              | V <sub>TR_4P7_F</sub> | LVD 4.7 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 4700 | Typ + 4% | mV    |                                       |
| SID540                                              | V <sub>TR_4P8_F</sub> | LVD 4.8 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 4800 | Typ + 4% | mV    |                                       |
| SID541                                              | V <sub>TR_4P9_F</sub> | LVD 4.9 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 4900 | Typ + 4% | mV    |                                       |
| SID542                                              | V <sub>TR_5P0_F</sub> | LVD 5.0 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 5000 | Typ + 4% | mV    |                                       |
| SID543                                              | V <sub>TR_5P1_F</sub> | LVD 5.1 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 5100 | Typ + 4% | mV    |                                       |
| SID544                                              | V <sub>TR_5P2_F</sub> | LVD 5.2 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 5200 | Typ + 4% | mV    |                                       |
| SID545                                              | V <sub>TR_5P3_F</sub> | LVD 5.3 V falling detection point for V <sub>DDD</sub> | Typ – 4% | 5300 | Typ + 4% | mV    |                                       |
| SID546                                              | V <sub>TR_2P8_R</sub> | LVD 2.8 V rising detection point for V <sub>DDD</sub>  | Typ – 4% | 2825 | Typ + 4% | mV    | Same as V <sub>TR_2P8_F</sub> + 25 mV |
| SID547                                              | V <sub>TR_2P9_R</sub> | LVD 2.9 V rising detection point for V <sub>DDD</sub>  | Typ – 4% | 2925 | Typ + 4% | mV    | Same as V <sub>TR_2P9_F</sub> + 25 mV |
| SID548                                              | V <sub>TR_3P0_R</sub> | LVD 3.0 V rising detection point for V <sub>DDD</sub>  | Typ – 4% | 3025 | Typ + 4% | mV    | Same as V <sub>TR_3P0_F</sub> + 25 mV |

## Electrical specifications

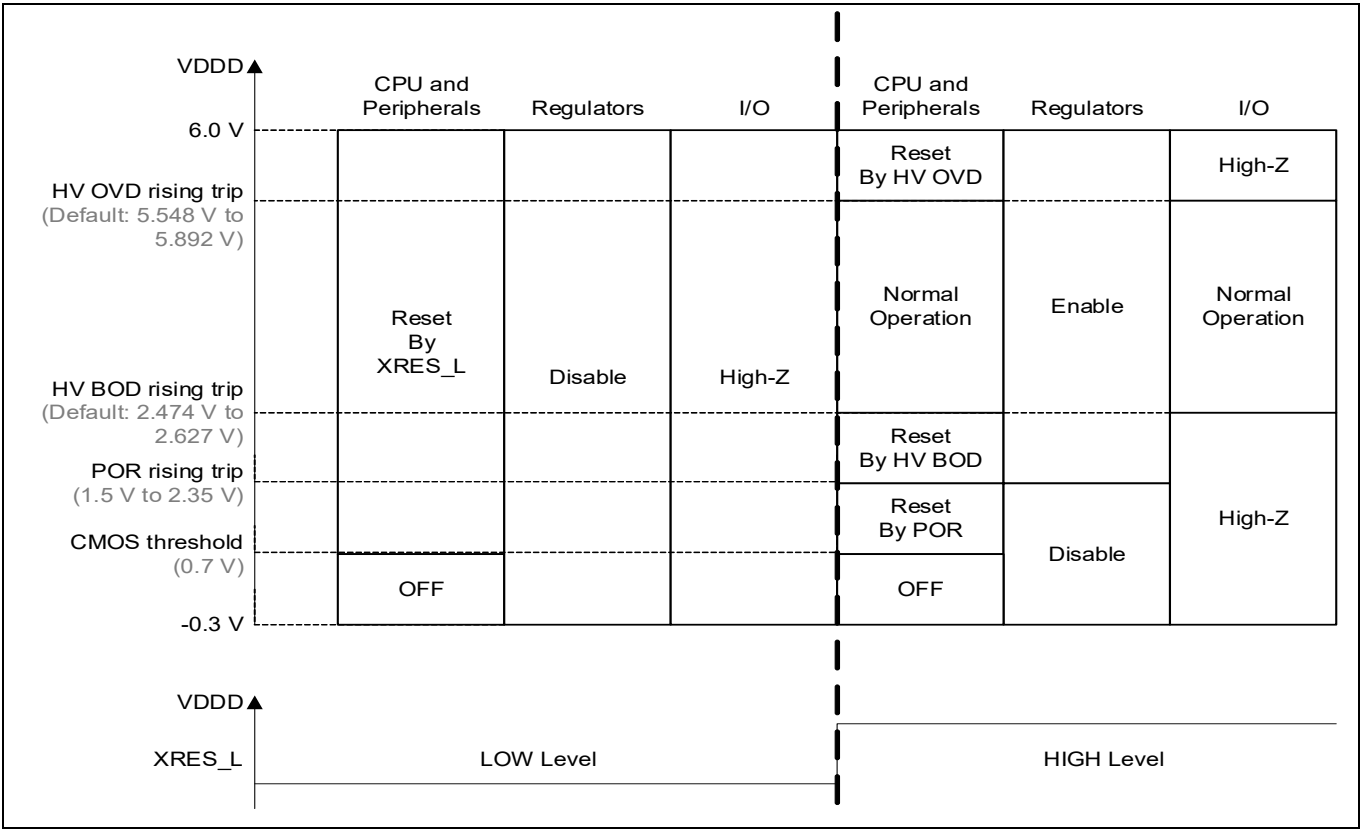
**Table 26-16 System resources** (continued)

| Spec ID | Parameter                | Description                                                                                                                            | Min      | Typ  | Max      | Units | Details/conditions                    |
|---------|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------|----------|------|----------|-------|---------------------------------------|
| SID549  | V <sub>TR_3P1_R</sub>    | LVD 3.1 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 3125 | Typ + 4% | mV    | Same as V <sub>TR_3P1_F</sub> + 25 mV |
| SID550  | V <sub>TR_3P2_R</sub>    | LVD 3.2 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 3225 | Typ + 4% | mV    | Same as V <sub>TR_3P2_F</sub> + 25 mV |
| SID551  | V <sub>TR_3P3_R</sub>    | LVD 3.3 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 3325 | Typ + 4% | mV    | Same as V <sub>TR_3P3_F</sub> + 25 mV |
| SID552  | V <sub>TR_3P4_R</sub>    | LVD 3.4 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 3425 | Typ + 4% | mV    | Same as V <sub>TR_3P4_F</sub> + 25 mV |
| SID553  | V <sub>TR_3P5_R</sub>    | LVD 3.5 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 3525 | Typ + 4% | mV    | Same as V <sub>TR_3P5_F</sub> + 25 mV |
| SID554  | V <sub>TR_3P6_R</sub>    | LVD 3.6 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 3625 | Typ + 4% | mV    | Same as V <sub>TR_3P6_F</sub> + 25 mV |
| SID555  | V <sub>TR_3P7_R</sub>    | LVD 3.7 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 3725 | Typ + 4% | mV    | Same as V <sub>TR_3P7_F</sub> + 25 mV |
| SID556  | V <sub>TR_3P8_R</sub>    | LVD 3.8 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 3825 | Typ + 4% | mV    | Same as V <sub>TR_3P8_F</sub> + 25 mV |
| SID557  | V <sub>TR_3P9_R</sub>    | LVD 3.9 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 3925 | Typ + 4% | mV    | Same as V <sub>TR_3P9_F</sub> + 25 mV |
| SID558  | V <sub>TR_4P0_R</sub>    | LVD 4.0 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 4025 | Typ + 4% | mV    | Same as V <sub>TR_4P0_F</sub> + 25 mV |
| SID559  | V <sub>TR_4P1_R</sub>    | LVD 4.1 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 4125 | Typ + 4% | mV    | Same as V <sub>TR_4P1_F</sub> + 25 mV |
| SID560  | V <sub>TR_4P2_R</sub>    | LVD 4.2 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 4225 | Typ + 4% | mV    | Same as V <sub>TR_4P2_F</sub> + 25 mV |
| SID561  | V <sub>TR_4P3_R</sub>    | LVD 4.3 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 4325 | Typ + 4% | mV    | Same as V <sub>TR_4P3_F</sub> + 25 mV |
| SID562  | V <sub>TR_4P4_R</sub>    | LVD 4.4 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 4425 | Typ + 4% | mV    | Same as V <sub>TR_4P4_F</sub> + 25 mV |
| SID563  | V <sub>TR_4P5_R</sub>    | LVD 4.5 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 4525 | Typ + 4% | mV    | Same as V <sub>TR_4P5_F</sub> + 25 mV |
| SID564  | V <sub>TR_4P6_R</sub>    | LVD 4.6 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 4625 | Typ + 4% | mV    | Same as V <sub>TR_4P6_F</sub> + 25 mV |
| SID565  | V <sub>TR_4P7_R</sub>    | LVD 4.7 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 4725 | Typ + 4% | mV    | Same as V <sub>TR_4P7_F</sub> + 25 mV |
| SID566  | V <sub>TR_4P8_R</sub>    | LVD 4.8 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 4825 | Typ + 4% | mV    | Same as V <sub>TR_4P8_F</sub> + 25 mV |
| SID567  | V <sub>TR_4P9_R</sub>    | LVD 4.9 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 4925 | Typ + 4% | mV    | Same as V <sub>TR_4P9_F</sub> + 25 mV |
| SID568  | V <sub>TR_5P0_R</sub>    | LVD 5.0 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 5025 | Typ + 4% | mV    | Same as V <sub>TR_5P0_F</sub> + 25 mV |
| SID569  | V <sub>TR_5P1_R</sub>    | LVD 5.1 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 5125 | Typ + 4% | mV    | Same as V <sub>TR_5P1_F</sub> + 25 mV |
| SID570  | V <sub>TR_5P2_R</sub>    | LVD 5.2 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 5225 | Typ + 4% | mV    | Same as V <sub>TR_5P2_F</sub> + 25 mV |
| SID571  | V <sub>TR_5P3_R</sub>    | LVD 5.3 V rising detection point for V <sub>DDD</sub>                                                                                  | Typ – 4% | 5325 | Typ + 4% | mV    | Same as V <sub>TR_5P3_F</sub> + 25 mV |
| SID573  | LVD_RR_A                 | Power ramp rate: V <sub>DDD</sub> (Active)                                                                                             | –        | –    | 100      | mV/μs |                                       |
| SID574  | LVD_RR_DS                | Power ramp rate: V <sub>DDD</sub> (DeepSleep)                                                                                          | –        | –    | 10       | mV/μs |                                       |
| SID575  | t <sub>DLY_ACT_LVD</sub> | Active mode delay between V <sub>DDD</sub> falling/rising through LVD rising/falling point and an internal LVD signal transitioning    | –        | –    | 1        | μs    | Guaranteed by design                  |
| SID575A | t <sub>DLY_DS_LVD</sub>  | DeepSleep mode delay between V <sub>DDD</sub> falling/rising through LVD rising/falling point and an internal LVD signal transitioning | –        | –    | 4        | μs    | Guaranteed by design                  |
| SID576  | t <sub>RES_LVD</sub>     | Response time of LVD, V <sub>DDD</sub> supply. (For falling-then-rising supply at max ramp rate; threshold is LVD falling point)       | 100      | –    | –        | ns    | Guaranteed by design                  |

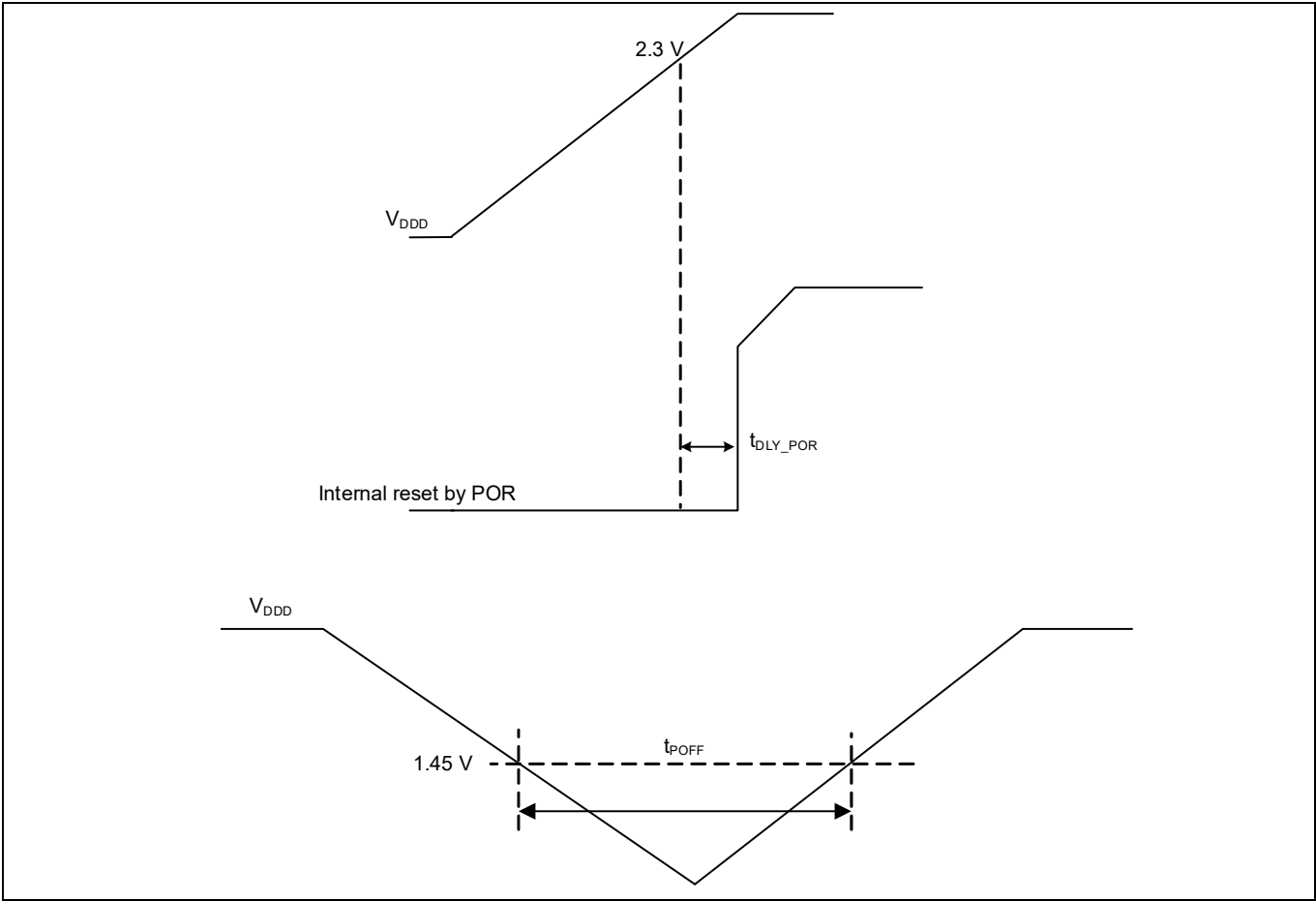
## Electrical specifications

**Table 26-16 System resources** (continued)

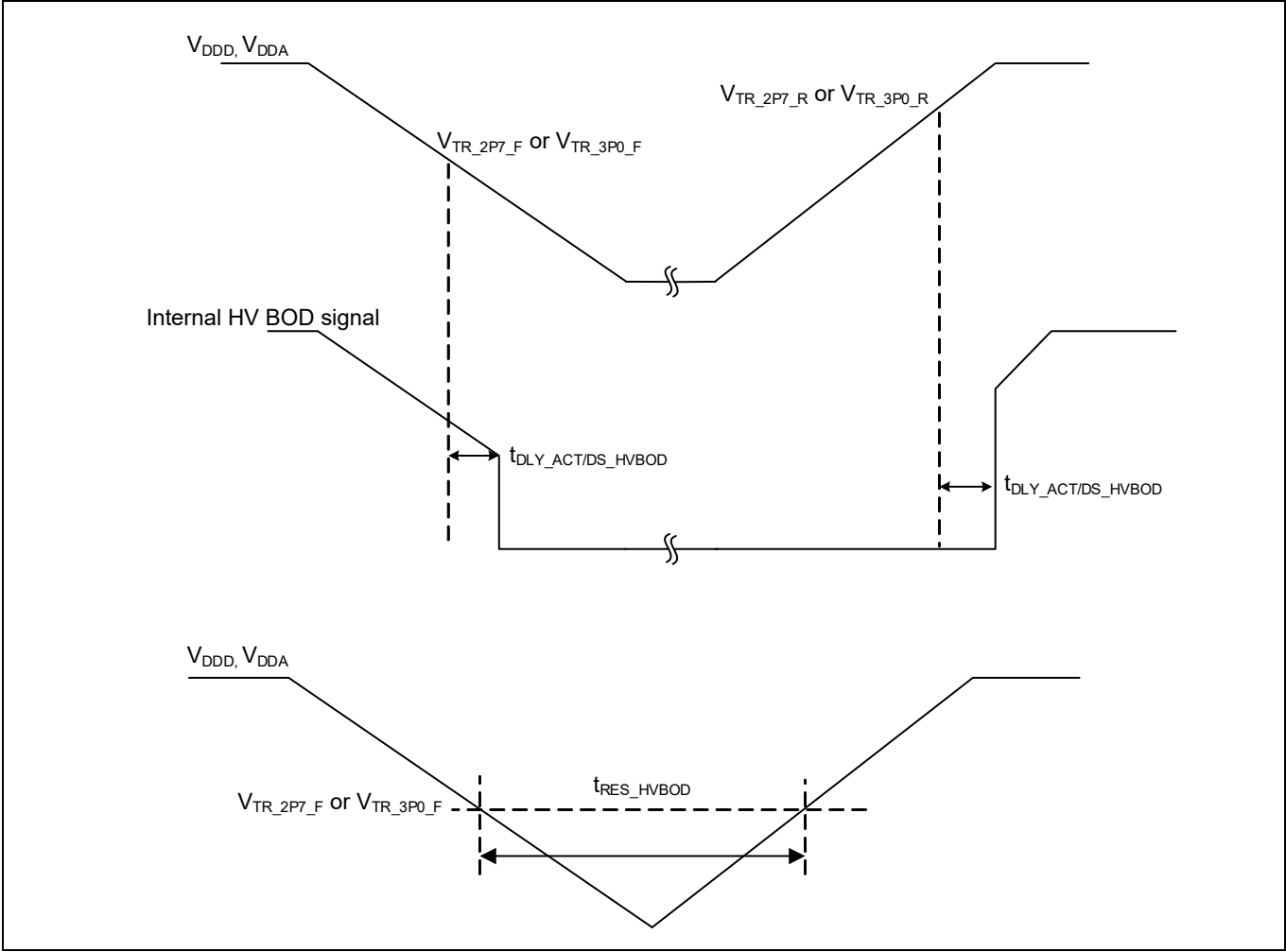
| Spec ID                                            | Parameter                | Description                                                                                                                                                | Min   | Typ   | Max   | Units | Details/conditions   |
|----------------------------------------------------|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-------|-------|----------------------|
| <b>High-voltage OVD specifications</b>             |                          |                                                                                                                                                            |       |       |       |       |                      |
| SID580                                             | $V_{TR\_5P0\_R}$         | HV OVD 5.0-V rising detection point for $V_{DDD}$ and $V_{DDA}$                                                                                            | 5.049 | 5.205 | 5.361 | V     |                      |
| SID581                                             | $V_{TR\_5P0\_F}$         | HV OVD 5.0-V falling detection point for $V_{DDD}$ and $V_{DDA}$                                                                                           | 5.025 | 5.18  | 5.335 | V     |                      |
| SID582                                             | $V_{TR\_5P5\_R}$         | HV OVD 5.5-V rising detection point for $V_{DDD}$ and $V_{DDA}$ (default)                                                                                  | 5.548 | 5.72  | 5.892 | V     |                      |
| SID583                                             | $V_{TR\_5P5\_F}$         | HV OVD 5.5-V falling detection point for $V_{DDD}$ and $V_{DDA}$ (default)                                                                                 | 5.524 | 5.695 | 5.866 | V     |                      |
| SID585                                             | HVOVD_RR_A               | Power ramp rate: $V_{DDD}$ and $V_{DDA}$ (Active)                                                                                                          | –     | –     | 100   | mV/μs |                      |
| SID586                                             | HVOVD_RR_DS              | Power ramp rate: $V_{DDD}$ and $V_{DDA}$ (DeepSleep)                                                                                                       | –     | –     | 10    | mV/μs |                      |
| SID587                                             | $t_{DLY\_ACT\_HVOVD}$    | Active mode delay between $V_{DDD}$ falling/rising through $V_{TR\_5P0\_F/R}$ or $V_{TR\_5P5\_F/R}$ and an internal HV OVD signal transitioning            | –     | –     | 1     | μs    | Guaranteed by design |
| SID587A                                            | $t_{DLY\_ACT\_HVOVD\_A}$ | Active mode delay between $V_{DDA}$ falling/rising through $V_{TR\_5P0\_F/R}$ or $V_{TR\_5P5\_F/R}$ and an internal HV OVD signal transitioning            | –     | –     | 1.5   | μs    | Guaranteed by design |
| SID587B                                            | $t_{DLY\_DS\_HVOVD}$     | DeepSleep mode delay between $V_{DDD}/V_{DDA}$ falling/rising through $V_{TR\_5P0\_F/R}$ or $V_{TR\_5P5\_F/R}$ and an internal HV OVD signal transitioning | –     | –     | 4     | μs    | Guaranteed by design |
| SID588                                             | $t_{RES\_HVOVD}$         | Response time of HV OVD (for rising-then-falling supply at max ramp rate; threshold is $V_{TR\_5P0\_R}$ or $V_{TR\_5P5\_R}$ )                              | 100   | –     | –     | ns    | Guaranteed by design |
| <b>Low-voltage OVD specifications</b>              |                          |                                                                                                                                                            |       |       |       |       |                      |
| SID590                                             | $V_{TR\_R\_LVOVD}$       | LV OVD rising detection point for $V_{CCD}$                                                                                                                | 1.261 | 1.3   | 1.339 | V     |                      |
| SID591                                             | $V_{TR\_F\_LVOVD}$       | LV OVD falling detection point for $V_{CCD}$                                                                                                               | 1.237 | 1.275 | 1.313 | V     |                      |
| SID595                                             | $t_{DLY\_ACT\_LVOVD}$    | Active mode delay between $V_{CCD}$ falling/rising through $V_{TR\_F/R\_LVOVD}$ and an internal LV OVD signal transitioning                                | –     | –     | 1     | μs    | Guaranteed by design |
| SID595A                                            | $t_{DLY\_DS\_LVOVD}$     | DeepSleep mode delay between $V_{CCD}$ falling/rising through $V_{TR\_F/R\_LVOVD}$ and an internal LV OVD signal transitioning                             | –     | –     | 12    | μs    | Guaranteed by design |
| SID596                                             | $t_{RES\_LVOVD}$         | Response time of LV OVD. (For rising-then-falling supply at max ramp rate; threshold is $V_{TR\_R\_LVOVD}$ )                                               | 100   | –     | –     | ns    | Guaranteed by design |
| <b>Over current detection (OCD) specifications</b> |                          |                                                                                                                                                            |       |       |       |       |                      |
| SID598A                                            | $I_{OCD\_LDO}$           | Over current detection range for internal Active regulator                                                                                                 | 312   | –     | 630   | mA    | Guaranteed by design |
| SID598B                                            | $I_{OCD\_EXT}$           | Over current detection range for external transistor mode                                                                                                  | 675   | –     | 825   | mA    |                      |
| SID599                                             | $I_{OCD\_DPSLP}$         | Over current detection range for internal DeepSleep regulator                                                                                              | 18    | –     | 72    | mA    |                      |



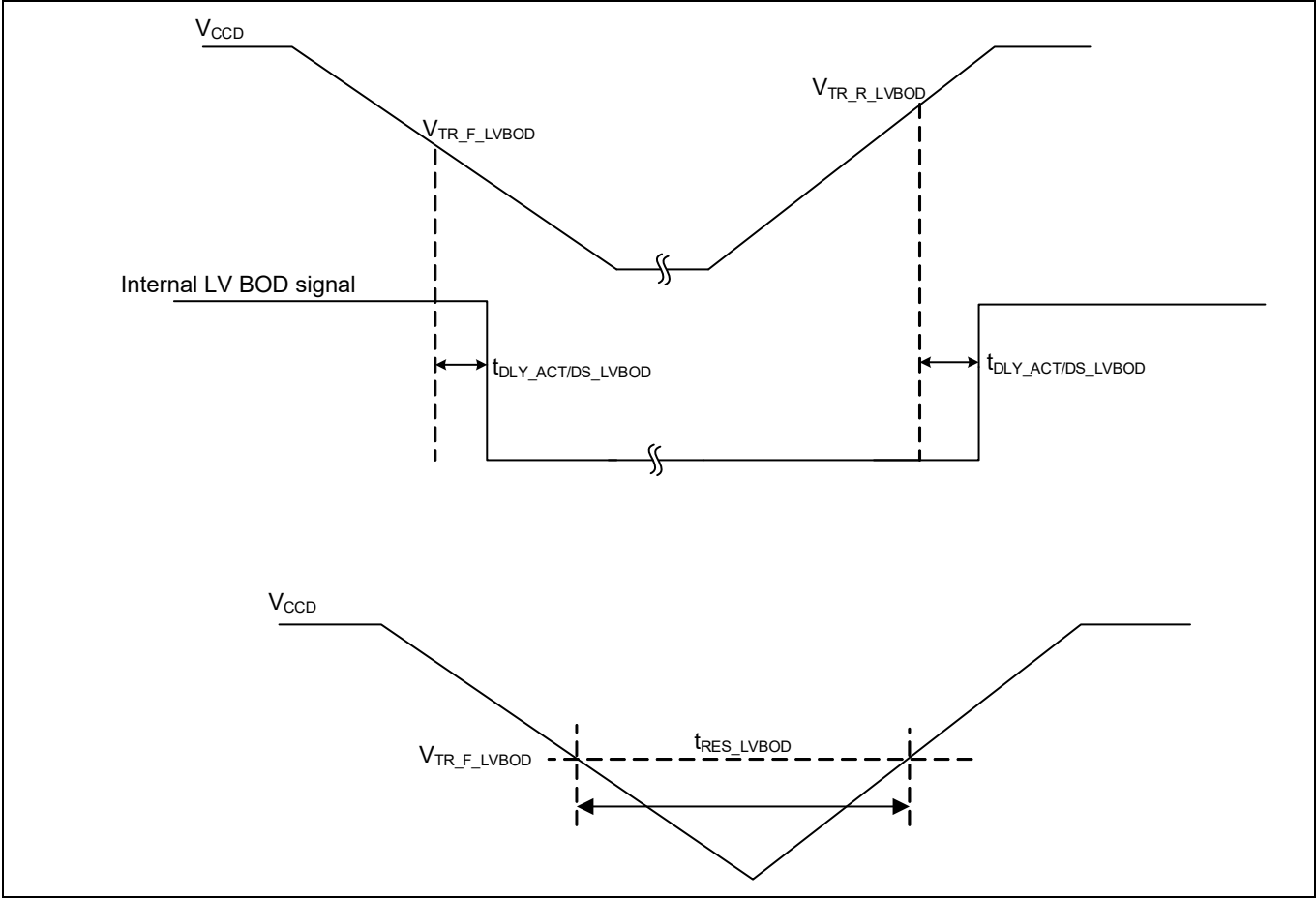
**Figure 26-14 Device operations supply range**



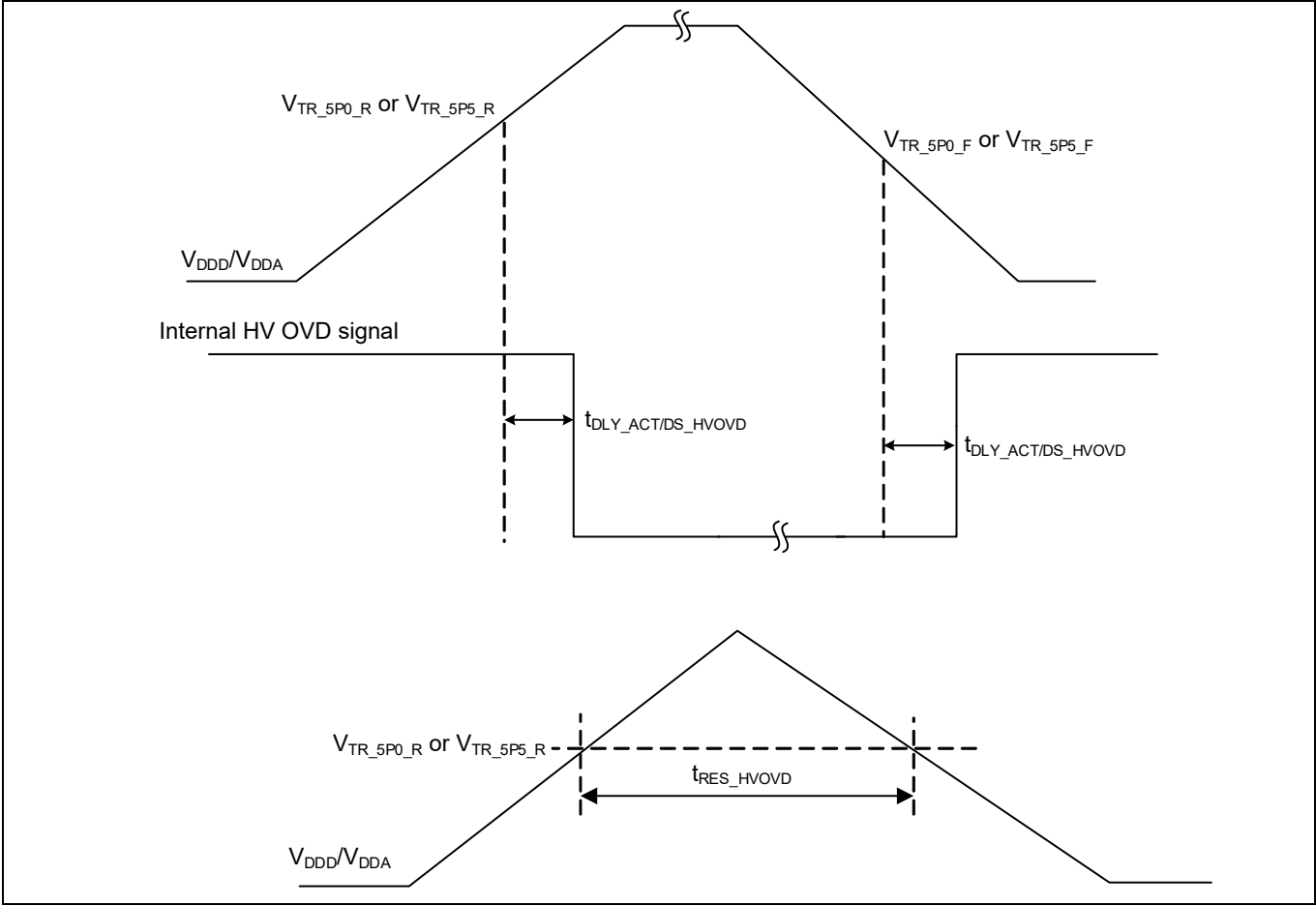
**Figure 26-15** POR specifications



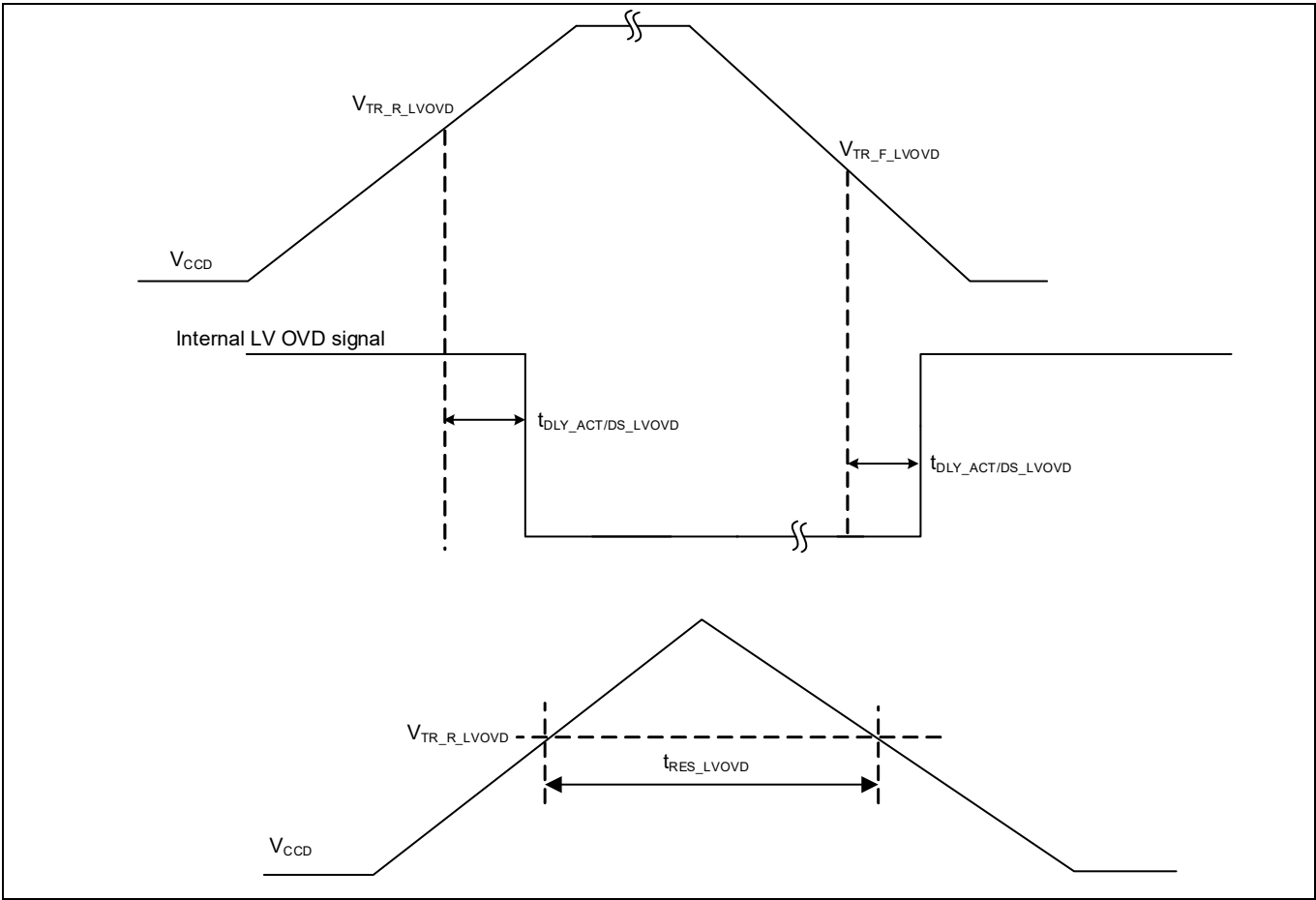
**Figure 26-16 High-voltage BOD specifications**



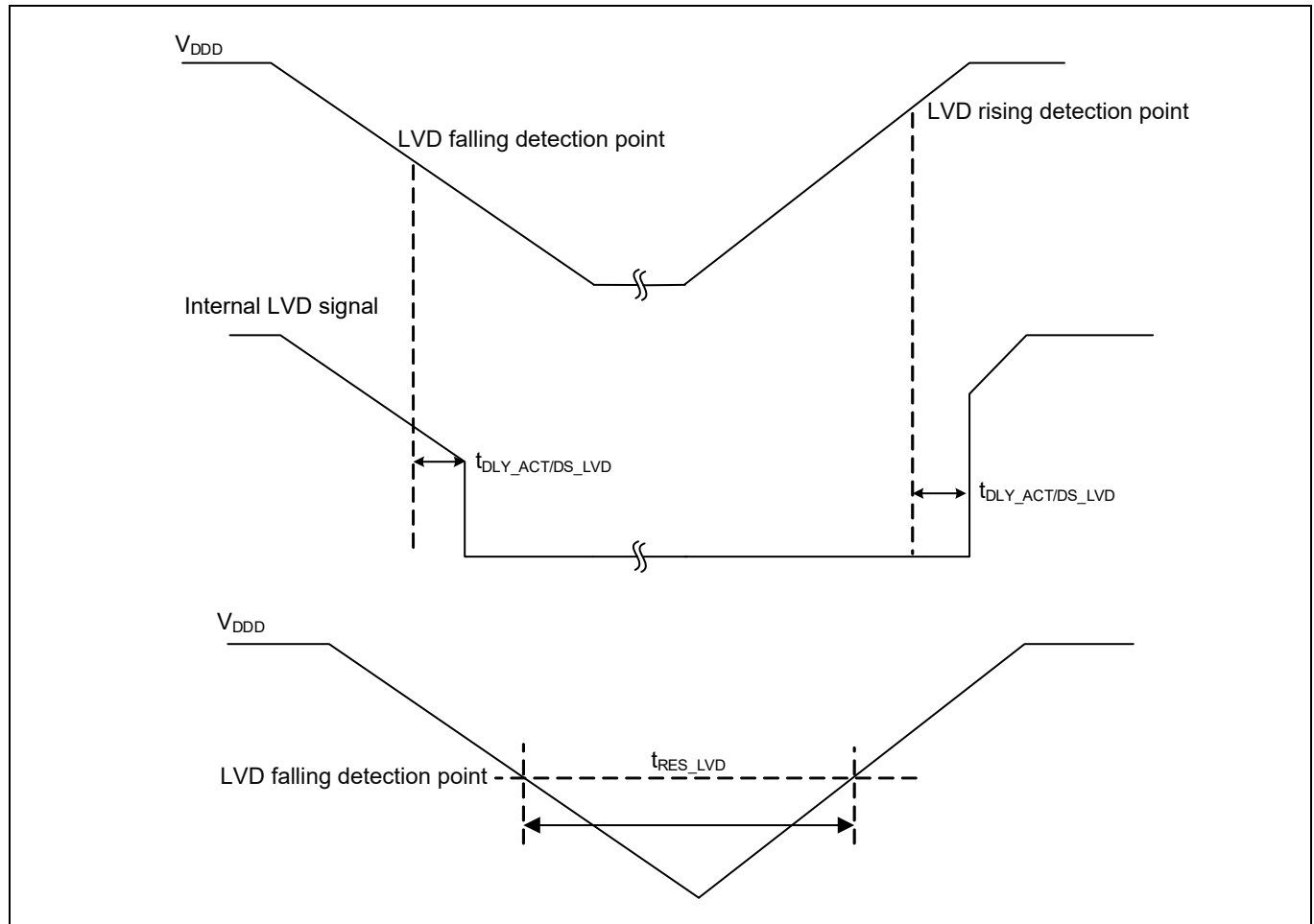
**Figure 26-17 Low-voltage BOD specifications**



**Figure 26-18 High-voltage OVD specifications**



**Figure 26-19 Low-voltage OVD specifications**



**Figure 26-20 LVD specifications**

### 26.10.1 SWD interface

**Table 26-17 SWD interface specifications [Conditions: drive\_sel<1:0>= 00]**

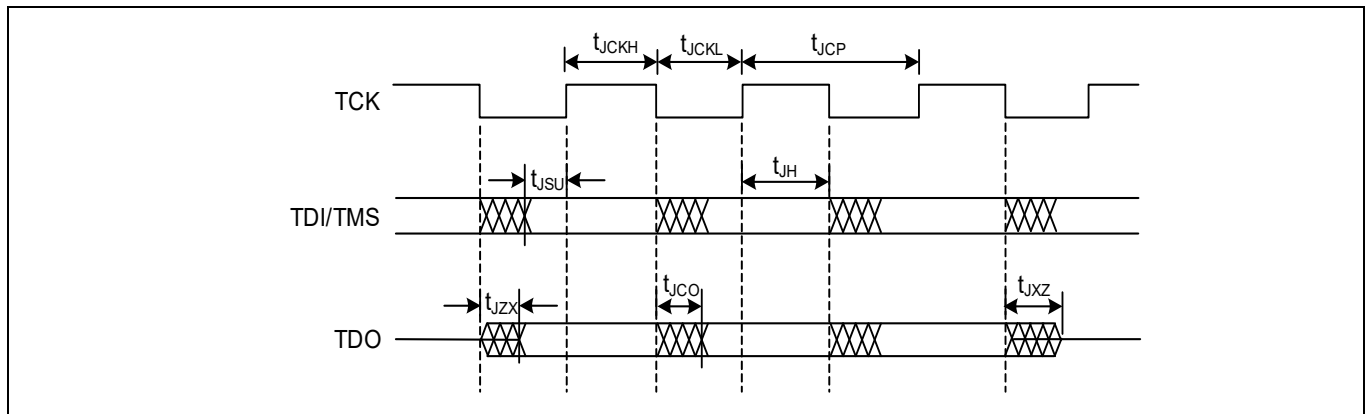
| Spec ID | Parameter         | Description               | Min             | Typ | Max            | Units | Details/conditions                           |
|---------|-------------------|---------------------------|-----------------|-----|----------------|-------|----------------------------------------------|
| SID300  | $f_{SWDCLK}$      | SWD clock input frequency | –               | –   | 10             | MHz   | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |
| SID301  | $t_{SWDI\_SETUP}$ | SWDI setup time           | $0.25 \times T$ | –   | –              | ns    | $T = 1 / f_{SWDCLK}$                         |
| SID302  | $t_{SWDI\_HOLD}$  | SWDI hold time            | $0.25 \times T$ | –   | –              | ns    | $T = 1 / f_{SWDCLK}$                         |
| SID303  | $t_{SWDO\_VALID}$ | SWDO valid time           | –               | –   | $0.5 \times T$ | ns    | $T = 1 / f_{SWDCLK}$                         |
| SID304  | $t_{SWDO\_HOLD}$  | SWDO hold time            | 1               | –   | –              | ns    | $T = 1 / f_{SWDCLK}$                         |

**Table 26-18 JTAG AC specifications [Conditions: drive\_sel<1:0>= 00]**

| Spec ID | Parameter  | Description        | Min  | Typ | Max | Units | Details/conditions |
|---------|------------|--------------------|------|-----|-----|-------|--------------------|
| SID620  | $t_{JCKH}$ | TCK HIGH time      | 30   | –   | –   | ns    | 30-pF load         |
| SID621  | $t_{JCKL}$ | TCK LOW time       | 30   | –   | –   | ns    | 30-pF load         |
| SID622  | $t_{JCP}$  | TCK clock period   | 66.7 | –   | –   | ns    | 30-pF load         |
| SID623  | $t_{JSU}$  | TDI/TMS setup time | 12   | –   | –   | ns    | 30-pF load         |
| SID624  | $t_{JH}$   | TDI/TMS hold time  | 12   | –   | –   | ns    | 30-pF load         |

**Table 26-18 JTAG AC specifications [Conditions: drive\_sel<1:0>= 00] (continued)**

| Spec ID | Parameter | Description          | Min | Typ | Max | Units | Details/conditions |
|---------|-----------|----------------------|-----|-----|-----|-------|--------------------|
| SID625  | $t_{JZX}$ | TDO High-Z to active | –   | –   | 30  | ns    | 30-pF load         |
| SID626  | $t_{JXZ}$ | TDO active to High-Z | –   | –   | 30  | ns    | 30-pF load         |
| SID627  | $t_{JCO}$ | TDO clock to output  | –   | –   | 30  | ns    | 30-pF load         |


**Figure 26-21 JTAG specifications**
**Table 26-19 Trace specifications [Conditions: drive\_sel<1:0>= 00]**

| Spec ID  | Parameter          | Description                  | Min | Typ | Max | Units | Details/conditions                |
|----------|--------------------|------------------------------|-----|-----|-----|-------|-----------------------------------|
| SID1412A | $C_{TRACE}$        | Trace capacitive load        | –   | –   | 30  | pF    |                                   |
| SID1412  | $t_{TRACE\_CYC}$   | Trace clock period           | 40  | –   | –   | ns    | Trace clock cycle time for 25 MHz |
| SID1413  | $t_{TRACE\_CLKL}$  | Trace clock LOW pulse width  | 2   | –   | –   | ns    | Clock low pulse width             |
| SID1414  | $t_{TRACE\_CLKH}$  | Trace clock HIGH pulse width | 2   | –   | –   | ns    | Clock high pulse width            |
| SID1415A | $t_{TRACE\_SETUP}$ | Trace data setup time        | 3   | –   | –   | ns    | Trace data setup time             |
| SID1416A | $t_{TRACE\_HOLD}$  | Trace data hold time         | 2   | –   | –   | ns    | Trace data hold time              |

## 26.11 Clock specifications

All specifications are valid for  $-40\text{ °C} \leq T_A \leq 125\text{ °C}$  and for 2.7 V to 5.5 V except where noted.

**Table 26-20 Root and intermediate clocks<sup>[67]</sup>**

| Clock      | Max permitted clock frequency (MHz) <sup>[68]</sup> | Source   | Maximum permitted clock frequency setting (MHz) <sup>[68]</sup> |      |            |                                           |      |            | Description                                                                                                                |
|------------|-----------------------------------------------------|----------|-----------------------------------------------------------------|------|------------|-------------------------------------------|------|------------|----------------------------------------------------------------------------------------------------------------------------|
|            |                                                     |          | PLL/FLL Clock source: ECO <sup>[69]</sup>                       |      |            | PLL/FLL Clock source: IMO <sup>[70]</sup> |      |            |                                                                                                                            |
|            |                                                     |          | Integer                                                         | SSCG | Fractional | Integer                                   | SSCG | Fractional |                                                                                                                            |
| CLK_HF0    | 160                                                 | PLL200#0 | 160                                                             | NA   | NA         | 155                                       | NA   | NA         | Root clock for CPUSS, PERI                                                                                                 |
|            |                                                     | FLL      | 100                                                             | NA   | NA         | 96                                        | NA   | NA         |                                                                                                                            |
|            | 100                                                 | PLL200#0 | 100                                                             | NA   | NA         | 98                                        | NA   | NA         |                                                                                                                            |
|            |                                                     | FLL      | 100                                                             | NA   | NA         | 96                                        | NA   | NA         |                                                                                                                            |
| CLK_HF1    | 250                                                 | PLL400#0 | 250                                                             | 240  | 250        | 242                                       | 237  | 239        | CM7 CPU Core#0, CM7 CPU Core#1 clock                                                                                       |
|            |                                                     | FLL      | 100                                                             | NA   | NA         | 96                                        | NA   | NA         |                                                                                                                            |
| CLK_HF2    | 100                                                 | PLL200#1 | 100                                                             | NA   | NA         | 98                                        | NA   | NA         | Peripheral clock root other than CLK_PERI                                                                                  |
|            |                                                     | FLL      | 100                                                             | NA   | NA         | 96                                        | NA   | NA         |                                                                                                                            |
| CLK_HF3    | 100                                                 | PLL200#1 | 100                                                             | NA   | NA         | 98                                        | NA   | NA         | Event generator (CLK_REF), clock output on EXT_CLK pins (when used as output)                                              |
|            |                                                     | FLL      | 100                                                             | NA   | NA         | 96                                        | NA   | NA         |                                                                                                                            |
| CLK_HF4    | 50                                                  | PLL200#1 | 50                                                              | NA   | NA         | 48                                        | NA   | NA         | Ethernet Channel#0, Ethernet Channel#1 internal clock                                                                      |
|            |                                                     | FLL      | 50                                                              | NA   | NA         | 48                                        | NA   | NA         |                                                                                                                            |
| CLK_HF5    | 196.608                                             | PLL400#1 | 196.608                                                         | 193  | 196.608    | 189                                       | 185  | 187        | I <sup>2</sup> S channel#0, I <sup>2</sup> S channel#1, I <sup>2</sup> S channel#2 interface clock, Ethernet Channel#0 TSU |
|            |                                                     | FLL      | 100                                                             | NA   | NA         | 96                                        | NA   | NA         |                                                                                                                            |
| CLK_HF6    | 200                                                 | PLL200#1 | 200                                                             | NA   | NA         | 190                                       | NA   | NA         | Root clock for SDHC, SMIF interface clock                                                                                  |
|            |                                                     | FLL      | 100                                                             | NA   | NA         | 96                                        | NA   | NA         |                                                                                                                            |
| CLK_HF7    | 8                                                   | ILO      | NA                                                              | NA   | NA         | NA                                        | NA   | NA         | CSV                                                                                                                        |
| CLK_FAST_0 | 250                                                 | PLL400#0 | 250                                                             | 240  | 250        | 242                                       | 237  | 239        | Generated by clock gating CLK_HF1, CM7 CPU Core#0, intermediate clock                                                      |
|            |                                                     | FLL      | 100                                                             | NA   | NA         | 96                                        | NA   | NA         |                                                                                                                            |
| CLK_FAST_1 | 250                                                 | PLL400#0 | 250                                                             | 240  | 250        | 242                                       | 237  | 239        | Generated by clock gating CLK_HF1, CM7 CPU Core#1, intermediate clock                                                      |
|            |                                                     | FLL      | 100                                                             | NA   | NA         | 96                                        | NA   | NA         |                                                                                                                            |

### Notes

67. Intermediate clocks that are not listed have the same limitations as that of their parent clock.

68. Maximum clock frequency after the corresponding clock source (PLL/FLL + dividers). All internal tolerances and affects are covered by these frequencies.

69. For ECO: up to  $\pm 150$  ppm uncertainty of the external clock source are tolerated by design.

70. The IMO operation frequency tolerance is included. When DeepSleep mode isn't used, maximum permitted clock frequency setting of clock source IMO case is equal to clock source ECO case.

71. CLOCK\_SLOW and CLK\_HF0 are related by integer frequency ratio (that is, 1:1, 1:2, 1:3, and so on).

**Table 26-20 Root and intermediate clocks<sup>[67]</sup>**

| Clock    | Max permitted clock frequency (MHz) <sup>[68]</sup> | Source   | Maximum permitted clock frequency setting (MHz) <sup>[68]</sup> |      |            |                                           |      |            | Description                                                                                      |
|----------|-----------------------------------------------------|----------|-----------------------------------------------------------------|------|------------|-------------------------------------------|------|------------|--------------------------------------------------------------------------------------------------|
|          |                                                     |          | PLL/FLL Clock source: ECO <sup>[69]</sup>                       |      |            | PLL/FLL Clock source: IMO <sup>[70]</sup> |      |            |                                                                                                  |
|          |                                                     |          | Integer                                                         | SSCG | Fractional | Integer                                   | SSCG | Fractional |                                                                                                  |
| CLK_MEM  | 160                                                 | PLL200#0 | 160                                                             | NA   | NA         | 155                                       | NA   | NA         | Generated by clock gating CLK_HF0, intermediate clock for SMIF, Flash, Ethernet                  |
|          |                                                     | FLL      | 100                                                             | NA   | NA         | 96                                        | NA   | NA         |                                                                                                  |
|          | 100                                                 | PLL200#0 | 100                                                             | NA   | NA         | 98                                        | NA   | NA         |                                                                                                  |
|          |                                                     | FLL      | 100                                                             | NA   | NA         | 96                                        | NA   | NA         |                                                                                                  |
| CLK_SLOW | 100                                                 | PLL200#0 | 100                                                             | NA   | NA         | 98                                        | NA   | NA         | Generated by clock gating CLK_MEM, intermediate clock for CM0+, P-DMA, M-DMA, Crypto, SMIF, SDHC |
|          |                                                     | FLL      | 100                                                             | NA   | NA         | 96                                        | NA   | NA         |                                                                                                  |
| CLK_PERI | 100                                                 | PLL200#0 | 100                                                             | NA   | NA         | 98                                        | NA   | NA         | Generated by clock gating CLK_HF0, intermediate clock for IOSS, TCPWM0, CPU trace, SMIF          |
|          |                                                     | FLL      | 100                                                             | NA   | NA         | 96                                        | NA   | NA         |                                                                                                  |

**Table 26-21 Relation between CLK\_HF0 and CLK\_SLOW (Example)<sup>[71]</sup>**

| CLK_HF0 (MHz) | CLK_SLOW (MHz) |
|---------------|----------------|
| 160           | 80             |
| 120           | 60             |
| 100           | 100            |
| 80            | 80             |

**Table 26-22 IMO AC specifications**

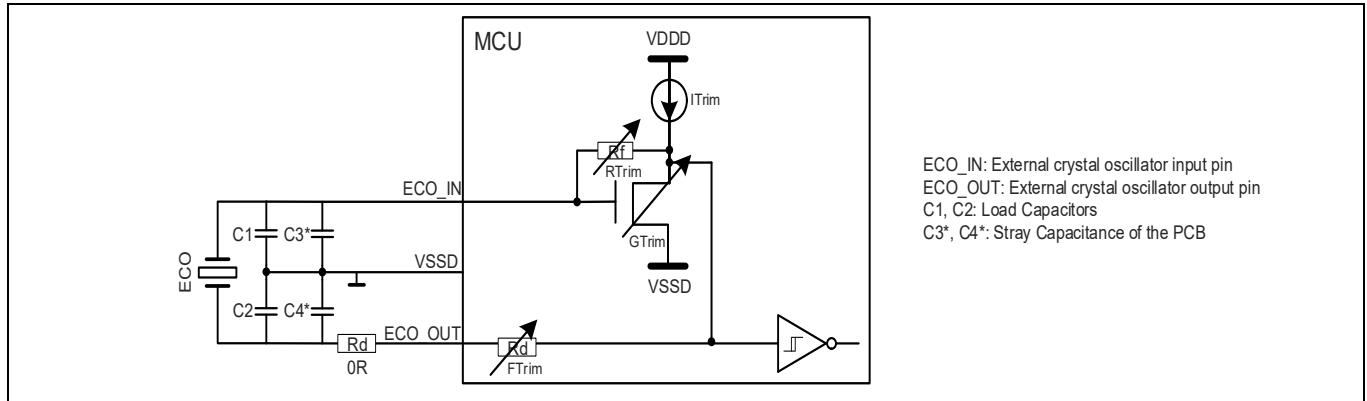
| Spec ID | Parameter             | Description             | Min  | Typ  | Max  | Units | Details/conditions                      |
|---------|-----------------------|-------------------------|------|------|------|-------|-----------------------------------------|
| SID310  | f <sub>IMOTOL</sub>   | IMO operating frequency | 7.68 | 8    | 8.32 | MHz   |                                         |
| SID311  | t <sub>STARTIMO</sub> | IMO start-up time       | –    | –    | 7.5  | μs    | Start-up time to 90% of final frequency |
| SID312  | I <sub>IMO_ACT</sub>  | IMO current             | –    | 13.5 | 22   | μA    |                                         |

**Table 26-23 ILO AC specifications**

| Spec ID | Parameter             | Description             | Min      | Typ    | Max      | Units | Details/conditions                      |
|---------|-----------------------|-------------------------|----------|--------|----------|-------|-----------------------------------------|
| SID320  | f <sub>ILOTRIM</sub>  | ILO operating frequency | 30.47424 | 32.768 | 35.06176 | kHz   |                                         |
| SID321  | t <sub>STARTILO</sub> | ILO start-up time       | –        | 8      | 12       | μs    | Start-up time to 90% of final frequency |
| SID323  | I <sub>ILO</sub>      | ILO current             | –        | 500    | 2800     | nA    |                                         |

**Table 26-24 ECO specifications**

| Spec ID | Parameter              | Description                                                                                  | Min | Typ | Max   | Units | Details/conditions                                                                                               |
|---------|------------------------|----------------------------------------------------------------------------------------------|-----|-----|-------|-------|------------------------------------------------------------------------------------------------------------------|
| SID330  | f <sub>ECO</sub>       | Crystal frequency range                                                                      | 8   | –   | 33.34 | MHz   |                                                                                                                  |
| SID332  | R <sub>FDBK</sub>      | Feedback resistor value.<br>Min: RTRIM = 3; Max: RTRIM = 0<br>with 100-kΩ step size on RTRIM | 100 | –   | 400   | kΩ    | Guaranteed by design                                                                                             |
| SID333  | I <sub>ECO3</sub>      | ECO current at T <sub>J</sub> = 150 °C                                                       | –   | –   | 2000  | μA    | Maximum operation current with a 33-MHz crystal, 18-pF load                                                      |
| SID334  | t <sub>START_8M</sub>  | 8-MHz ECO start-up time <sup>[72]</sup>                                                      | –   | –   | 10    | ms    | Time from set CLK_ECO_-CONFIG.ECO_EN to 1 until CLK_ECO_STATUS.ECO_READY is set to 1 (See Clock Timing Diagrams) |
| SID335  | t <sub>START_33M</sub> | 33-MHz ECO start-up time <sup>[72]</sup>                                                     | –   | –   | 1     | ms    | Time from set CLK_ECO_-CONFIG.ECO_EN to 1 until CLK_ECO_STATUS.ECO_READY is set to 1 (See Clock Timing Diagrams) |


**Figure 26-22 ECO connection scheme**<sup>[73]</sup>
**Table 26-25 PLL specifications**

| Spec ID                                                                     | Parameter                 | Description                     | Min   | Typ | Max  | Units | Details/conditions                                                                                                                                                                            |
|-----------------------------------------------------------------------------|---------------------------|---------------------------------|-------|-----|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>PLL (without SSCG and fractional divider) specifications for 200 MHz</b> |                           |                                 |       |     |      |       |                                                                                                                                                                                               |
| SID340                                                                      | $t_{\text{PLL200\_LOCK}}$ | Time to achieve PLL lock        | –     | –   | 35   | μs    | Time from stable reference clock until PLL frequency is within 0.1% of final value and lock indicator is set                                                                                  |
| SID341                                                                      | $f_{\text{PLL\_OUT}}$     | Output frequency from PLL block | 11    | –   | 200  | MHz   |                                                                                                                                                                                               |
| SID342                                                                      | PLL_LJIT1                 | Long term jitter                | –0.25 | –   | 0.25 | ns    | For 125 ns<br>Guaranteed by design<br>$f_{\text{PLL\_VCO}}$ : 320 MHz or 400 MHz<br>$f_{\text{PLL\_OUT}}$ : 40 MHz to 200 MHz<br>$f_{\text{PLL\_PFD}}$ : 8 MHz<br>$f_{\text{PLL\_IN}}$ : ECO  |
| SID343                                                                      | PLL_LJIT2                 | Long term jitter                | –0.5  | –   | 0.5  | ns    | For 500 ns<br>Guaranteed by design<br>$f_{\text{PLL\_VCO}}$ : 320 MHz or 400 MHz<br>$f_{\text{PLL\_OUT}}$ : 40 MHz to 200 MHz<br>$f_{\text{PLL\_PFD}}$ : 8 MHz<br>$f_{\text{PLL\_IN}}$ : ECO  |
| SID344                                                                      | PLL_LJIT3                 | Long term jitter                | –0.5  | –   | 0.5  | ns    | For 1000 ns<br>Guaranteed by design<br>$f_{\text{PLL\_VCO}}$ : 320 MHz or 400 MHz<br>$f_{\text{PLL\_OUT}}$ : 40 MHz to 200 MHz<br>$f_{\text{PLL\_PFD}}$ : 8 MHz<br>$f_{\text{PLL\_IN}}$ : ECO |

**Notes**

72. Mainly depends on the external crystal.

73. Refer to the family-specific Architecture TRM for more information on crystal requirements (002-24401, TRAVEO™ T2G Automotive MCU body controller high architecture technical reference manual).

**Table 26-25 PLL specifications (continued)**

| Spec ID                                                                  | Parameter          | Description                                                | Min   | Typ  | Max   | Units | Details/conditions                                                                                                                                                 |
|--------------------------------------------------------------------------|--------------------|------------------------------------------------------------|-------|------|-------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID345A1                                                                 | PLL_LJIT5          | Long term jitter                                           | -0.75 | -    | 0.75  | ns    | For 10000 ns<br>Guaranteed by design<br>$f_{PLL\_VCO}$ : 320 MHz or 400 MHz<br>$f_{PLL\_OUT}$ : 40 MHz to 200 MHz<br>$f_{PLL\_PFD}$ : 8 MHz<br>$f_{PLL\_IN}$ : ECO |
| SID346                                                                   | $f_{PLL\_IN}$      | PLL input frequency                                        | 3.988 | -    | 33.34 | MHz   |                                                                                                                                                                    |
| SID347                                                                   | $I_{PLL\_200M}$    | PLL operating current<br>( $f_{OUT} = 200$ MHz)            | -     | 0.87 | 1.8   | mA    | $f_{OUT} = 200$ MHz                                                                                                                                                |
| SID348C                                                                  | $f_{PLL\_VCO}$     | VCO frequency                                              | 170   | -    | 400   | MHz   |                                                                                                                                                                    |
| SID349C                                                                  | $f_{PLL\_PFD}$     | PFD frequency                                              | 3.988 | -    | 8     | MHz   |                                                                                                                                                                    |
| <b>PLL (with SSCG and fractional divider) specifications for 400 MHz</b> |                    |                                                            |       |      |       |       |                                                                                                                                                                    |
| SID340A                                                                  | $t_{PLL400\_LOCK}$ | Time to achieve PLL lock                                   | -     | -    | 50    | μs    | Time from stable reference clock until PLL frequency is within 0.1% of final value and lock indicator is set                                                       |
| SID341A4                                                                 | $f_{OUT0\_4M}$     | Programmed output frequency from PLL Block (spreading off) | 25    | -    | 250   | MHz   | Spreading off                                                                                                                                                      |
| SID341B4                                                                 | $f_{OUT1\_4M}$     | Programmed output frequency from PLL Block (spreading on)  | 25    | -    | 240   | MHz   | Spreading on                                                                                                                                                       |
| SID343A                                                                  | SPREAD_D           | Spread spectrum modulation depth                           | 0.5   | -    | 3     | %     | Downspread only, triangle modulation                                                                                                                               |
| SID343B                                                                  | $f_{SPREAD\_MR}$   | Spread spectrum modulation rate                            | -     | -    | 32    | kHz   | Selected by modulation divider from $f_{PFD}$                                                                                                                      |
| SID342D14                                                                | PLL400_L-JIT14     | Long term jitter                                           | -0.25 | -    | 0.25  | ns    | For 125 ns<br>Guaranteed by design<br>$f_{VCO}$ : 800 MHz or 500 MHz (spreading is off)<br>$f_{IN}$ : ECO<br>$f_{PFD}$ : 4 MHz<br>$f_{OUT}$ : 100 MHz to 250 MHz   |
| SID343D14                                                                | PLL400_L-JIT24     | Long term jitter                                           | -0.5  | -    | 0.5   | ns    | For 500 ns<br>Guaranteed by design<br>$f_{VCO}$ : 800 MHz or 500 MHz (spreading is off)<br>$f_{IN}$ : ECO<br>$f_{PFD}$ : 4 MHz<br>$f_{OUT}$ : 100 MHz to 250 MHz   |
| SID344D14                                                                | PLL400_L-JIT34     | Long term jitter                                           | -1    | -    | 1     | ns    | For 1000 ns<br>Guaranteed by design<br>$f_{VCO}$ : 800 MHz or 500 MHz (spreading is off)<br>$f_{IN}$ : ECO<br>$f_{PFD}$ : 4 MHz<br>$f_{OUT}$ : 100 MHz to 250 MHz  |

Electrical specifications

**Table 26-25 PLL specifications** (continued)

| Spec ID   | Parameter                | Description                                       | Min   | Typ | Max   | Units | Details/conditions                                                                                                                                                    |
|-----------|--------------------------|---------------------------------------------------|-------|-----|-------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID345E14 | PLL400_L-JIT54           | Long term jitter                                  | -1.5  | -   | 1.5   | ns    | For 10000 ns<br>Guaranteed by design<br>$f_{VCO}$ : 800 MHz or 500 MHz<br>(spreading is off)<br>$f_{IN}$ : ECO<br>$f_{PFD}$ : 4 MHz<br>$f_{OUT}$ : 100 MHz to 250 MHz |
| SID345A   | $f_{VCO}$                | VCO frequency                                     | 400   | -   | 800   | MHz   |                                                                                                                                                                       |
| SID346A   | $f_{IN}$                 | PLL input frequency                               | 3.988 | -   | 33.34 | MHz   |                                                                                                                                                                       |
| SID347A   | $I_{PLL\_400M}$          | PLL operating current<br>( $f_{OUT} = 400$ MHz)   | -     | 1.4 | 2.2   | mA    | $f_{OUT} = 400$ MHz                                                                                                                                                   |
| SID348A   | $f_{PFD\_S}$             | PFD Frequency<br>( $f_{IN}$ / Reference divider)  | 3.988 | -   | 20    | MHz   | Spreading off/on                                                                                                                                                      |
| SID349A   | $f_{PFD\_F}$             | PFD Frequency<br>( $f_{IN}$ / Reference divider)  | 8     | -   | 20    | MHz   | Fractional operation                                                                                                                                                  |
| SID341C   | $f_{OUT\_400\_8S1}$      | Output frequency from<br>PLL Block (spreading on) | 93    | -   | 105   | MHz   | $f_{PFD} = 8$ MHz,<br>$f_{VCO} = 400$ MHz,<br>$f_{OUT} = 100$ MHz,<br>Modulation frequency:<br>$f_{PFD} / 512$ ,<br>Modulation depth: 3%                              |
| SID342C   | $t_{PLL\_C-JIT400\_8S1}$ | Cycle-to-cycle jitter<br>(spreading on)           | -710  | -   | 710   | ps    | $f_{PFD} = 8$ MHz,<br>$f_{VCO} = 400$ MHz,<br>$f_{OUT} = 100$ MHz,<br>Modulation frequency:<br>$f_{PFD} / 512$ ,<br>Modulation depth: 3%                              |
| SID341D   | $f_{OUT\_400\_8S2}$      | Output frequency from<br>PLL Block (spreading on) | 93    | -   | 105   | MHz   | $f_{PFD} = 8$ MHz,<br>$f_{VCO} = 400$ MHz,<br>$f_{OUT} = 100$ MHz,<br>Modulation frequency:<br>$f_{PFD} / 256$ ,<br>Modulation depth: 3%                              |
| SID342D   | $t_{PLL\_C-JIT400\_8S2}$ | Cycle-to-cycle jitter<br>(spreading on)           | -710  | -   | 710   | ps    | $f_{PFD} = 8$ MHz,<br>$f_{VCO} = 400$ MHz,<br>$f_{OUT} = 100$ MHz,<br>Modulation frequency:<br>$f_{PFD} / 256$ ,<br>Modulation depth: 3%                              |

**Table 26-26 FLL specifications**

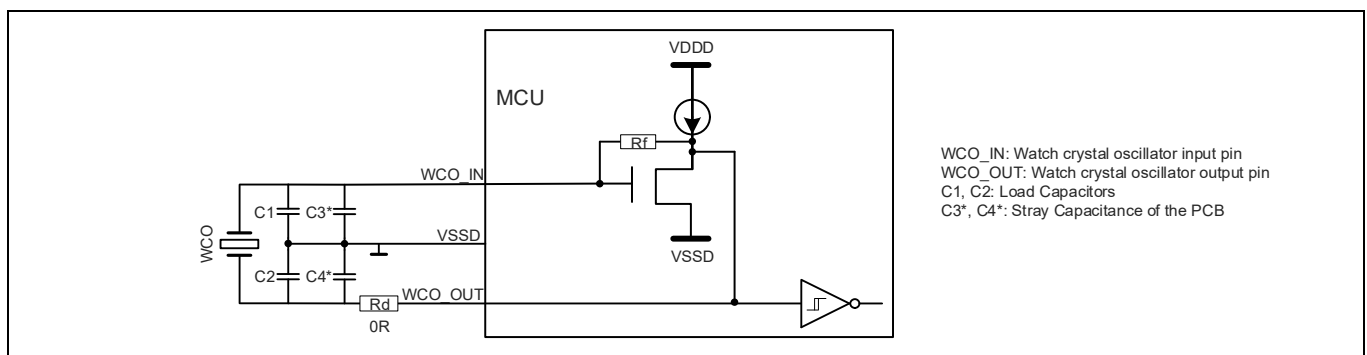
| Spec ID | Parameter       | Description                        | Min | Typ | Max | Units | Details/conditions                                                                                                                                                                                                   |
|---------|-----------------|------------------------------------|-----|-----|-----|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SID350  | $t_{FLL\_WAKE}$ | FLL wake up time                   | -   | -   | 5   | μs    | Wakeup with < 10 °C<br>temperature change<br>while in DeepSleep.<br>$f_{FLL\_IN} = 8$ MHz,<br>$f_{FLL\_OUT} = 100$ MHz,<br>Time from stable<br>reference clock until<br>FLL frequency is within<br>5% of final value |
| SID351  | $f_{FLL\_OUT}$  | Output frequency from FLL<br>block | 24  | -   | 100 | MHz   | Output range of FLL<br>divided-by-2 output                                                                                                                                                                           |

**Table 26-26 FLL specifications**

| Spec ID | Parameter     | Description            | Min  | Typ | Max | Units   | Details/conditions                                                                         |
|---------|---------------|------------------------|------|-----|-----|---------|--------------------------------------------------------------------------------------------|
| SID352  | FLL_CJIT      | FLL frequency accuracy | -1   | -   | 1   | %       | This is added to the error of the source                                                   |
| SID353  | $f_{FLL\_IN}$ | Input frequency        | 0.25 | -   | 80  | MHz     |                                                                                            |
| SID354  | $I_{FLL}$     | FLL operating current  | -    | 250 | 360 | $\mu A$ | Reference clock: IMO, CCO frequency: 200 MHz, FLL frequency: 100 MHz, guaranteed by design |

**Table 26-27 WCO specifications**

| Spec ID | Parameter         | Description                       | Min | Typ    | Max  | Units   | Details/conditions                                                                                                |
|---------|-------------------|-----------------------------------|-----|--------|------|---------|-------------------------------------------------------------------------------------------------------------------|
| SID360  | $f_{WCO}$         | Crystal frequency                 | -   | 32.768 | -    | kHz     | Maximum drive level: 0.5 $\mu W$                                                                                  |
| SID361  | WCO_DC            | WCO duty cycle                    | 10  | -      | 90   | %       |                                                                                                                   |
| SID362  | $t_{START\_WCO}$  | WCO start up time <sup>[74]</sup> | -   | -      | 1000 | ms      | For Grade-S devices<br>Time from set CTL.WCO_EN to 1 until STATUS.WCO_OK is set to 1. (See Clock Timing Diagrams) |
| SID362E | $t_{START\_WCOE}$ | WCO start-up time <sup>[74]</sup> | -   | -      | 1400 | ms      | For Grade-E devices<br>Time from set CTL.WCO_EN to 1 until STATUS.WCO_OK is set to 1. (See Clock Timing Diagrams) |
| SID363  | $I_{WCO}$         | WCO current                       | -   | 1.4    | -    | $\mu A$ |                                                                                                                   |



**Figure 26-23 WCO connection scheme<sup>[75]</sup>**

**Table 26-28 External clock input specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/conditions |
|---------|-----------|-------------|-----|-----|-----|-------|--------------------|
|---------|-----------|-------------|-----|-----|-----|-------|--------------------|

**Notes**

74. Mainly depends on the external crystal.

75. Refer to the family-specific Architecture TRM for more information on crystal requirements (002-24401, TRAVEO™ T2G Automotive MCU body controller high architecture technical reference manual).

**Table 26-28 External clock input specifications**

|        |           |                                |      |   |    |     |                                                                   |
|--------|-----------|--------------------------------|------|---|----|-----|-------------------------------------------------------------------|
| SID366 | $f_{EXT}$ | External clock input frequency | 0.25 | – | 80 | MHz | For EXT_CLK pin (all input level settings: CMOS, TTL, Automotive) |
| SID367 | EXT_DC    | External clock duty cycle      | 45   | – | 55 | %   |                                                                   |

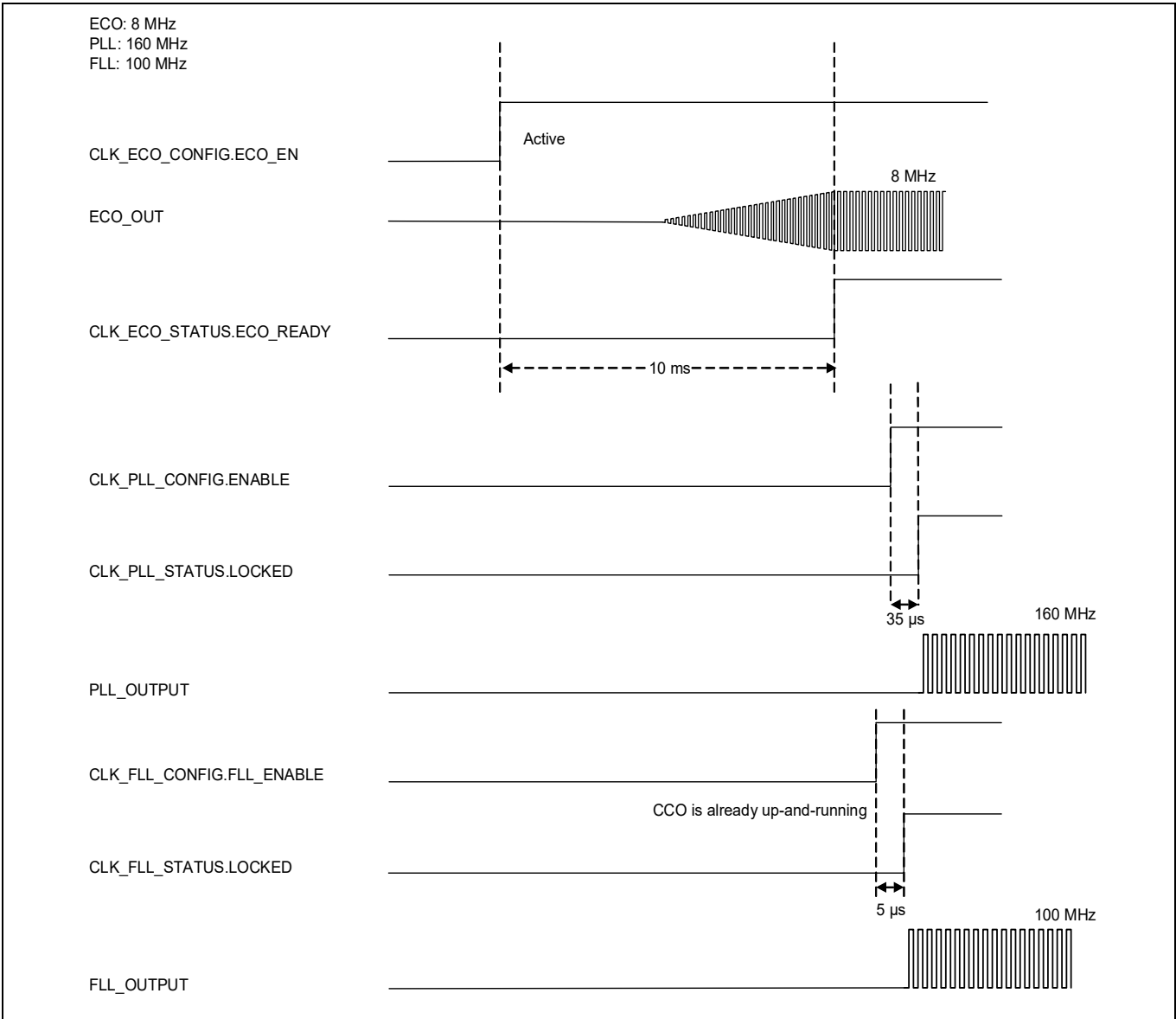
**Table 26-29 MCWDT timeout specifications**

| Spec ID | Parameter           | Description           | Min | Typ | Max  | Units | Details/conditions                                                                    |
|---------|---------------------|-----------------------|-----|-----|------|-------|---------------------------------------------------------------------------------------|
| SID410  | t <sub>MCWDT1</sub> | Minimum MCWDT timeout | 57  | –   | –    | μs    | When using the ILO (32.768 kHz + 7%) and 16-bit MCWDT counter<br>Guaranteed by design |
| SID411  | t <sub>MCWDT2</sub> | Maximum MCWDT timeout | –   | –   | 2.15 | s     | When using the ILO (32.768 kHz – 7%) and 16-bit MCWDT counter<br>Guaranteed by design |

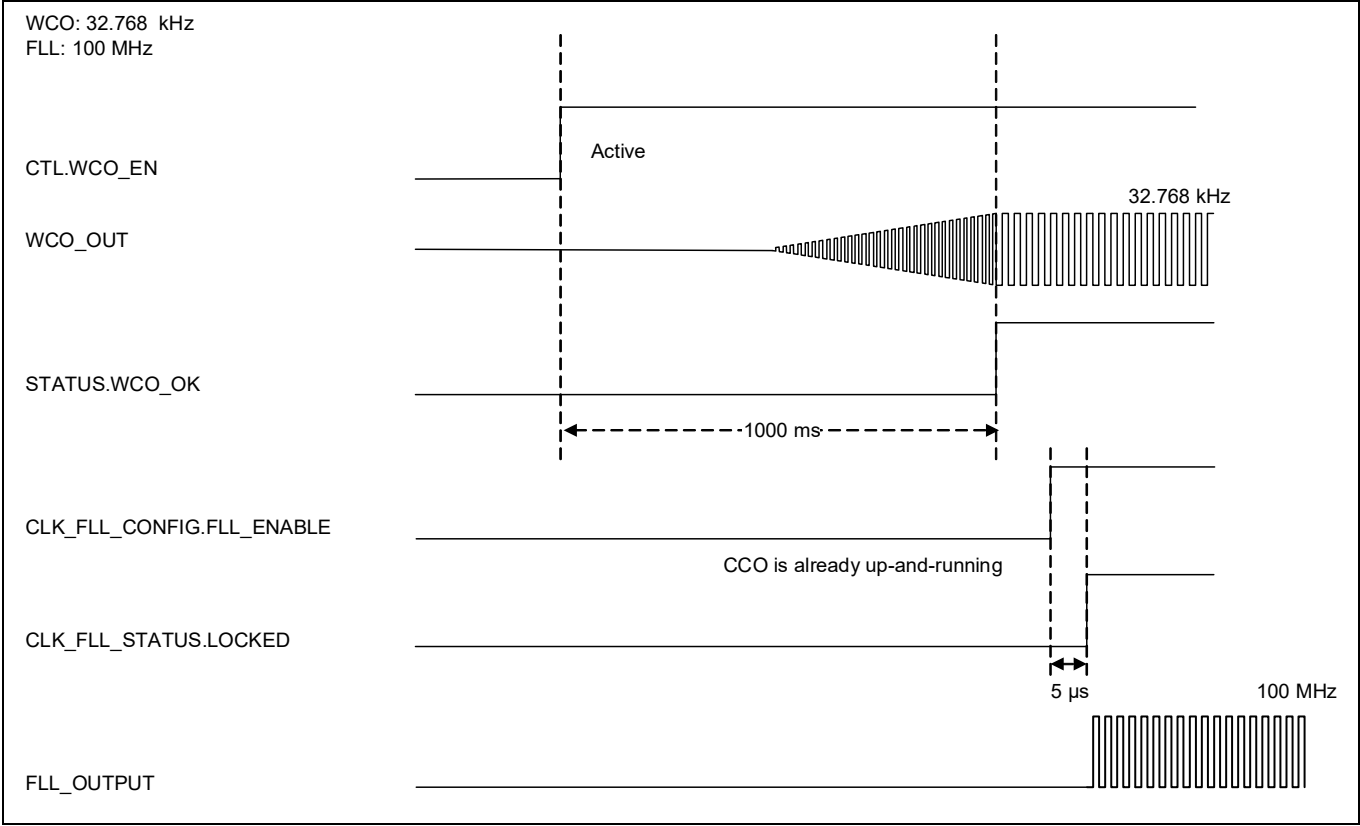
**Table 26-30 WDT timeout specifications**

| Spec ID | Parameter         | Description         | Min | Typ  | Max   | Units | Details/conditions                                                                           |
|---------|-------------------|---------------------|-----|------|-------|-------|----------------------------------------------------------------------------------------------|
| SID412  | t <sub>WDT1</sub> | Minimum WDT timeout | 57  | –    | –     | μs    | When using the ILO (32.768 kHz + 7%) and 32-bit WDT counter,<br>guaranteed by design         |
| SID413  | t <sub>WDT2</sub> | Maximum WDT timeout | –   | –    | 39.15 | h     | When using the ILO (32.768 kHz – 7%) and 32-bit WDT counter,<br>guaranteed by design         |
| SID414  | t <sub>WDT3</sub> | Default WDT timeout | –   | 1000 | –     | ms    | When using the ILO and 32-bit WDT counter at 0x8000 (default value),<br>guaranteed by design |

## 26.12 Clock timing diagrams



**Figure 26-24 ECO to PLL or FLL diagram**



**Figure 26-25 WCO to FLL diagram**

## 26.13 Ethernet specifications

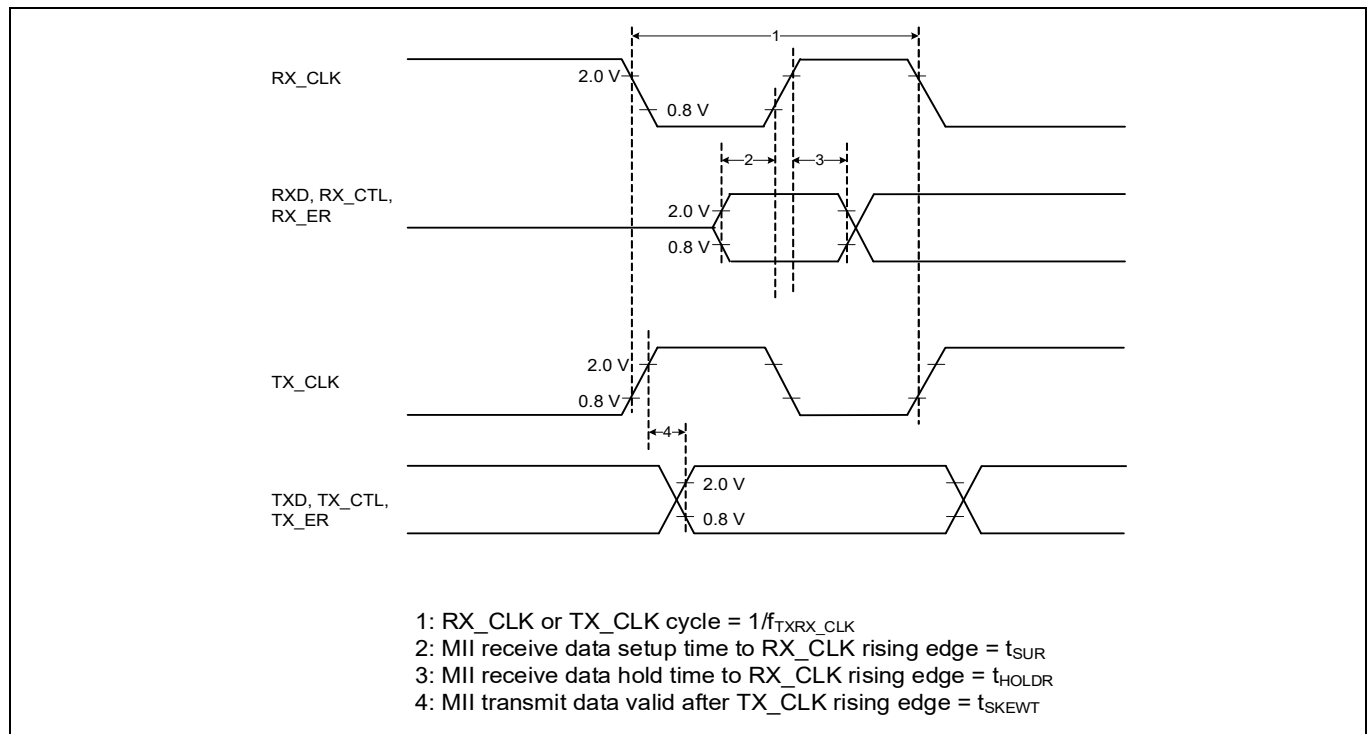
All specifications are valid for  $-40\text{ °C} \leq T_A \leq 125\text{ °C}$  and for 2.7 V to 5.5 V except where noted.

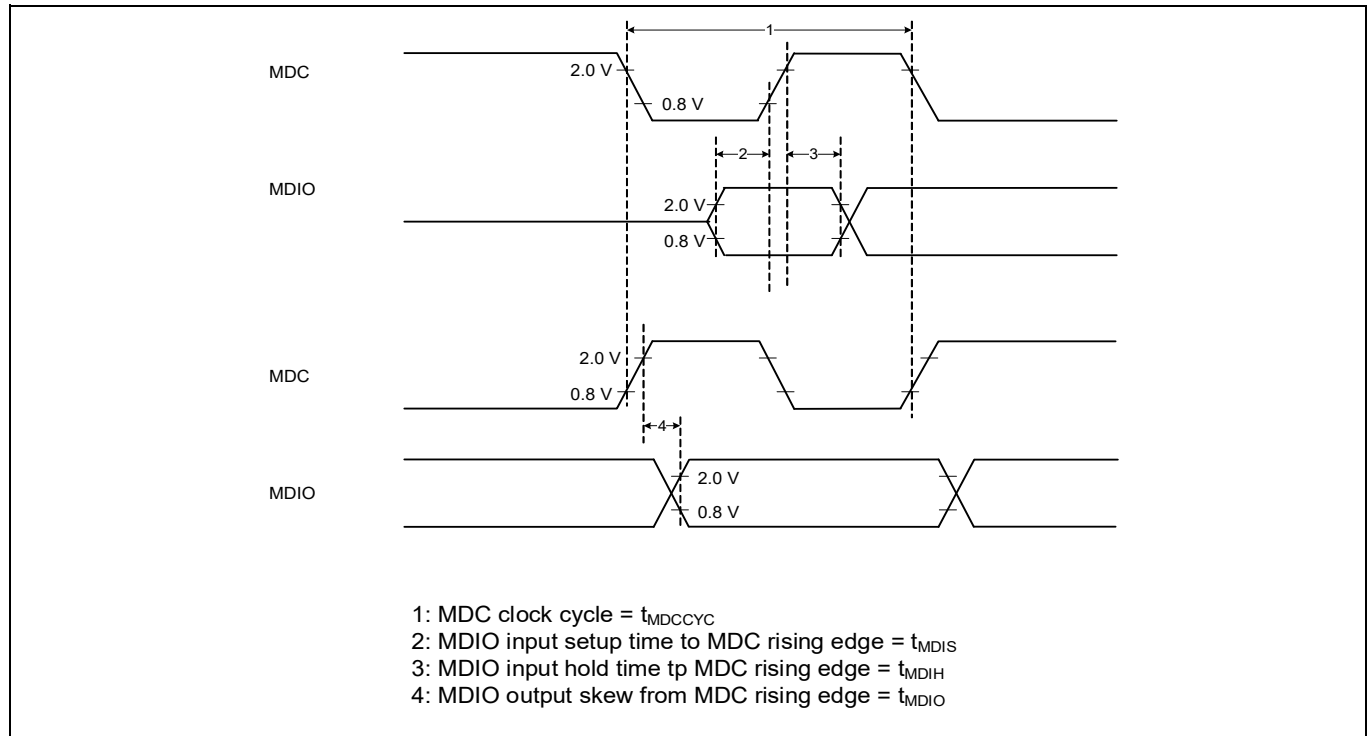
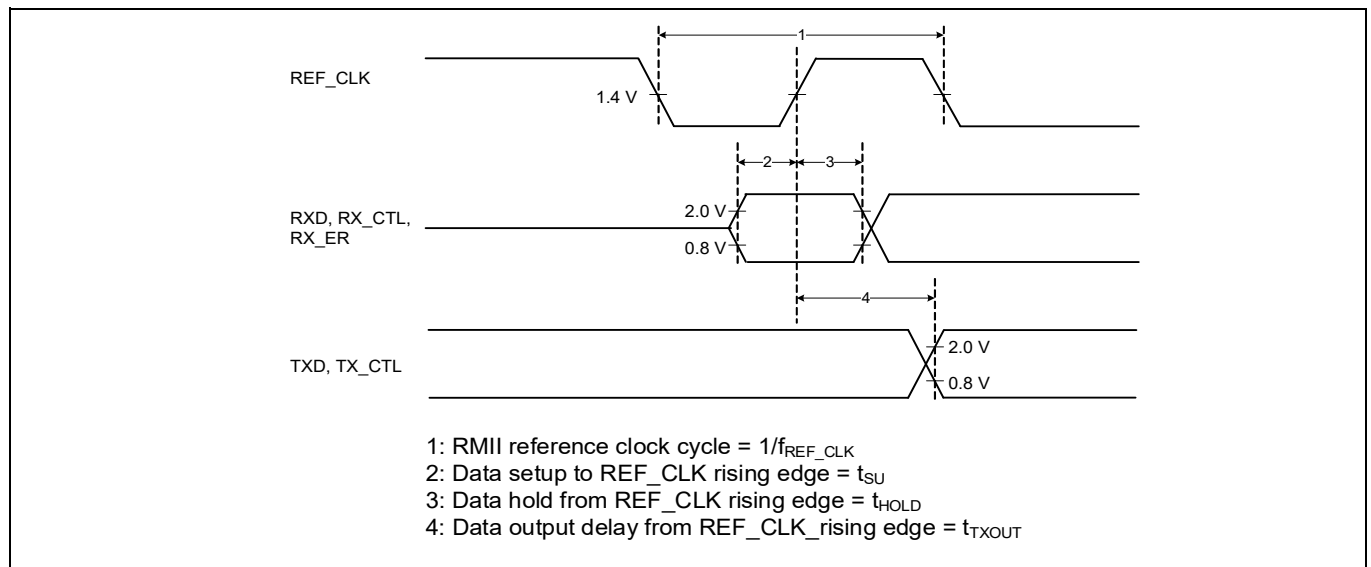
**Table 26-31 Ethernet specifications [Conditions: drive\_sel<1:0>= 00]**

| Spec ID                                          | Parameter             | Description                                                  | Min         | Typ | Max    | Units | Details/conditions                                              |
|--------------------------------------------------|-----------------------|--------------------------------------------------------------|-------------|-----|--------|-------|-----------------------------------------------------------------|
| <b>Ethernet general specifications</b>           |                       |                                                              |             |     |        |       |                                                                 |
| SID368                                           | f <sub>SYS</sub>      | System clock max frequency                                   | –           | –   | 100    | MHz   | Guaranteed by design                                            |
| SID369                                           | f <sub>AXI</sub>      | AXI clock max frequency                                      | –           | –   | 200    | MHz   | Guaranteed by design                                            |
| SID399                                           | V <sub>ETH</sub>      | Ethernet MAC I/O supply voltage                              | 3.0         | –   | 3.6    | V     | For V <sub>DDD</sub>                                            |
| SID364A                                          | C <sub>L_MD</sub>     | Load capacitance                                             | –           | –   | 25     | pF    | For MDIO all signals between MAC and PHY using GPIO_STD         |
| SID364A2                                         | C <sub>L_MG</sub>     | Load capacitance                                             | –           | –   | 15     | pF    | For MII and RMII all signals between MAC and PHY using GPIO_STD |
| SID365A                                          | t <sub>RF</sub>       | Rise / fall time (For input pins)                            | –           | –   | 2      | ns    | 20% to 80%, for MII and RMII using GPIO_STD                     |
| <b>Ethernet MII specifications for GPIO_STD</b>  |                       |                                                              |             |     |        |       |                                                                 |
| SID375                                           | f <sub>TXRX_CLK</sub> | MII TX/RX_CLK Clock frequency at 100 Mbps                    | –<br>100ppm | 25  | 100ppm | MHz   |                                                                 |
| SID376                                           | DUTY_TX-RX_CLK        | TX/RX Clock Duty cycle                                       | 35          | –   | 65     | %     |                                                                 |
| SID372                                           | t <sub>SKEWT</sub>    | MII Transmit data (TX_CTL, TXD, TX_ER) valid after TX_CLK    | 0.5         | –   | 25     | ns    |                                                                 |
| SID373                                           | t <sub>SUR</sub>      | MII Receive data setup to RX_CLK rising edge                 | 10          | –   | –      | ns    |                                                                 |
| SID374                                           | t <sub>HOLDR</sub>    | MII Receive data hold to RX_CLK rising edge                  | 10          | –   | –      | ns    |                                                                 |
| <b>Ethernet RMII specifications for GPIO_STD</b> |                       |                                                              |             |     |        |       |                                                                 |
| SID375A                                          | f <sub>REF_CLK</sub>  | RMII reference Clock frequency (input)                       | –50ppm      | 50  | 50ppm  | MHz   | External clock                                                  |
| SID376A                                          | DUTY_REF_CLK          | Duty cycle of reference clock (input)                        | 35          | –   | 65     | %     |                                                                 |
| SID377                                           | t <sub>SU</sub>       | RX_CTL, RXD[1:0], RX_ER Data Setup to REF_CLK rising edge    | 4           | –   | –      | ns    |                                                                 |
| SID378                                           | t <sub>HOLD</sub>     | RX_CTL, RXD[1:0], RX_ER, Data hold from REF_CLK rising edge  | 2           | –   | –      | ns    |                                                                 |
| SID393                                           | t <sub>TXOUT</sub>    | TX_CTL, TXD[1:0], Data output delay from REF_CLK rising edge | 2           | –   | 14.6   | ns    | For GPIO_STD                                                    |
| <b>Ethernet MDIO specifications for GPIO_STD</b> |                       |                                                              |             |     |        |       |                                                                 |
| SID395                                           | t <sub>MDCYC</sub>    | MDC clock cycle                                              | 400         | –   | –      | ns    |                                                                 |
| SID395A                                          | t <sub>HL_MDCYC</sub> | The minimum HIGH and LOW times for MDC                       | 160         | –   | –      | ns    |                                                                 |
| SID396                                           | t <sub>MDIS</sub>     | MDIO input setup time to MDC rising edge                     | 100         | –   | –      | ns    |                                                                 |

**Table 26-31 Ethernet specifications** *(continued)* [Conditions: drive\_sel<1:0>= 00]

| Spec ID | Parameter  | Description                             | Min | Typ | Max | Units | Details/conditions |
|---------|------------|-----------------------------------------|-----|-----|-----|-------|--------------------|
| SID397  | $t_{MDIH}$ | MDIO input hold time to MDC rising edge | 0   | –   | –   | ns    |                    |
| SID398  | $t_{MDIO}$ | MDIO output skew from MDC rising edge   | 10  | –   | 390 | ns    |                    |


**Figure 26-26 MII timing diagram**


**Figure 26-27 MDIO timing diagram**

**Figure 26-28 RMI timing diagram**

## 26.14 SDHC specifications

All specifications are valid for  $-40\text{ °C} \leq T_A \leq 125\text{ °C}$  and for 2.7 V to 5.5 V except where noted.

**Table 26-32 SDHC specifications**

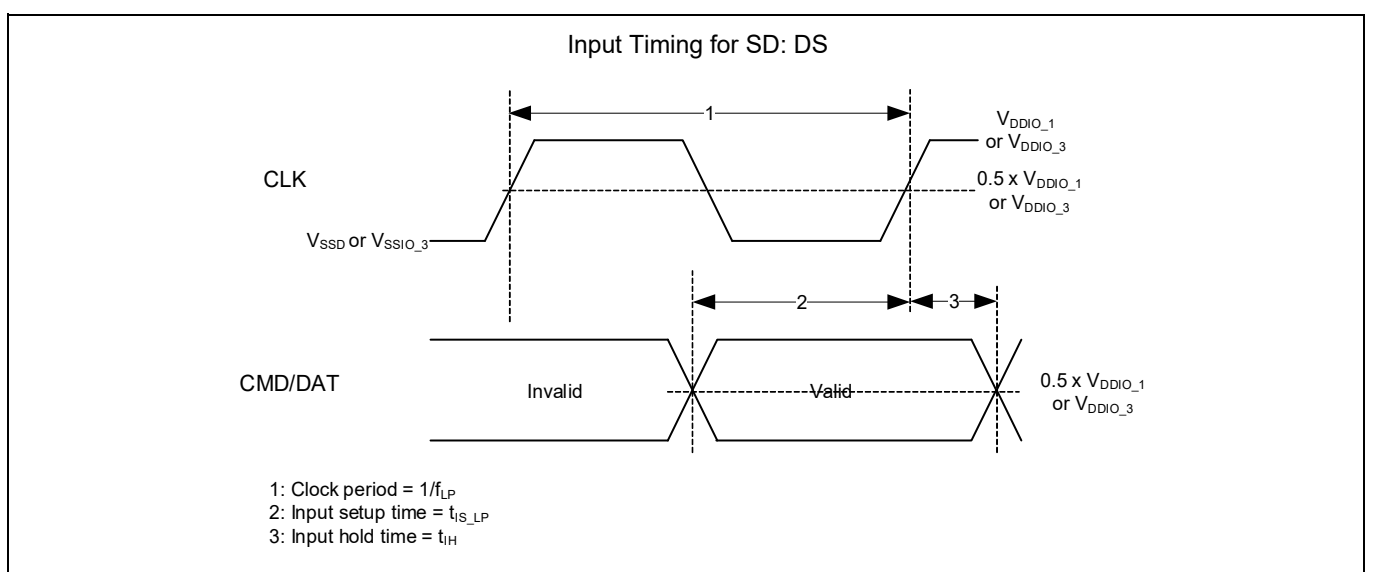
| Spec ID                                                                                          | Parameter                    | Description                               | Min | Typ | Max | Units | Details/conditions                             |
|--------------------------------------------------------------------------------------------------|------------------------------|-------------------------------------------|-----|-----|-----|-------|------------------------------------------------|
| <b>SDHC and eMMC specifications (the source clock must be divided by 2 or more in DDR modes)</b> |                              |                                           |     |     |     |       |                                                |
| SID801                                                                                           | V <sub>SDHC</sub>            | SDHC IO supply voltage                    | 2.7 | –   | 3.6 | V     | For V <sub>DDIO_1</sub> or V <sub>DDIO_3</sub> |
| SID802                                                                                           | I <sub>ODS</sub>             | I/O drive select                          | 8   | –   | 8   | mA    | drive_sel<1:0>= 0b00 for all modes             |
| SID803                                                                                           | t <sub>IT</sub>              | Input transition time                     | 0.7 | –   | 3   | ns    |                                                |
| <b>SD: DS timing specifications for GPIO_STD/HSIO_STD</b>                                        |                              |                                           |     |     |     |       |                                                |
| SID810                                                                                           | f <sub>LP</sub>              | Interface clock period                    | –   | –   | 25  | MHz   | 40-ns period                                   |
| SID812                                                                                           | C <sub>D</sub>               | I/O loading at DATA/CMD pins              | 40  | –   | 40  | pF    |                                                |
| SID813                                                                                           | C <sub>C</sub>               | I/O loading at CLK pins                   | 40  | –   | 40  | pF    |                                                |
| SID814                                                                                           | t <sub>OS</sub>              | Output setup time of CMD/DAT prior to CLK | 5.5 | –   | –   | ns    |                                                |
| SID815                                                                                           | t <sub>OH</sub>              | Output hold time of CMD/DAT after CLK     | 5.5 | –   | –   | ns    |                                                |
| SID816                                                                                           | t <sub>IS_LP</sub>           | Input setup time of CMD/DAT prior to CLK  | 24  | –   | –   | ns    | Clock period - Output delay                    |
| SID818                                                                                           | t <sub>IH</sub>              | Input hold time of CMD/DAT after CLK      | 0   | –   | –   | ns    |                                                |
| <b>SD: HS timing specifications for GPIO_STD/HSIO_STD</b>                                        |                              |                                           |     |     |     |       |                                                |
| SID820                                                                                           | f <sub>LP_SD_HS</sub>        | Interface clock period                    | –   | –   | 50  | MHz   | 20-ns period                                   |
| SID822                                                                                           | C <sub>D_SD_HS</sub>         | I/O loading at DATA/CMD pins              | 40  | –   | 40  | pF    |                                                |
| SID823                                                                                           | C <sub>C_SD_HS</sub>         | I/O loading at CLK pins                   | 40  | –   | 40  | pF    |                                                |
| SID824                                                                                           | t <sub>OS_SD_HS</sub>        | Output setup time of CMD/DAT prior to CLK | 6.5 | –   | –   | ns    |                                                |
| SID825                                                                                           | t <sub>OH_SD_HS</sub>        | Output hold time of CMD/DAT after CLK     | 2.5 | –   | –   | ns    |                                                |
| SID826                                                                                           | t <sub>IS_LP_SD_HS</sub>     | Input setup time of CMD/DAT prior to CLK  | 4   | –   | –   | ns    | Clock period less output delay                 |
| SID828                                                                                           | t <sub>IH_SD_HS</sub>        | Input hold time of CMD/DAT after CLK      | 2.5 | –   | –   | ns    |                                                |
| <b>eMMC: BWC timing specifications for GPIO_STD/HSIO_STD</b>                                     |                              |                                           |     |     |     |       |                                                |
| SID870                                                                                           | f <sub>LP_eMMC_BWC</sub>     | Interface clock period                    | –   | –   | 26  | MHz   | 38.4-ns period                                 |
| SID872                                                                                           | C <sub>D_eMMC_BWC</sub>      | I/O loading at DATA/CMD pins              | 30  | –   | 30  | pF    |                                                |
| SID873                                                                                           | C <sub>C_eMMC_BWC</sub>      | I/O loading at CLK pins                   | 30  | –   | 30  | pF    |                                                |
| SID874                                                                                           | t <sub>OS_eM-MC_BWC</sub>    | Output setup time of CMD/DAT prior to CLK | 3.5 | –   | –   | ns    |                                                |
| SID875                                                                                           | t <sub>OH_eM-MC_BWC</sub>    | Output hold time of CMD/DAT after CLK     | 3.5 | –   | –   | ns    |                                                |
| SID876                                                                                           | t <sub>IS_LP_eM-MC_BWC</sub> | Input setup time of CMD/DAT prior to CLK  | 9.7 | –   | –   | ns    | Clock period less output delay                 |
| SID878                                                                                           | t <sub>IH_eMMC_BWC</sub>     | Input hold time of CMD/DAT after CLK      | 8.3 | –   | –   | ns    |                                                |
| <b>eMMC: SDR timing specifications for HSIO_STD</b>                                              |                              |                                           |     |     |     |       |                                                |

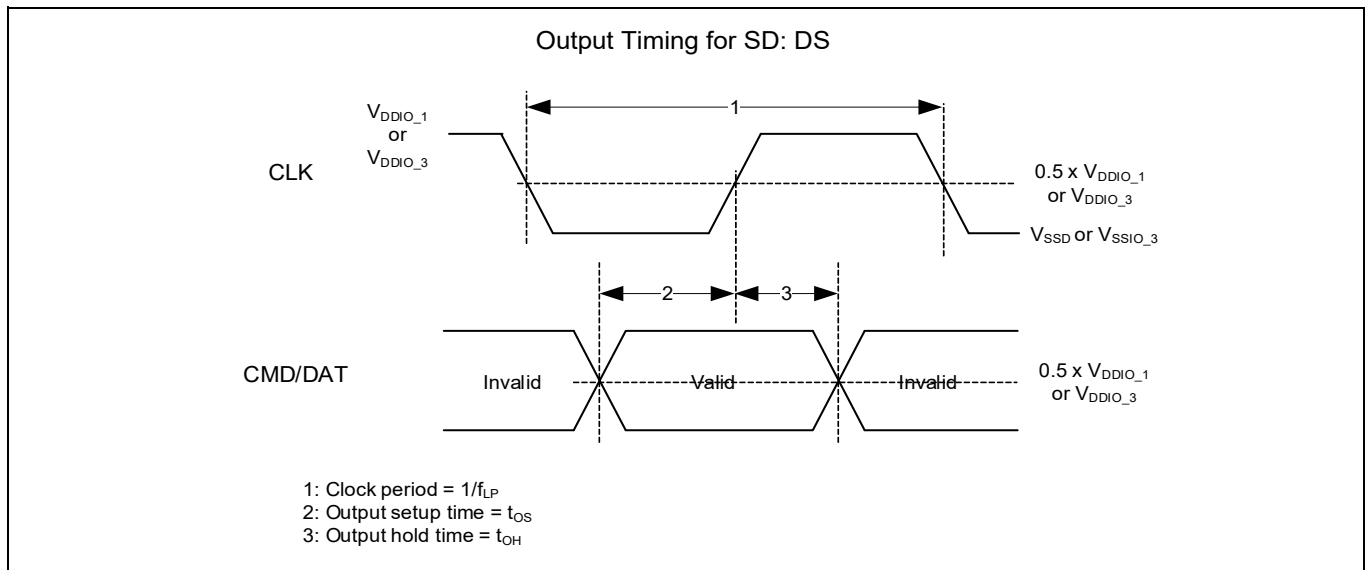
**Table 26-32 SDHC specifications** (continued)

| Spec ID | Parameter               | Description                               | Min | Typ | Max | Units | Details/conditions             |
|---------|-------------------------|-------------------------------------------|-----|-----|-----|-------|--------------------------------|
| SID880  | $f_{LP\_eMMC\_SDR}$     | Interface clock period                    | –   | –   | 52  | MHz   | 19.2-ns period                 |
| SID882  | $C_{D\_eMMC\_SDR}$      | I/O loading at DATA/CMD pins              | 30  | –   | 30  | pF    |                                |
| SID883  | $C_{C\_eMMC\_SDR}$      | I/O loading at CLK pins                   | 30  | –   | 30  | pF    |                                |
| SID884  | $t_{OS\_eMMC\_SDR}$     | Output setup time of CMD/DAT prior to CLK | 3.5 | –   | –   | ns    |                                |
| SID885  | $t_{OH\_eMMC\_SDR}$     | Output hold time of CMD/DAT after CLK     | 3.5 | –   | –   | ns    |                                |
| SID886  | $t_{IS\_LP\_eMMC\_SDR}$ | Input setup time of CMD/DAT prior to CLK  | 3.5 | –   | –   | ns    | Clock period less output delay |
| SID888  | $t_{IH\_eMMC\_SDR}$     | Input hold time of CMD/DAT after CLK      | 2.5 | –   | –   | ns    |                                |

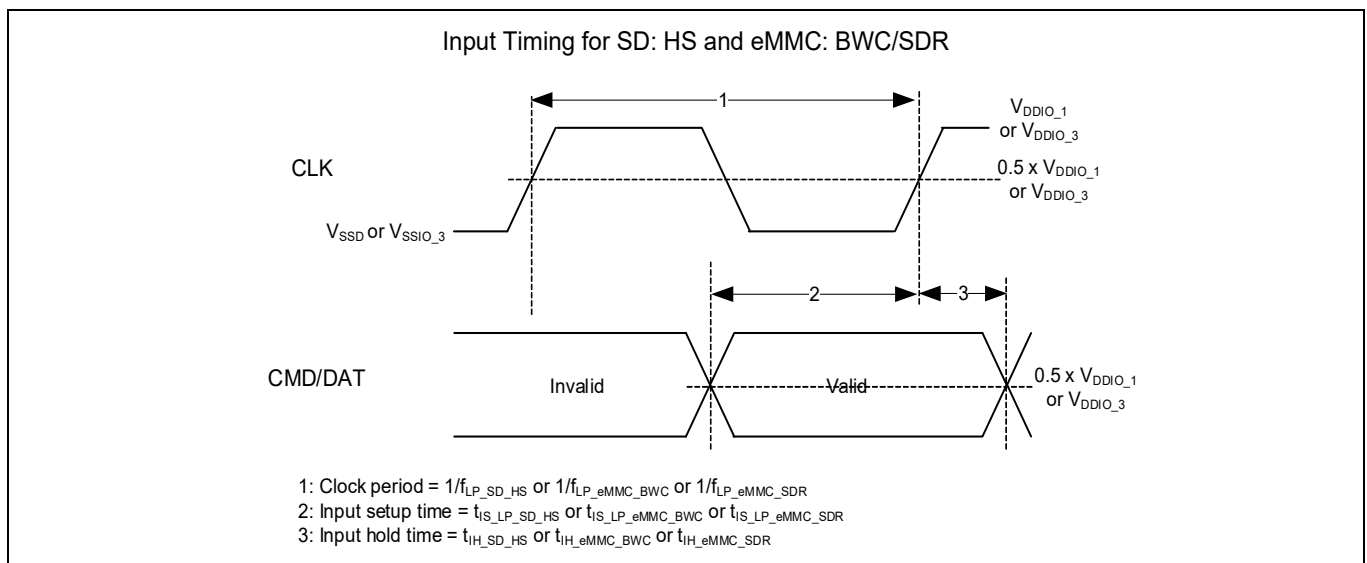
**eMMC: DDR timing specifications for HSIO\_STD**

|        |                         |                                           |     |   |    |     |                                |
|--------|-------------------------|-------------------------------------------|-----|---|----|-----|--------------------------------|
| SID890 | $f_{LP\_eMMC\_DDR}$     | Interface clock period                    | –   | – | 52 | MHz | 19.2-ns period                 |
| SID892 | DUTY_-CLK_eMMC_DDR      | Duty cycle of output CLK                  | 45  | – | 55 | %   |                                |
| SID893 | $C_{D\_eMMC\_DDR}$      | I/O loading at DATA/CMD pins              | 20  | – | 20 | pF  |                                |
| SID894 | $C_{C\_eMMC\_DDR}$      | I/O loading at CLK pins                   | 20  | – | 20 | pF  |                                |
| SID895 | $t_{OS\_eMMC\_DDR}$     | Output setup time of CMD/DAT prior to CLK | 2.6 | – | –  | ns  |                                |
| SID896 | $t_{OH\_eMMC\_DDR}$     | Output hold time of CMD/DAT after CLK     | 2.6 | – | –  | ns  |                                |
| SID897 | $t_{IS\_LP\_eMMC\_DDR}$ | Input setup time of CMD/DAT prior to CLK  | 2.4 | – | –  | ns  | Clock period less output delay |
| SID899 | $t_{IH\_eMMC\_DDR}$     | Input hold time of CMD/DAT after CLK      | 1.5 | – | –  | ns  |                                |

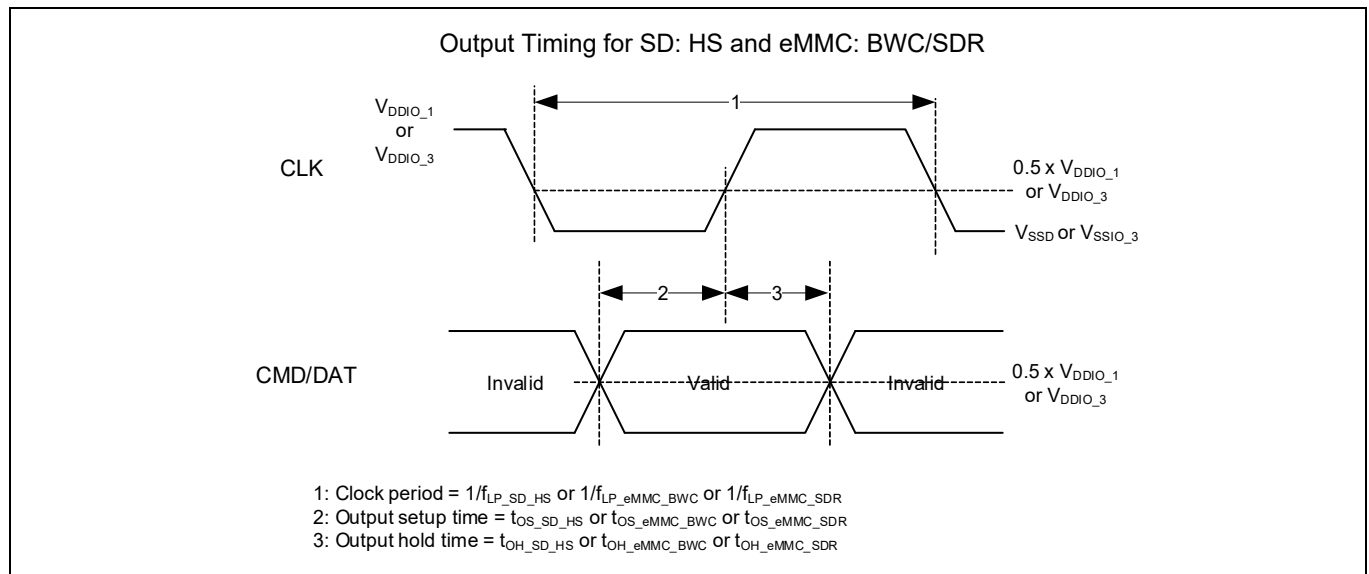

**Figure 26-29 SD default speed input timing**



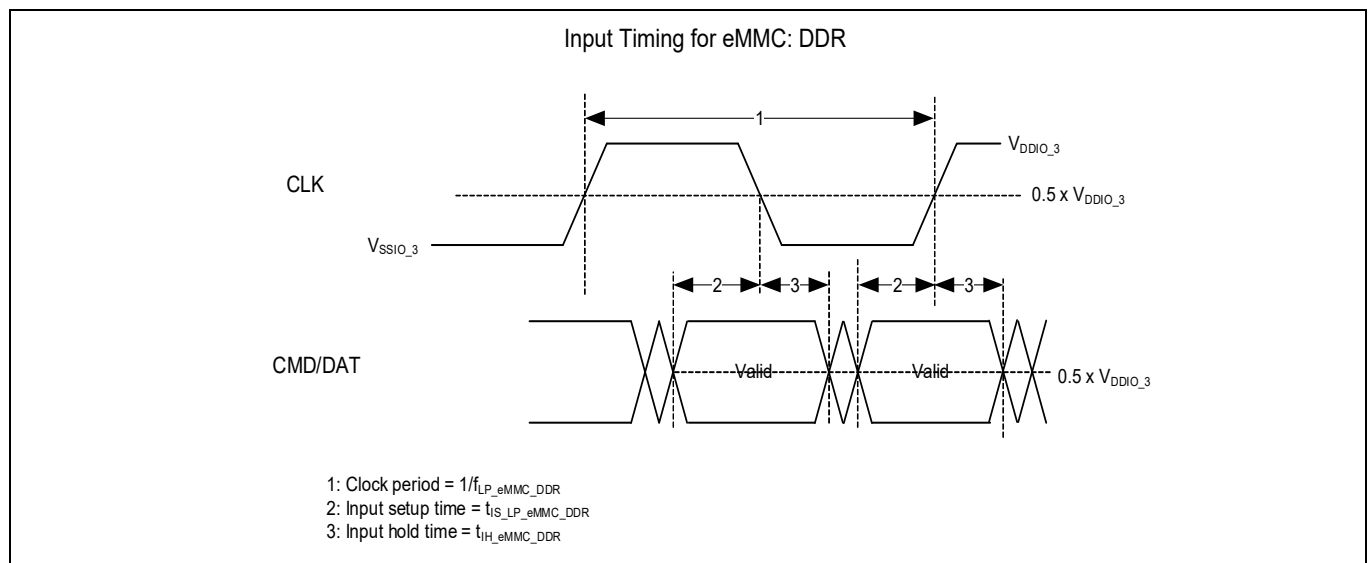
**Figure 26-30 SD default speed output timing**



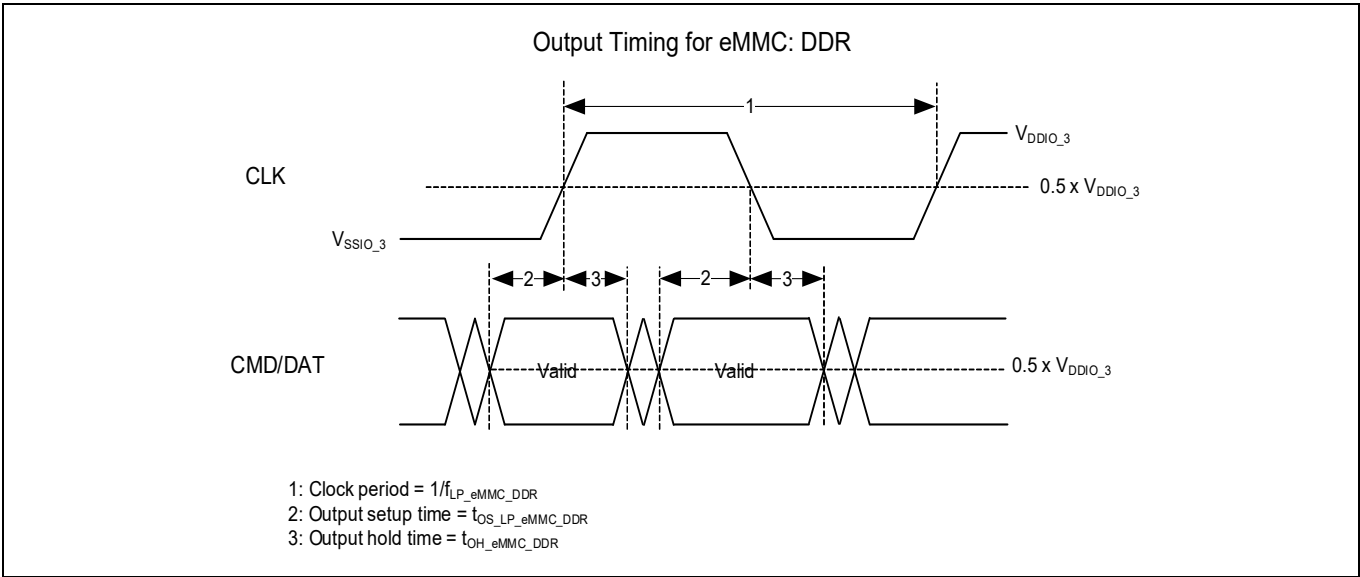
**Figure 26-31 SD high speed and eMMC BWC/SDR input timing**



**Figure 26-32 SD high speed and eMMC BWC/SDR output timing**



**Figure 26-33 eMMC DDR input timing**



**Figure 26-34 eMMC DDR output timing**

## 26.15 Audio subsystem specifications

All specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$  and for 2.7 V to 5.5 V except where noted.

**Table 26-33 Audio subsystem specifications**

| Spec ID | Parameter               | Description                               | Min                            | Typ | Max                            | Units | Details/conditions                            |
|---------|-------------------------|-------------------------------------------|--------------------------------|-----|--------------------------------|-------|-----------------------------------------------|
| SID770  | $f_{\text{AUDIO}}$      | Audio subsystem frequency                 | –                              | –   | 200                            | MHz   | Guaranteed by design                          |
| SID772  | $V_{\text{AUDIO}}$      | Audio subsystem I/O supply voltage        | 3.0                            | –   | 3.6                            | V     | For $V_{\text{DDIO}_2}$                       |
| SID773  | $V_{\text{OL}_A}$       | Output voltage LOW level                  | –                              | –   | 0.4                            | V     | drive_sel<1:0>= 0b0X, Pull-up, pull-down: off |
| SID774  | $V_{\text{OH}_A}$       | Output voltage HIGH level                 | $V_{\text{DDIO}_2} - 0.5$      | –   | –                              | V     | drive_sel<1:0>= 0b0X, Pull-up, pull-down: off |
| SID775  | $V_{\text{IH\_CMOS}_A}$ | Input voltage HIGH threshold in CMOS mode | $0.7 \times V_{\text{DDIO}_2}$ | –   | –                              | V     |                                               |
| SID776  | $V_{\text{IL\_CMOS}_A}$ | Input Voltage LOW threshold in CMOS mode  | –                              | –   | $0.3 \times V_{\text{DDIO}_2}$ | V     |                                               |

### I<sup>2</sup>S/TDM Word Clock Frequency

|        |                      |                                        |   |   |     |     |                      |
|--------|----------------------|----------------------------------------|---|---|-----|-----|----------------------|
| SID796 | $f_{\text{WS\_I2S}}$ | WS Clock Rate in I <sup>2</sup> S mode | 8 | – | 192 | kHz | Guaranteed by design |
| SID797 | $f_{\text{WS\_TDM}}$ | WS Clock Rate in TDM mode              | – | – | 96  | kHz | Guaranteed by design |
| SID798 | Word                 | Length of I <sup>2</sup> S Word        | 8 | – | 32  | bit | Guaranteed by design |

### I<sup>2</sup>S/TDM Master Mode

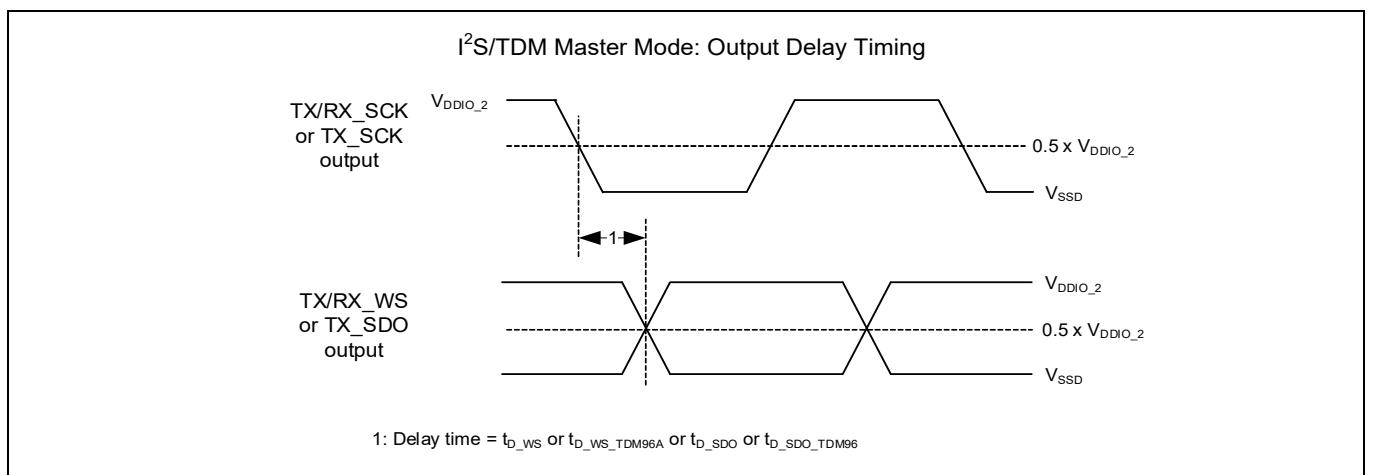
|         |                            |                                                                                           |                            |   |    |    |                                                                                                                                 |
|---------|----------------------------|-------------------------------------------------------------------------------------------|----------------------------|---|----|----|---------------------------------------------------------------------------------------------------------------------------------|
| SID740  | $t_{\text{D\_WS}}$         | Delay Time of TX/RX_WS Output Transition from Falling Edge of TX/RX_SCK Output            | –8                         | – | 9  | ns | Except TDM 96 kHz mode, TX/RX_WS output and TX/RX_SCK output with drive_sel<1:0>= 0b01, guaranteed by design                    |
| SID740A | $t_{\text{D\_WS\_TDM96A}}$ | Delay Time of TX/RX_WS output Transition from Falling Edge of TX/RX_SCK output            | –8                         | – | 11 | ns | TDM 96 kHz mode, TX/RX_WS output with drive_sel<1:0>= 0b01 and TX/RX_SCK output with drive_sel<1:0>= 0b00, guaranteed by design |
| SID741  | $t_{\text{D\_SDO}}$        | Delay Time of TX_SDO Transition from Falling Edge of TX_SCK Output                        | –8                         | – | 8  | ns | TX_SDO and TX_SCK output with drive_sel<1:0>= 0b01 for except TDM 96 kHz mode, guaranteed by design                             |
| SID741A | $t_{\text{D\_SDO\_TDM96}}$ | Delay Time of TX_SDO Transition from Falling Edge of TX_SCK Output                        | –8                         | – | 8  | ns | TX_SDO with drive_sel<1:0>= 0b01 and TX_SCK output with drive_sel<1:0>= 0b00 for TDM 96 kHz mode, guaranteed by design          |
| SID742  | $t_{\text{S\_SDI}}$        | RX_SDI Setup Time to the Following Rising Edge of RX_SCK Output (RX_CTL.B_CLOCK_INV = 0)  | 11                         | – | –  | ns | RX_SCK output with drive_sel<1:0>= 0b00, guaranteed by design                                                                   |
| SID743  | $t_{\text{H\_SDI}}$        | RX_SDI Hold Time to the Rising Edge of RX_SCK Output (RX_CTL.B_CLOCK_INV = 0)             | $t_{\text{MCLK\_S}} - 0.9$ | – | –  | ns | RX_SCK output with drive_sel<1:0>= 0b00, guaranteed by design                                                                   |
| SID744  | $t_{\text{S\_SDI1}}$       | RX_SDI Setup Time to the Following Falling Edge of RX_SCK Output (RX_CTL.B_CLOCK_INV = 1) | 11                         | – | –  | ns | RX_SCK output with drive_sel<1:0>= 0b00, guaranteed by design                                                                   |
| SID745  | $t_{\text{H\_SDI1}}$       | RX_SDI Hold Time to the Falling Edge of RX_SCK Output (RX_CTL.B_CLOCK_INV = 1)            | $t_{\text{MCLK\_S}} - 0.9$ | – | –  | ns | RX_SCK output with drive_sel<1:0>= 0b00, guaranteed by design                                                                   |

**Table 26-33 Audio subsystem specifications (continued)**

| Spec ID | Parameter          | Description                           | Min   | Typ | Max     | Units | Details/conditions                                             |
|---------|--------------------|---------------------------------------|-------|-----|---------|-------|----------------------------------------------------------------|
| SID746  | $t_{SCKCY}$        | TX/RX_SCK Output Bit Clock Duty Cycle | 45    | –   | 55      | %     | Guaranteed by design                                           |
| SID748  | $f_{MCLK\_SOC}$    | MCLK input clock frequency            | 1.024 | –   | 196.608 | MHz   | Internal Fractional PLL, guaranteed by design                  |
| SID748A | $f_{MCLK\_SOC\_E}$ | MCLK input clock frequency            | 1.024 | –   | 98.304  | MHz   | External clock                                                 |
| SID749  | $t_{MCLK\_SOC}$    | MCLK input clock period               | 5.086 | –   | 976.563 | ns    | Guaranteed by design                                           |
| SID750  | $t_{JITTER}$       | MCLK Input clock jitter tolerance     | –200  | –   | 200     | ps    | Guaranteed by design                                           |
| SID748B | $f_{MCLK}$         | MCLK output clock frequency           | 1.024 | –   | 25      | MHz   | MCLK output with drive_sel<1:0> = 0b00<br>Guaranteed by design |
| SID748C | $f_{MCLK1}$        | MCLK output clock frequency           | 1.024 | –   | 15      | MHz   | MCLK output with drive_sel<1:0> = 0b01<br>Guaranteed by design |
| SID749B | $f_{MCLK\_DT}$     | MCLK output clock duty                | 45    | –   | 55      | %     | Guaranteed by design                                           |

**I<sup>2</sup>S/TDM Slave Mode**

|        |               |                                                                                            |                       |   |                      |    |                                                         |
|--------|---------------|--------------------------------------------------------------------------------------------|-----------------------|---|----------------------|----|---------------------------------------------------------|
| SID751 | $t_{S\_WS}$   | TX/RX_WS Input Alignment Clock Setup Time to the following Rising Edge of TX/RX_SCK Input  | 5                     | – | –                    | ns | Guaranteed by design                                    |
| SID752 | $t_{H\_WS}$   | TX/RX_WS Input Alignment Clock Hold Time to the Rising Edge of TX/RX_SCK Input             | $t_{MCLK\_SOC} + 5.0$ | – | –                    | ns | Guaranteed by design                                    |
| SID753 | $t_{D\_SDO}$  | Delay Time of TX_SDO Transition from Falling Edge of TX_SCK Input (TX_CTL.B_CLOCK_INV = 0) | $t_{MCLK\_SOC} + 5.0$ | – | $t_{MCLK\_SOC} + 15$ | ns | TX_SDO with drive_sel<1:0> = 0b00, guaranteed by design |
| SID754 | $t_{D\_SDO1}$ | Delay Time of TX_SDO Transition from Rising Edge of TX_SCK Input (TX_CTL.B_CLOCK_INV = 1)  | $t_{MCLK\_SOC} + 5.0$ | – | $t_{MCLK\_SOC} + 15$ | ns | TX_SDO with drive_sel<1:0> = 0b00, guaranteed by design |
| SID755 | $t_{S\_SDI}$  | RX_SDI Setup Time to the Following Rising Edge of RX_SCK Input                             | 5                     | – | –                    | ns | Guaranteed by design                                    |
| SID756 | $t_{H\_SDI}$  | RX_SDI Hold Time to the Rising Edge of RX_SCK Input                                        | $t_{MCLK\_SOC} + 5.0$ | – | –                    | ns | Guaranteed by design                                    |
| SID757 | $t_{SCKCY}$   | TX/RX_SCK Input Bit Clock Duty Cycle                                                       | 45                    | – | 55                   | %  | Guaranteed by design                                    |


**Figure 26-35 Master output delay**

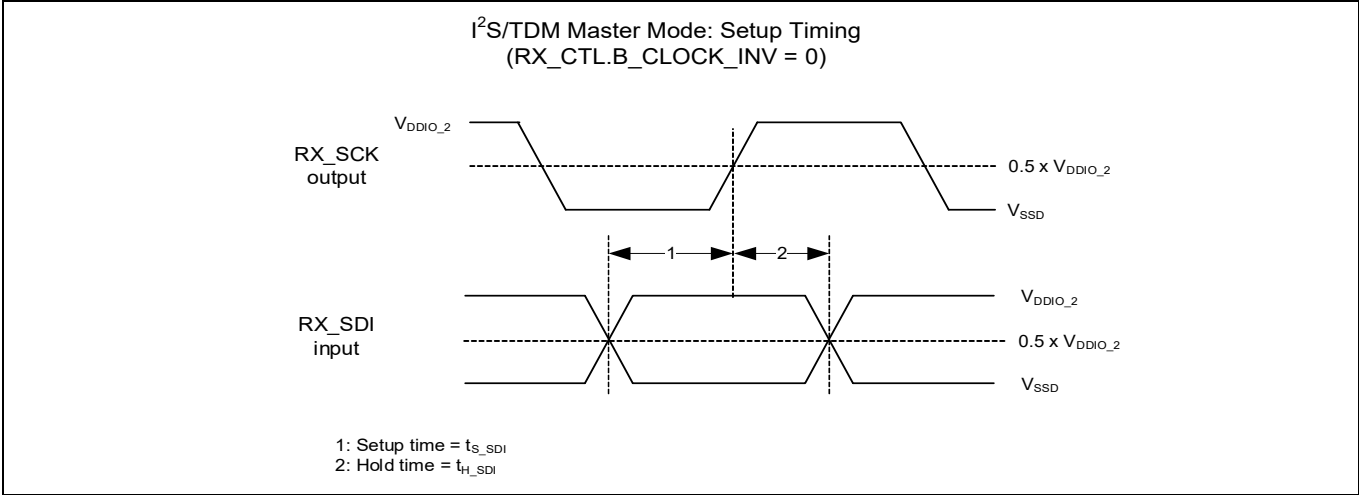


Figure 26-36 Master setup without clock inversion

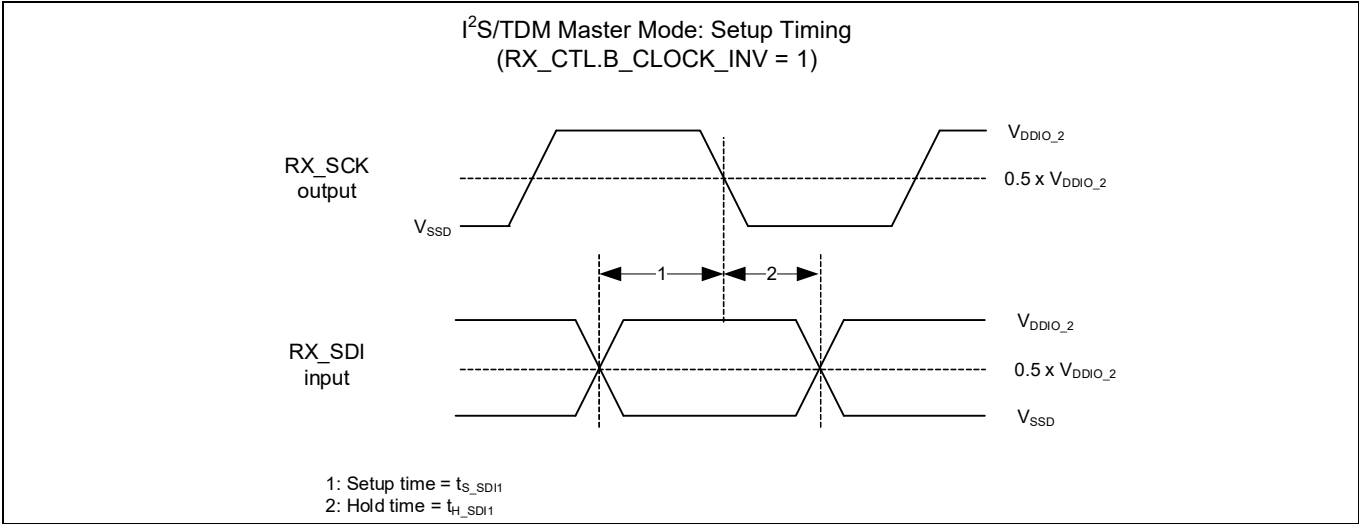
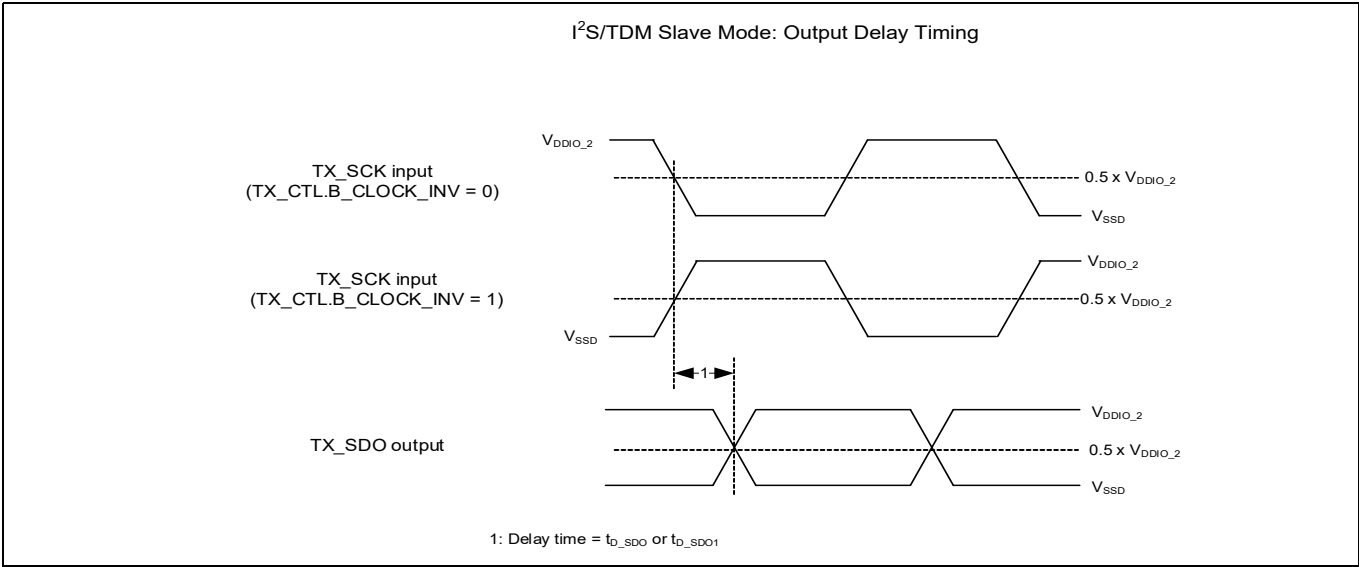
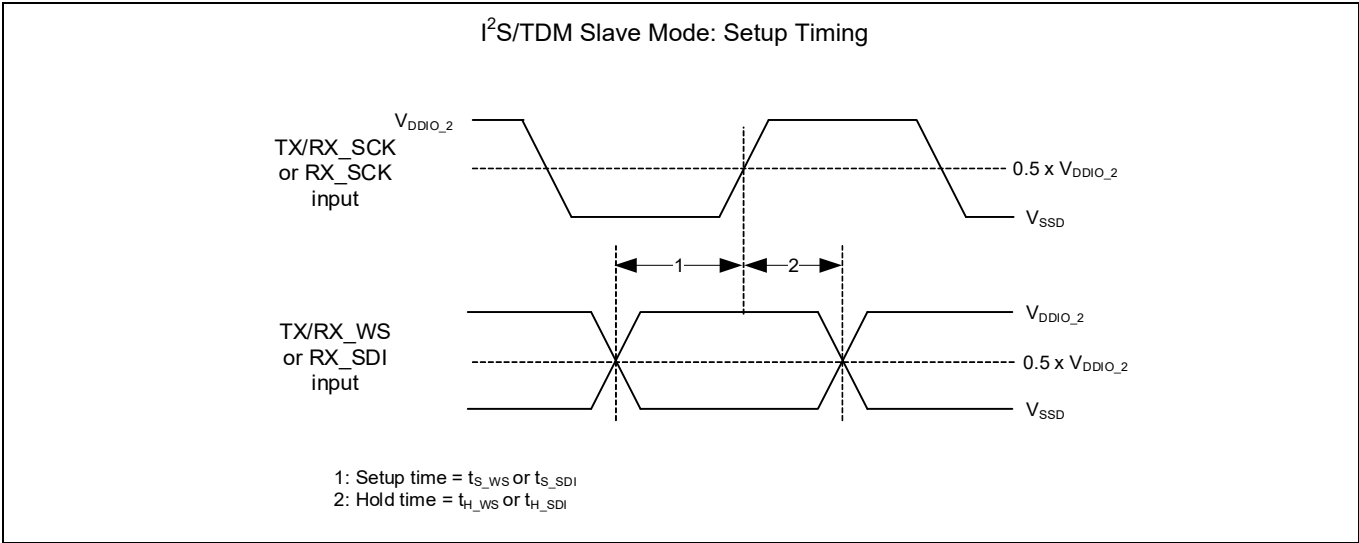


Figure 26-37 Master setup with clock inversion



**Figure 26-38 Slave output delay**



**Figure 26-39 Slave setup**

## 26.16 Serial memory interface specifications

All specifications are valid for  $-40\text{ °C} \leq T_A \leq 125\text{ °C}$  and for 2.7 V to 5.5 V except where noted.

**Table 26-34 SMIF specifications [Conditions: drive\_sel<1:0>= 00]**

| Spec ID                                           | Parameter                     | Description                                 | Min                          | Typ | Max  | Units | Details/conditions                             |
|---------------------------------------------------|-------------------------------|---------------------------------------------|------------------------------|-----|------|-------|------------------------------------------------|
| <b>SMIF DC Specification</b>                      |                               |                                             |                              |     |      |       |                                                |
| SID785                                            | V <sub>SMIF</sub>             | SMIF I/O supply voltage                     | 2.7                          | –   | 3.6  | V     | For V <sub>DDIO_1</sub> or V <sub>DDIO_3</sub> |
| <b>SMIF HSSPI(SDR) Specification for HSIO_STD</b> |                               |                                             |                              |     |      |       |                                                |
| SID760                                            | C <sub>L_SDR_HSIO</sub>       | Load capacitance                            | –                            | –   | 30   | pF    |                                                |
| SID761                                            | SR <sub>SDR_HSIO</sub>        | Input rise and fall slew rates              | 1.5                          | –   | –    | V/ns  | Guaranteed by design                           |
| SID762                                            | f <sub>CK_SDR_HSIO</sub>      | Clock frequency                             | –                            | –   | 100  | MHz   |                                                |
| SID763                                            | t <sub>CK_SDR_HSIO</sub>      | Clock period                                | 1 / f <sub>CK_SDR_HSIO</sub> | –   | –    | ns    |                                                |
| SID764                                            | DCK <sub>SDR_HSIO</sub>       | Clock duty                                  | 45                           | –   | 55   | %     |                                                |
| SID765                                            | CSR <sub>SDR_HSIO</sub>       | Clock rise and fall slew rates              | 1.5                          | –   | –    | V/ns  |                                                |
| SID766                                            | t <sub>CS_SDR_HSIO</sub>      | Chip select HIGH time                       | 10                           | –   | –    | ns    |                                                |
| SID767                                            | t <sub>CSS_SDR_HSIO</sub>     | Chip select active setup time               | 3                            | –   | –    | ns    |                                                |
| SID768                                            | t <sub>CSH_SDR_HSIO</sub>     | Chip select active hold time                | 5                            | –   | –    | ns    |                                                |
| SID769                                            | t <sub>SU_SDR_HSIO</sub>      | Data setup time                             | 1.5                          | –   | –    | ns    |                                                |
| SID780                                            | t <sub>HD_SDR_HSIO</sub>      | Data hold time                              | 2                            | –   | –    | ns    |                                                |
| SID781                                            | t <sub>V_SDR_HSIO</sub>       | Clock LOW output valid                      | 1.5                          | –   | 7.65 | ns    |                                                |
| SID782                                            | t <sub>HO_SDR_HSIO</sub>      | Input hold time                             | 2                            | –   | –    | ns    |                                                |
| SID783                                            | t <sub>DIS_SDR_HSIO</sub>     | Input disable time                          | 0                            | –   | 7.5  | ns    |                                                |
| SID784                                            | t <sub>IO_SKEW_SDR_HSIO</sub> | Data skew (first data bit to last data bit) | –                            | –   | 0.6  | ns    | Guaranteed by design                           |
| <b>SMIF HSSPI(SDR) Specification for GPIO_STD</b> |                               |                                             |                              |     |      |       |                                                |
| SID760A                                           | C <sub>L_SDR_GPIO</sub>       | Load capacitance                            | –                            | –   | 30   | pF    |                                                |
| SID761A                                           | SR <sub>SDR_GPIO</sub>        | Input rise and fall slew rates              | 1                            | –   | –    | V/ns  | Guaranteed by design                           |
| SID762A                                           | f <sub>CK_SDR_GPIO</sub>      | Clock frequency                             | –                            | –   | 32   | MHz   |                                                |
| SID763A                                           | t <sub>CK_SDR_GPIO</sub>      | Clock period                                | 1 / f <sub>CK_SDR_GPIO</sub> | –   | –    | ns    |                                                |
| SID764A                                           | DCK <sub>SDR_GPIO</sub>       | Clock duty                                  | 45                           | –   | 55   | %     |                                                |
| SID765A                                           | CSR <sub>SDR_GPIO</sub>       | Clock rise and fall slew rates              | 1                            | –   | –    | V/ns  |                                                |
| SID766A                                           | t <sub>CS_SDR_GPIO</sub>      | Chip select HIGH time                       | 30                           | –   | –    | ns    |                                                |
| SID767A                                           | t <sub>CSS_SDR_GPIO</sub>     | Chip select active setup time               | 9                            | –   | –    | ns    |                                                |
| SID768A                                           | t <sub>CSH_SDR_GPIO</sub>     | Chip select active hold time                | 15                           | –   | –    | ns    |                                                |
| SID769A                                           | t <sub>SU_SDR_GPIO</sub>      | Data setup time                             | 4.5                          | –   | –    | ns    |                                                |
| SID780A                                           | t <sub>HD_SDR_GPIO</sub>      | Data hold time                              | 6                            | –   | –    | ns    |                                                |
| SID781A                                           | t <sub>V_SDR_GPIO</sub>       | Clock LOW output valid                      | 4.5                          | –   | 9    | ns    |                                                |
| SID782A                                           | t <sub>HO_SDR_GPIO</sub>      | Input hold time                             | 2                            | –   | –    | ns    |                                                |
| SID783A                                           | t <sub>DIS_SDR_GPIO</sub>     | Input disable time                          | 0                            | –   | 22.5 | ns    |                                                |

**Table 26-34 SMIF specifications (continued)[Conditions: drive\_sel<1:0>= 00]**

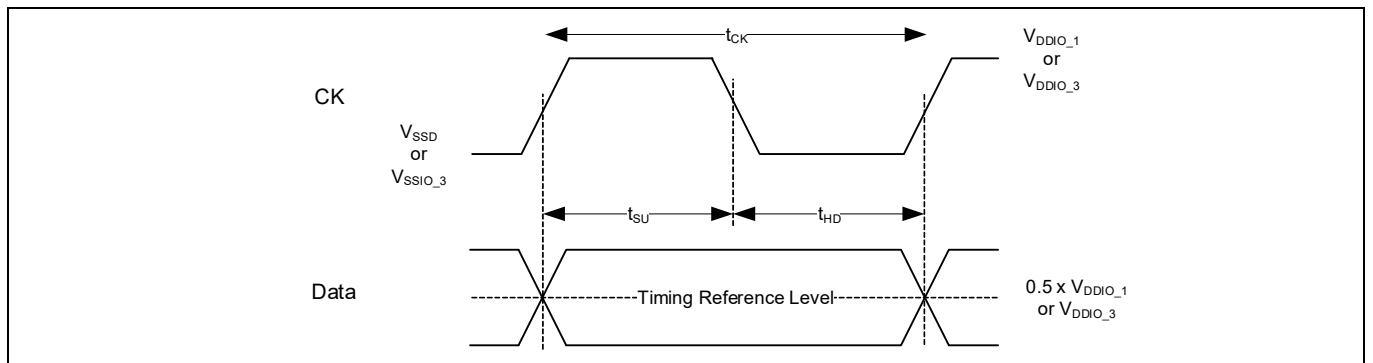
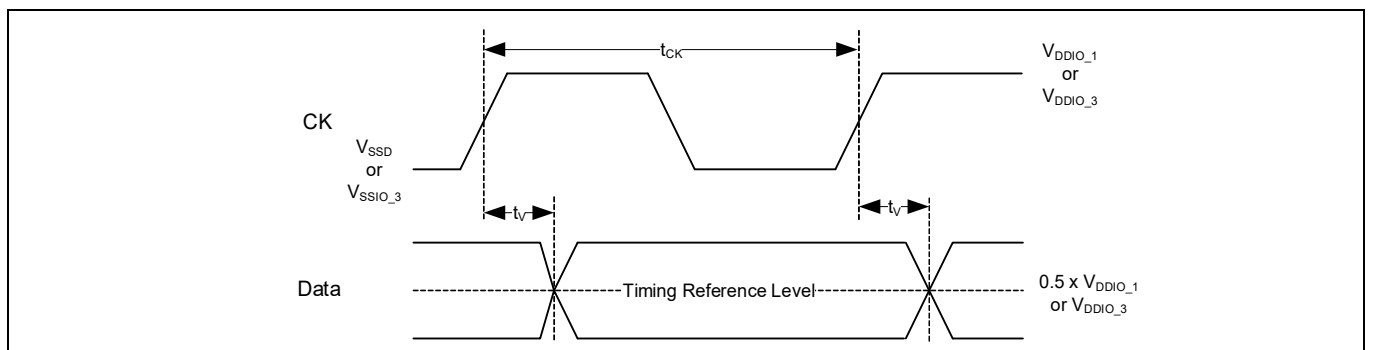
| Spec ID                                           | Parameter                      | Description                                 | Min                           | Typ | Max  | Units | Details/conditions   |
|---------------------------------------------------|--------------------------------|---------------------------------------------|-------------------------------|-----|------|-------|----------------------|
| SID784A                                           | t <sub>IO_SKEW_S-DR_GPIO</sub> | Data skew (first data bit to last data bit) | –                             | –   | 1.8  | ns    | Guaranteed by design |
| <b>SMIF HSSPI(DDR) Specification for HSIO_STD</b> |                                |                                             |                               |     |      |       |                      |
| SID760B                                           | C <sub>L_DDR_HSIO</sub>        | Load capacitance                            | –                             | –   | 15   | pF    |                      |
| SID761B                                           | SR <sub>DDR_HSIO</sub>         | Input rise and fall slew rates              | 1.5                           | –   | –    | V/ns  | Guaranteed by design |
| SID762B2                                          | f <sub>CK_DDR_HSIO</sub>       | Clock frequency                             | –                             | –   | 90   | MHz   |                      |
| SID763B                                           | t <sub>CK_DDR_HSIO</sub>       | Clock period                                | 1 / f <sub>CK_D-DR_HSIO</sub> | –   | –    | ns    |                      |
| SID764B                                           | DCK <sub>D-DR_HSIO</sub>       | Clock duty                                  | 45                            | –   | 55   | %     |                      |
| SID765B                                           | CSR <sub>DDR_HSIO</sub>        | Clock rise and fall slew rates              | 1.5                           | –   | –    | V/ns  |                      |
| SID766B                                           | t <sub>CS_DDR_HSIO</sub>       | Chip select HIGH time                       | 10                            | –   | –    | ns    |                      |
| SID767B                                           | t <sub>CSS_DDR_HSIO</sub>      | Chip select active setup time               | 4                             | –   | –    | ns    |                      |
| SID768B                                           | t <sub>CSH_DDR_HSIO</sub>      | Chip select active hold time                | 4                             | –   | –    | ns    |                      |
| SID769B                                           | t <sub>SU_DDR_HSIO</sub>       | Data setup time                             | 2                             | –   | –    | ns    |                      |
| SID780B                                           | t <sub>HD_DDR_HSIO</sub>       | Data hold time                              | 1.2                           | –   | –    | ns    |                      |
| SID781B                                           | t <sub>V_DDR_HSIO</sub>        | Clock LOW output valid                      | 0                             | –   | 6.5  | ns    |                      |
| SID782B                                           | t <sub>HO_DDR_HSIO</sub>       | Input hold time                             | 1                             | –   | –    | ns    |                      |
| SID783B                                           | t <sub>DIS_DDR_HSIO</sub>      | Input disable time                          | –                             | –   | 7.5  | ns    |                      |
| SID784B                                           | t <sub>IO_SKEW_D-DR_HSIO</sub> | Data skew (first data bit to last data bit) | –                             | –   | 0.6  | ns    | Guaranteed by design |
| <b>SMIF HSSPI(DDR) Specification for GPIO_STD</b> |                                |                                             |                               |     |      |       |                      |
| SID760C                                           | C <sub>L_DDR_GPIO</sub>        | Load capacitance                            | –                             | –   | 15   | pF    |                      |
| SID761C                                           | SR <sub>DDR_GPIO</sub>         | Input rise and fall slew rates              | 1                             | –   | –    | V/ns  | Guaranteed by design |
| SID762C                                           | f <sub>CK_DDR_GPIO</sub>       | Clock frequency                             | –                             | –   | 32   | MHz   |                      |
| SID763C                                           | t <sub>CK_DDR_GPIO</sub>       | Clock period                                | 1 / f <sub>CK_D-DR_GPIO</sub> | –   | –    | ns    |                      |
| SID764C                                           | DCK <sub>D-DR_GPIO</sub>       | Clock duty                                  | 45                            | –   | 55   | %     |                      |
| SID765C                                           | CSR <sub>DDR_GPIO</sub>        | Clock rise and fall slew rates              | 1                             | –   | –    | V/ns  |                      |
| SID766C                                           | t <sub>CS_DDR_GPIO</sub>       | Chip select HIGH time                       | 30                            | –   | –    | ns    |                      |
| SID767C                                           | t <sub>CSS_DDR_GPIO</sub>      | Chip select active setup time               | 5                             | –   | –    | ns    |                      |
| SID768C                                           | t <sub>CSH_DDR_GPIO</sub>      | Chip select active hold time                | 4                             | –   | –    | ns    |                      |
| SID769C                                           | t <sub>SU_DDR_GPIO</sub>       | Data setup time                             | 5                             | –   | –    | ns    |                      |
| SID780C                                           | t <sub>HD_DDR_GPIO</sub>       | Data hold time                              | 4.5                           | –   | –    | ns    |                      |
| SID781C                                           | t <sub>V_DDR_GPIO</sub>        | Clock LOW output valid                      | 0                             | –   | 9    | ns    |                      |
| SID782C                                           | t <sub>HO_DDR_GPIO</sub>       | Input hold time                             | 3                             | –   | –    | ns    |                      |
| SID783C                                           | t <sub>DIS_DDR_GPIO</sub>      | Input disable time                          | –                             | –   | 22.5 | ns    |                      |
| SID784C                                           | t <sub>IO_SKEW_D-DR_GPIO</sub> | Data skew (first data bit to last data bit) | –                             | –   | 1.8  | ns    | Guaranteed by design |

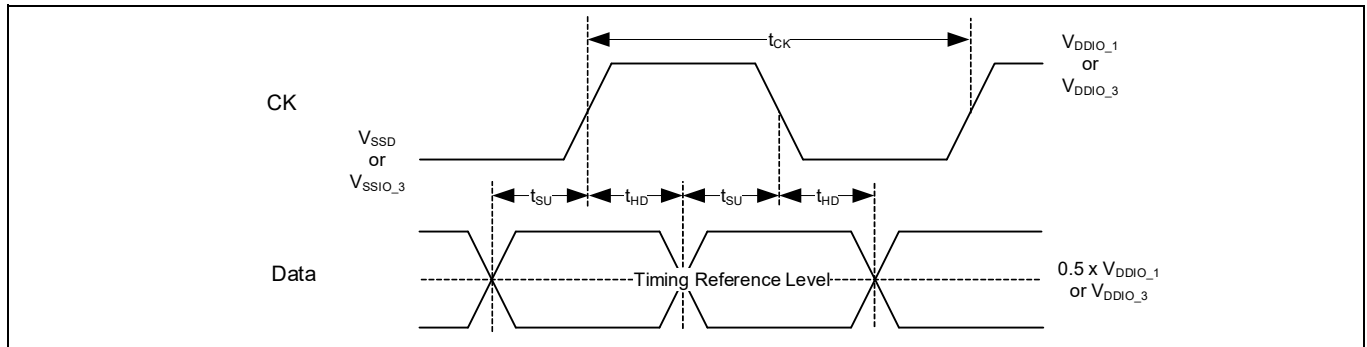
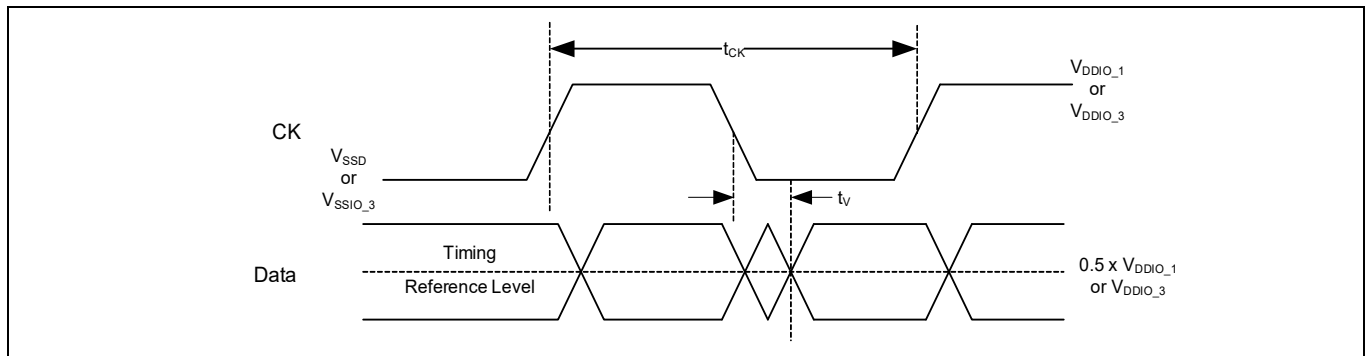
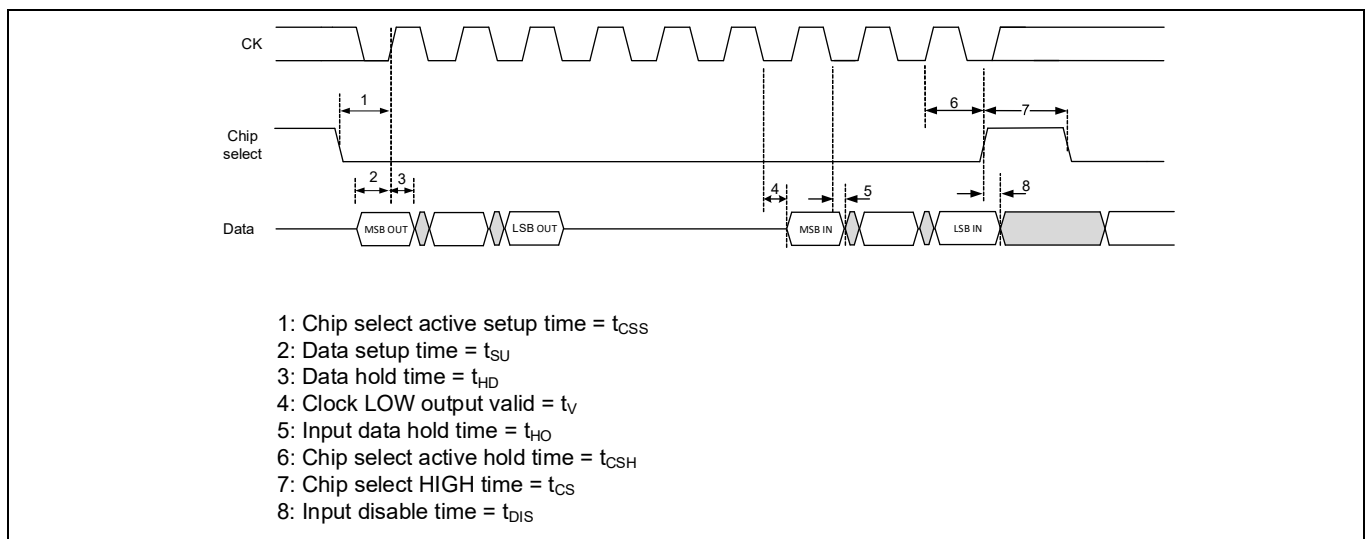
**Table 26-34 SMIF specifications (continued)[Conditions: drive\_sel<1:0>= 00]**

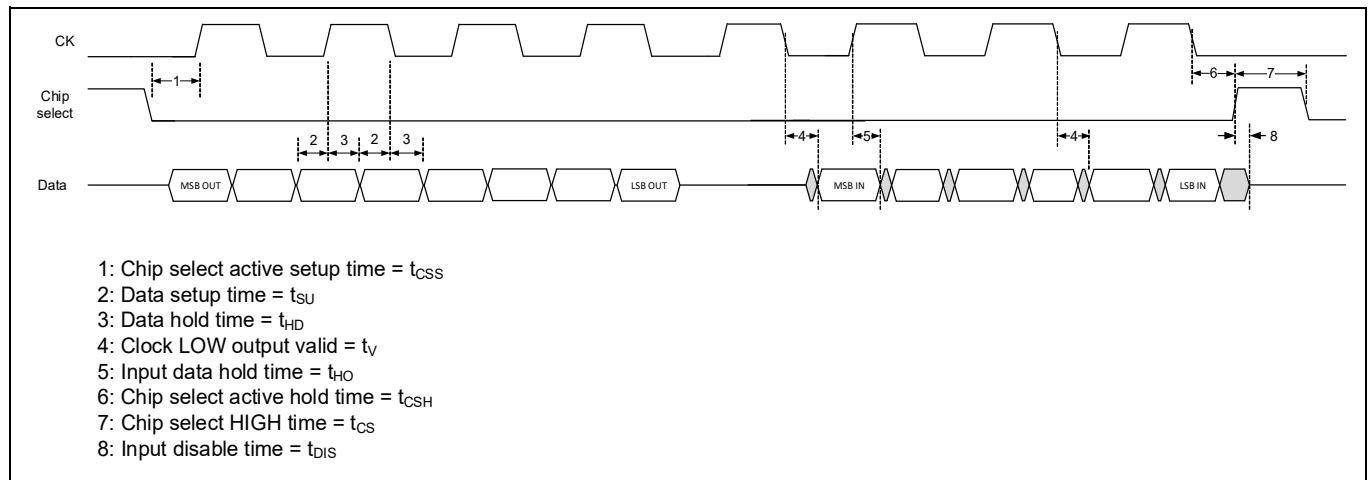
| Spec ID                                          | Parameter                 | Description                              | Min                          | Typ | Max | Units | Details/conditions                    |
|--------------------------------------------------|---------------------------|------------------------------------------|------------------------------|-----|-----|-------|---------------------------------------|
| <b>SMIF HYPERBUS™ Specification for HSIO_STD</b> |                           |                                          |                              |     |     |       |                                       |
| SID785                                           | C <sub>L_HB_HSIO</sub>    | Load capacitance                         | –                            | –   | 20  | pF    |                                       |
| SID786                                           | SRI <sub>_HB_HSIO</sub>   | Input rise and fall slew rates           | 1                            | –   | –   | V/ns  | For all signals, Guaranteed by design |
| SID787                                           | SRO <sub>_HB_HSIO</sub>   | Output rise and fall slew rates          | 1                            | –   | –   | V/ns  | For all signals                       |
| <b>Clock characteristics</b>                     |                           |                                          |                              |     |     |       |                                       |
| SID700                                           | f <sub>CK_HB_HSIO</sub>   | Clock frequency                          | –                            | –   | 100 | MHz   |                                       |
| SID701                                           | t <sub>CK_HB_HSIO</sub>   | Clock period                             | 1 / f <sub>CK_H-B_HSIO</sub> | –   | –   | ns    |                                       |
| SID702                                           | DCK <sub>_HB_HSIO</sub>   | Clock duty                               | 45                           | –   | 55  | %     |                                       |
| <b>AC Parameters</b>                             |                           |                                          |                              |     |     |       |                                       |
| SID706                                           | t <sub>CSHI_HB_HSIO</sub> | Chip select HIGH between transactions    | 10                           | –   | –   | ns    | Guaranteed by design                  |
| SID708                                           | t <sub>CSS_HB_HSIO</sub>  | Chip select setup to next CK rising edge | 3                            | –   | –   | ns    |                                       |
| SID709                                           | t <sub>DSV_HB_HSIO</sub>  | Data strobe valid                        | –                            | –   | 12  | ns    |                                       |
| SID710                                           | t <sub>OSU_HB_HSIO</sub>  | DQ output setup                          | 1                            | –   | –   | ns    |                                       |
| SID711                                           | t <sub>OH_HB_HSIO</sub>   | DQ output hold                           | 1                            | –   | –   | ns    |                                       |
| SID715                                           | t <sub>CKD_HB_HSIO</sub>  | CK transition to DQ valid                | 1                            | –   | 5.5 | ns    |                                       |
| SID718                                           | t <sub>CKDS_HB_HSIO</sub> | CK transition to RWDS valid              | 1                            | –   | 5.5 | ns    |                                       |
| SID719                                           | t <sub>DSS_HB_HSIO</sub>  | RWDS transition to input DQ valid        | –0.8                         | –   | 0.8 | ns    |                                       |
| SID720                                           | t <sub>DSH_HB_HSIO</sub>  | Input DQ invalid to RWDS transition      | –0.8                         | –   | 0.8 | ns    |                                       |
| SID721                                           | t <sub>CSH_HB_HSIO</sub>  | Chip select hold after CK falling edge   | 0                            | –   | –   | ns    |                                       |
| <b>SMIF HYPERBUS™ Specification for GPIO_STD</b> |                           |                                          |                              |     |     |       |                                       |
| SID785A                                          | C <sub>L_HB_GPIO</sub>    | Load capacitance                         | –                            | –   | 20  | pF    |                                       |
| SID786A                                          | SRI <sub>_HB_GPIO</sub>   | Input rise and fall slew rates           | 0.45                         | –   | –   | V/ns  | For all signals, guaranteed by design |
| SID787A                                          | SRO <sub>_HB_GPIO</sub>   | Output rise and fall slew rates          | 0.45                         | –   | –   | V/ns  | For all signals                       |
| <b>Clock characteristics</b>                     |                           |                                          |                              |     |     |       |                                       |
| SID700A                                          | f <sub>CK_HB_GPIO</sub>   | Clock frequency                          | –                            | –   | 32  | MHz   |                                       |
| SID701A                                          | t <sub>CK_HB_GPIO</sub>   | Clock period                             | 1 / f <sub>CK_H-B_GPIO</sub> | –   | –   | ns    |                                       |
| SID702A                                          | DCK <sub>_HB_GPIO</sub>   | Clock duty                               | 45                           | –   | 55  | %     |                                       |
| <b>AC Parameters</b>                             |                           |                                          |                              |     |     |       |                                       |
| SID706A                                          | t <sub>CSHI_HB_GPIO</sub> | Chip select HIGH between transactions    | 30                           | –   | –   | ns    | Guaranteed by design                  |

**Table 26-34 SMIF specifications** (continued) [Conditions: drive\_sel<1:0>= 00]

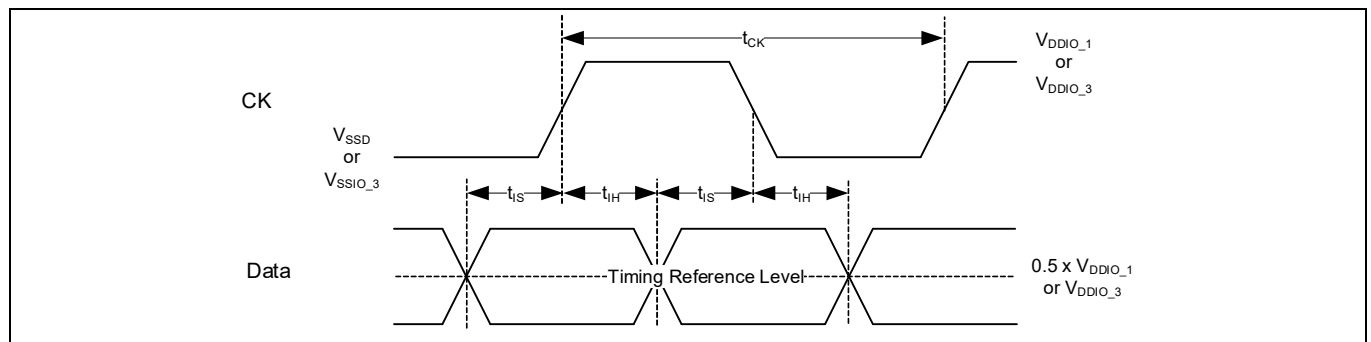
| Spec ID | Parameter            | Description                              | Min  | Typ | Max  | Units | Details/conditions   |
|---------|----------------------|------------------------------------------|------|-----|------|-------|----------------------|
| SID708A | $t_{CSS\_HB\_GPIO}$  | Chip select setup to next CK rising edge | 9    | –   | –    | ns    |                      |
| SID709A | $t_{DSV\_HB\_GPIO}$  | Data strobe valid                        | –    | –   | 36   | ns    | Guaranteed by design |
| SID710A | $t_{OSU\_HB\_GPIO}$  | DQ output setup                          | 3    | –   | –    | ns    |                      |
| SID711A | $t_{OH\_HB\_GPIO}$   | DQ output hold                           | 3    | –   | –    | ns    |                      |
| SID715A | $t_{CKD\_HB\_GPIO}$  | CK transition to DQ valid                | 3    | –   | 16.5 | ns    |                      |
| SID718A | $t_{CKDS\_HB\_GPIO}$ | CK transition to RWDS valid              | 3    | –   | 16.5 | ns    |                      |
| SID719A | $t_{DSS\_HB\_GPIO}$  | RWDS transition to input DQ valid        | –2.4 | –   | 2.4  | ns    |                      |
| SID720A | $t_{DSH\_HB\_GPIO}$  | Input DQ invalid to RWDS transition      | –2.4 | –   | 2.4  | ns    |                      |
| SID721A | $t_{CSH\_HB\_GPIO}$  | Chip select hold after CK falling edge   | 0    | –   | –    | ns    |                      |


**Figure 26-40 SDR write timing reference level**

**Figure 26-41 SDR read timing reference level**

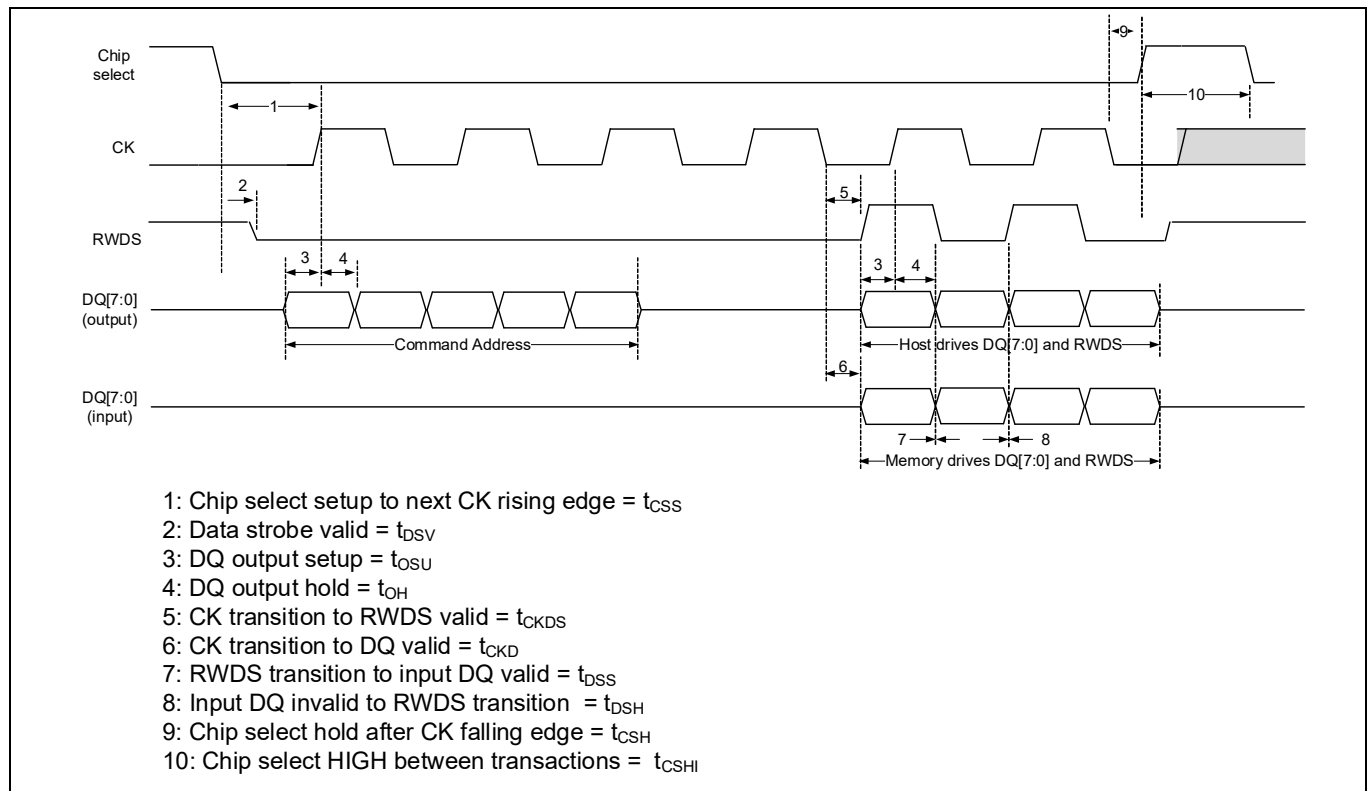

**Figure 26-42 DDR write timing reference level**

**Figure 26-43 DDR read timing reference level**

**Figure 26-44 SDR write and read timing diagram**



**Figure 26-45** DDR write and read timing diagram



**Figure 26-46** HYPERBUS™ timing reference level


**Figure 26-47 HYPERBUS™ timing diagram**

## 27 Ordering information

The CYT3BB/4BB microcontroller part numbers and features are listed in [Table 27-1](#). The Arm® TAP JTAG ID is 0x6BA0 0477.

**Table 27-1 CYT3BB/4BB Ordering information**

| Device Code                | Ordering Code <sup>[76]</sup> | Package   | CM7 Cores | Code-flash (KB)      | Work-flash (KB)     | RAM (KB) | ADC Channels | SCB Channels | LIN Channels | I <sup>2</sup> S Channels | Ethernet Channels | SD/eMMC | Temperature Grade | JTAG ID Code               |
|----------------------------|-------------------------------|-----------|-----------|----------------------|---------------------|----------|--------------|--------------|--------------|---------------------------|-------------------|---------|-------------------|----------------------------|
| CYT3BB5CES                 | CYT3BB5CEBQ0AESGS             | 100-TEQFP | 1         | 4160 <sup>[77]</sup> | 256 <sup>[78]</sup> | 768      | 39           | 9            | 9            | 2                         | 1                 | 1       | S <sup>[79]</sup> | 0x1E919069 <sup>[82]</sup> |
| CYT3BB5CEE                 | CYT3BB5CEBQ0AEEGS             | 100-TEQFP | 1         | 4160                 | 256                 | 768      | 39           | 9            | 9            | 2                         | 1                 | 1       | E <sup>[80]</sup> | 0x1E919069                 |
| CYT3BB7CES                 | CYT3BB7CEBQ0AESGS             | 144-TEQFP | 1         | 4160                 | 256                 | 768      | 54           | 10           | 12           | 3                         | 1                 | 1       | S                 | 0x1E91A069                 |
| CYT3BB7CEE                 | CYT3BB7CEBQ0AEEGS             | 144-TEQFP | 1         | 4160                 | 256                 | 768      | 54           | 10           | 12           | 3                         | 1                 | 1       | E                 | 0x1E91A069                 |
| CYT3BB8CES                 | CYT3BB8CEBQ0AESGS             | 176-TEQFP | 1         | 4160                 | 256                 | 768      | 64           | 10           | 16           | 3                         | 1                 | 1       | S                 | 0x1E91B069                 |
| CYT3BB8CEE                 | CYT3BB8CEBQ0AEEGS             | 176-TEQFP | 1         | 4160                 | 256                 | 768      | 64           | 10           | 16           | 3                         | 1                 | 1       | E                 | 0x1E91B069                 |
| CYT3BBBCES                 | CYT3BBBCEBQ0BZSGS             | 272-BGA   | 1         | 4160                 | 256                 | 768      | 72           | 11           | 16           | 3                         | 1                 | 1       | S                 | 0x1E91C069                 |
| CYT3BBBCEE                 | CYT3BBBCEBQ0BZEGS             | 272-BGA   | 1         | 4160                 | 256                 | 768      | 72           | 11           | 16           | 3                         | 1                 | 1       | E                 | 0x1E91C069                 |
| CYT4BB5CES                 | CYT4BB5CEBQ0AESGS             | 100-TEQFP | 2         | 4160                 | 256                 | 768      | 39           | 9            | 9            | 2                         | 1                 | 1       | S                 | 0x1E91D069                 |
| CYT4BB5CEE <sup>[81]</sup> | CYT4BB5CEBQ0AEEGS             | 100-TEQFP | 2         | 4160                 | 256                 | 768      | 39           | 9            | 9            | 2                         | 1                 | 1       | E                 | 0x1E91D069                 |
| CYT4BB7CES                 | CYT4BB7CEBQ0AESGS             | 144-TEQFP | 2         | 4160                 | 256                 | 768      | 54           | 10           | 12           | 3                         | 1                 | 1       | S                 | 0x1E91E069                 |
| CYT4BB7CEE <sup>[81]</sup> | CYT4BB7CEBQ0AEEGS             | 144-TEQFP | 2         | 4160                 | 256                 | 768      | 54           | 10           | 12           | 3                         | 1                 | 1       | E                 | 0x1E91E069                 |
| CYT4BB8CES                 | CYT4BB8CEBQ0AESGS             | 176-TEQFP | 2         | 4160                 | 256                 | 768      | 64           | 10           | 16           | 3                         | 1                 | 1       | S                 | 0x1E91F069                 |
| CYT4BB8CEE <sup>[81]</sup> | CYT4BB8CEBQ0AEEGS             | 176-TEQFP | 2         | 4160                 | 256                 | 768      | 64           | 10           | 16           | 3                         | 1                 | 1       | E                 | 0x1E91F069                 |
| CYT4BBBCES                 | CYT4BBBCEBQ0BZSGS             | 272-BGA   | 2         | 4160                 | 256                 | 768      | 72           | 11           | 16           | 3                         | 1                 | 1       | S                 | 0x1E920069                 |
| CYT4BBBCEE <sup>[81]</sup> | CYT4BBBCEBQ0BZEGS             | 272-BGA   | 2         | 4160                 | 256                 | 768      | 72           | 11           | 16           | 3                         | 1                 | 1       | E                 | 0x1E920069                 |

### Notes

76.Supported shipment types are “Tray” (default) and “Tape and Reel”. Add the character ‘T’ at the end to get the ordering code for “Tape and Reel” shipment type.

77.Code-flash size 4160 KB = 32 KB × 126 (Large Sectors) + 8 KB × 16 (Small Sectors).

78.Work-flash size 256 KB = 2 KB × 96 (Large Sectors) + 128 B × 512 (Small Sectors).

79.S-grade Temperature (–40 °C to 105 °C).

80.E-grade Temperature (–40 °C to 125 °C).

81.These parts are available as engineering samples.

82.JTAG ID CODE bits 12 through 27, represents the Silicon ID of the device.

## 27.1 Part number nomenclature

**Table 27-2 Device code nomenclature**

| Field | Description                         | Value | Meaning                       |
|-------|-------------------------------------|-------|-------------------------------|
| CY    | Cypress Prefix                      | CY    |                               |
| T     | Category                            | T     | TRAVEO™                       |
| 2     | Family Name                         | 3     | TRAVEO™ T2G (Core M7 Single)  |
|       |                                     | 4     | TRAVEO™ T2G (Core M7 dual)    |
| B     | Application                         | B     | Body                          |
| D     | Code-flash/Work-flash/SRAM quantity | B     | 4160 KB / 256 KB / 768 KB     |
| P     | Packages                            | B     | 272-BGA                       |
|       |                                     | 8     | 176-TEQFP                     |
|       |                                     | 7     | 144-TEQFP                     |
|       |                                     | 5     | 100-TEQFP                     |
| H     | Hardware Option                     | C     | eSHE – on, HSM – on, RSA - 2K |
| I     | Marketing Option                    | E     | Ethernet - 1 ch, eMMC - on    |
| C     | Temperature Grade                   | S     | S-grade (–40 °C to 105 °C)    |
|       |                                     | E     | E-grade (–40 °C to 125 °C)    |

**Table 27-3 Ordering code nomenclature**

| Field | Description                         | Value | Meaning                       |
|-------|-------------------------------------|-------|-------------------------------|
| CY    | Cypress Prefix                      | CY    |                               |
| T     | Category                            | T     | TRAVEO™                       |
| 2     | Family Name                         | 3     | TRAVEO™ T2G (Core M7 Single)  |
|       |                                     | 4     | TRAVEO™ T2G (Core M7 dual)    |
| B     | Application                         | B     | Body                          |
| D     | Code-flash/Work-flash/SRAM quantity | B     | 4160 KB / 256 KB / 768 KB     |
| P     | Packages                            | B     | 272-BGA                       |
|       |                                     | 8     | 176-TEQFP                     |
|       |                                     | 7     | 144-TEQFP                     |
|       |                                     | 5     | 100-TEQFP                     |
| H     | Hardware Option                     | C     | eSHE – on, HSM – on, RSA - 2K |
| I     | Marketing Option                    | E     | Ethernet - 1 ch, eMMC - on    |
| R     | Revision                            | A     | First revision                |
|       |                                     | B     | Second revision               |
| F     | Fab Location                        | Q     | UMC (Fab 12i) Singapore       |
| X     | Reserved                            | 0     | Reserved                      |
| K     | Package Code                        | AE    | TEQFP                         |
|       |                                     | BZ    | BGA                           |
| C     | Temperature Grade                   | S     | S-grade (–40 °C to 105 °C)    |
|       |                                     | E     | E-grade (–40 °C to 125 °C)    |
| Q     | Quality Grade                       | ES    | Engineering samples           |
|       |                                     | GS    | Standard grade of automotive  |
| S     | Shipment Type                       | Blank | Tray shipment                 |
|       |                                     | T     | Tape and Reel shipment        |

## 28 Packaging

CYT3BB/4BB microcontroller is offered in the packages listed in the [Table 28-1](#).

**Table 28-1 Package information**

| Package   | Dimensions <sup>[83]</sup> | Contact/Lead pitch | Coefficient of thermal expansion                              | I/O pins |
|-----------|----------------------------|--------------------|---------------------------------------------------------------|----------|
| 272-BGA   | 16 × 16 × 1.70 mm (max)    | 0.8-mm             | a1 <sup>[84]</sup> = 6 ppm/°C, a2 <sup>[85]</sup> = 25 ppm/°C | 220      |
| 176-TEQFP | 24 × 24 × 1.60 mm (max)    | 0.5-mm             | a1 = 9.5 ppm/°C, a2 = 37 ppm/°C                               | 148      |
| 144-TEQFP | 20 × 20 × 1.60 mm (max)    | 0.5-mm             | a1 = 9.5 ppm/°C, a2 = 36.7 ppm/°C                             | 116      |
| 100-TEQFP | 14 × 14 × 1.60 mm (max)    | 0.5-mm             | a1 = 9.4 ppm/°C, a2 = 36 ppm/°C                               | 72       |

**Table 28-2 Package characteristics**

| Parameter        | Description                                                                         | Conditions | Min | Typ | Max  | Units |
|------------------|-------------------------------------------------------------------------------------|------------|-----|-----|------|-------|
| T <sub>A</sub>   | Operating ambient temperature                                                       | S-grade    | −40 | −   | 105  | °C    |
| T <sub>A</sub>   | Operating ambient temperature                                                       | E-grade    | −40 | −   | 125  | °C    |
| T <sub>J</sub>   | Operating junction temperature                                                      | −          | −   | −   | 150  | °C    |
| R <sub>θJA</sub> | Package thermal resistance, junction to ambient θ <sub>JA</sub> <sup>[86, 87]</sup> | 272-BGA    | −   | −   | 21.6 | °C/W  |
|                  |                                                                                     | 176-TEQFP  | −   | −   | 17.8 | °C/W  |
|                  |                                                                                     | 144-TEQFP  | −   | −   | 17.4 | °C/W  |
|                  |                                                                                     | 100-TEQFP  | −   | −   | 18.3 | °C/W  |
| R <sub>θJB</sub> | Package θ <sub>JB</sub>                                                             | 272-BGA    | −   | −   | 12.8 | °C/W  |
|                  |                                                                                     | 176-TEQFP  | −   | −   | 13.0 | °C/W  |
|                  |                                                                                     | 144-TEQFP  | −   | −   | 12.3 | °C/W  |
|                  |                                                                                     | 100-TEQFP  | −   | −   | 10.4 | °C/W  |
| R <sub>θJC</sub> | Package thermal resistance, junction to case θ <sub>JC</sub>                        | 272-BGA    | −   | −   | 10.4 | °C/W  |
|                  |                                                                                     | 176-TEQFP  | −   | −   | 8.0  | °C/W  |
|                  |                                                                                     | 144-TEQFP  | −   | −   | 8.1  | °C/W  |
|                  |                                                                                     | 100-TEQFP  | −   | −   | 8.5  | °C/W  |

**Table 28-3 Solder reflow peak temperature, package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2**

| Package   | Maximum peak temperature (°C) | Maximum time at peak temperature (seconds) | MSL |
|-----------|-------------------------------|--------------------------------------------|-----|
| 272-BGA   | 260                           | 30                                         | 3   |
| 176-TEQFP | 260                           | 30                                         | 3   |
| 144-TEQFP | 260                           | 30                                         | 3   |
| 100-TEQFP | 260                           | 30                                         | 3   |

**Notes**

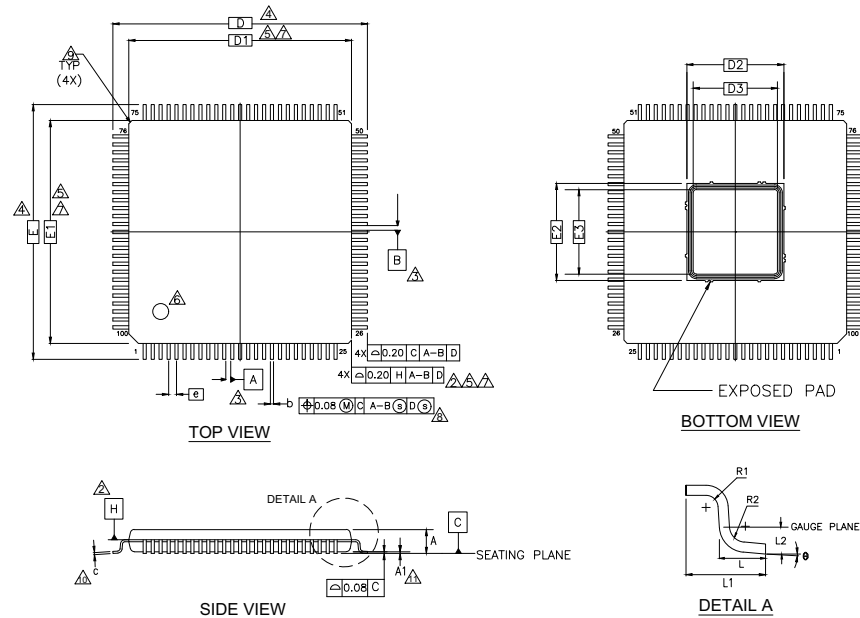
83.The dimensions (column 2) are valid for room temperature.

84.a1 = CTE (Coefficient of Thermal Expansion) value below T<sub>g</sub> (ppm/°C) (T<sub>g</sub> is glass transition temperature which is 131°C).

85.a2 = CTE value above T<sub>g</sub> (ppm/°C).

86.Maximum value °C/Watt shown is for T<sub>A</sub> = 125 °C.

87.Board condition complies to JESD51-7(4 Layers).



| SYMBOL | DIMENSION |       |      |
|--------|-----------|-------|------|
|        | MIN.      | NOM.  | MAX. |
| A      | —         | —     | 1.60 |
| A1     | 0.05      | —     | 0.15 |
| D      | 16.00 BSC |       |      |
| D1     | 14.00 BSC |       |      |
| D2     | 6.10 REF  |       |      |
| D3     | 5.30 REF  |       |      |
| E      | 16.00 BSC |       |      |
| E1     | 14.00 BSC |       |      |
| E2     | 6.10 REF  |       |      |
| E3     | 5.30 REF  |       |      |
| R1     | 0.08      | —     | —    |
| R2     | 0.08      | —     | 0.20 |
| θ      | 0°        | —     | 8°   |
| c      | 0.09      | 0.127 | 0.20 |
| b      | 0.15      | —     | 0.27 |
| L      | 0.45      | 0.60  | 0.75 |
| L1     | 1.00 REF  |       |      |
| L2     | 0.25 REF  |       |      |
| e      | 0.50 BSC  |       |      |

**NOTES**

1. ALL DIMENSIONS ARE IN MILLIMETERS.

△ DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

△ DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.

△ TO BE DETERMINED AT SEATING PLANE C.

△ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.

ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE.

△ DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

△ DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

△ REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.

△ DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBER CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

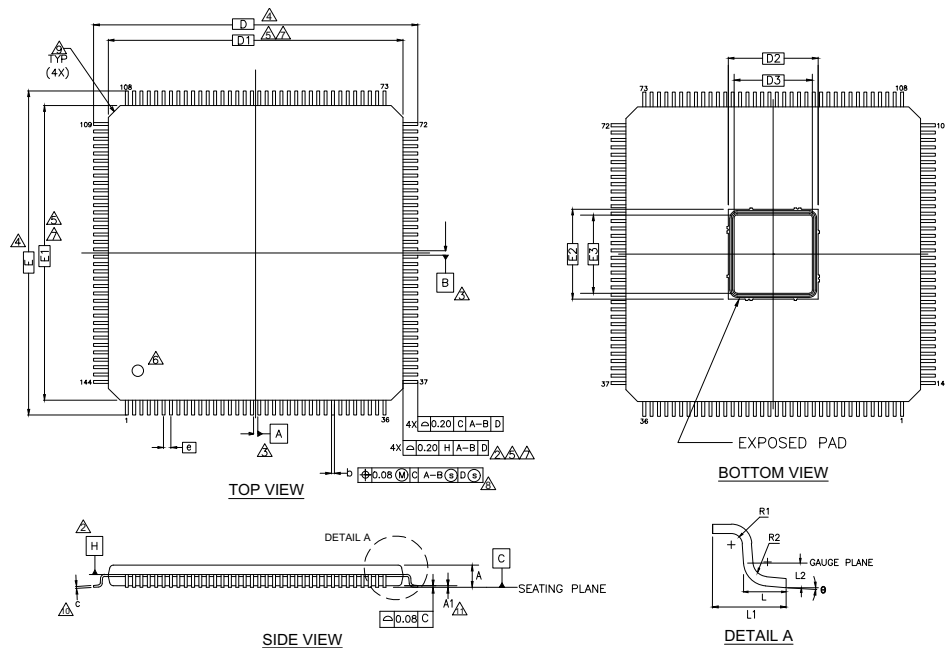
△ EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

△ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

△ A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-28239 \*B

**Figure 28-1 Package outline – 100-TEQFP**



| SYMBOL | DIMENSION |       |      |
|--------|-----------|-------|------|
|        | MIN.      | NOM.  | MAX. |
| A      | —         | —     | 1.60 |
| A1     | 0.05      | —     | 0.15 |
| D      | 22.00 BSC |       |      |
| D1     | 20.00 BSC |       |      |
| D2     | 6.10 REF  |       |      |
| D3     | 5.30 REF  |       |      |
| E      | 22.00 BSC |       |      |
| E1     | 20.00 BSC |       |      |
| E2     | 6.10 REF  |       |      |
| E3     | 5.30 REF  |       |      |
| R1     | 0.08      | —     | —    |
| R2     | 0.08      | —     | 0.20 |
| θ      | 0°        | —     | 8°   |
| c      | 0.09      | 0.127 | 0.20 |
| b      | 0.17      | 0.20  | 0.27 |
| L      | 0.45      | 0.60  | 0.75 |
| L1     | 1.00 REF  |       |      |
| L2     | 0.25 REF  |       |      |
| e      | 0.50 BSC  |       |      |

#### NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.

△ DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

△ DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.

△ TO BE DETERMINED AT SEATING PLANE C.

△ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.

ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE.  
DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

△ DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

△ REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.

△ DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

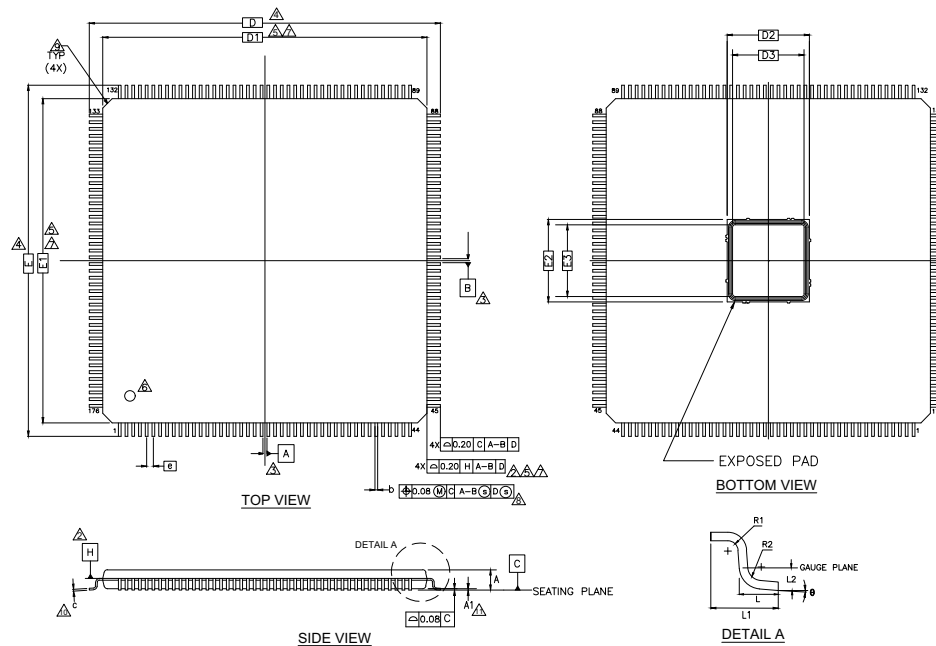
△ EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

△ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

△ A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-28240 \*B

Figure 28-2 Package outline - 144-TEQFP



| SYMBOL | DIMENSION |       |      |
|--------|-----------|-------|------|
|        | MIN.      | NOM.  | MAX. |
| A      | —         | —     | 1.60 |
| A1     | 0.05      | —     | 0.15 |
| D      | 26.00 BSC |       |      |
| D1     | 24.00 BSC |       |      |
| D2     | 6.10 REF  |       |      |
| D3     | 5.30 REF  |       |      |
| E      | 26.00 BSC |       |      |
| E1     | 24.00 BSC |       |      |
| E2     | 6.10 REF  |       |      |
| E3     | 5.30 REF  |       |      |
| R1     | 0.08      | —     | —    |
| R2     | 0.08      | —     | 0.20 |
| θ      | 0°        | —     | 8°   |
| c      | 0.09      | 0.127 | 0.20 |
| b      | 0.17      | 0.20  | 0.27 |
| L      | 0.45      | 0.60  | 0.75 |
| L1     | 1.00 REF  |       |      |
| L2     | 0.25 REF  |       |      |
| e      | 0.50 BSC  |       |      |

#### NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.

△ DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

△ DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.

△ TO BE DETERMINED AT SEATING PLANE C.

△ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE.

△ DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

△ DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

△ REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.

△ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

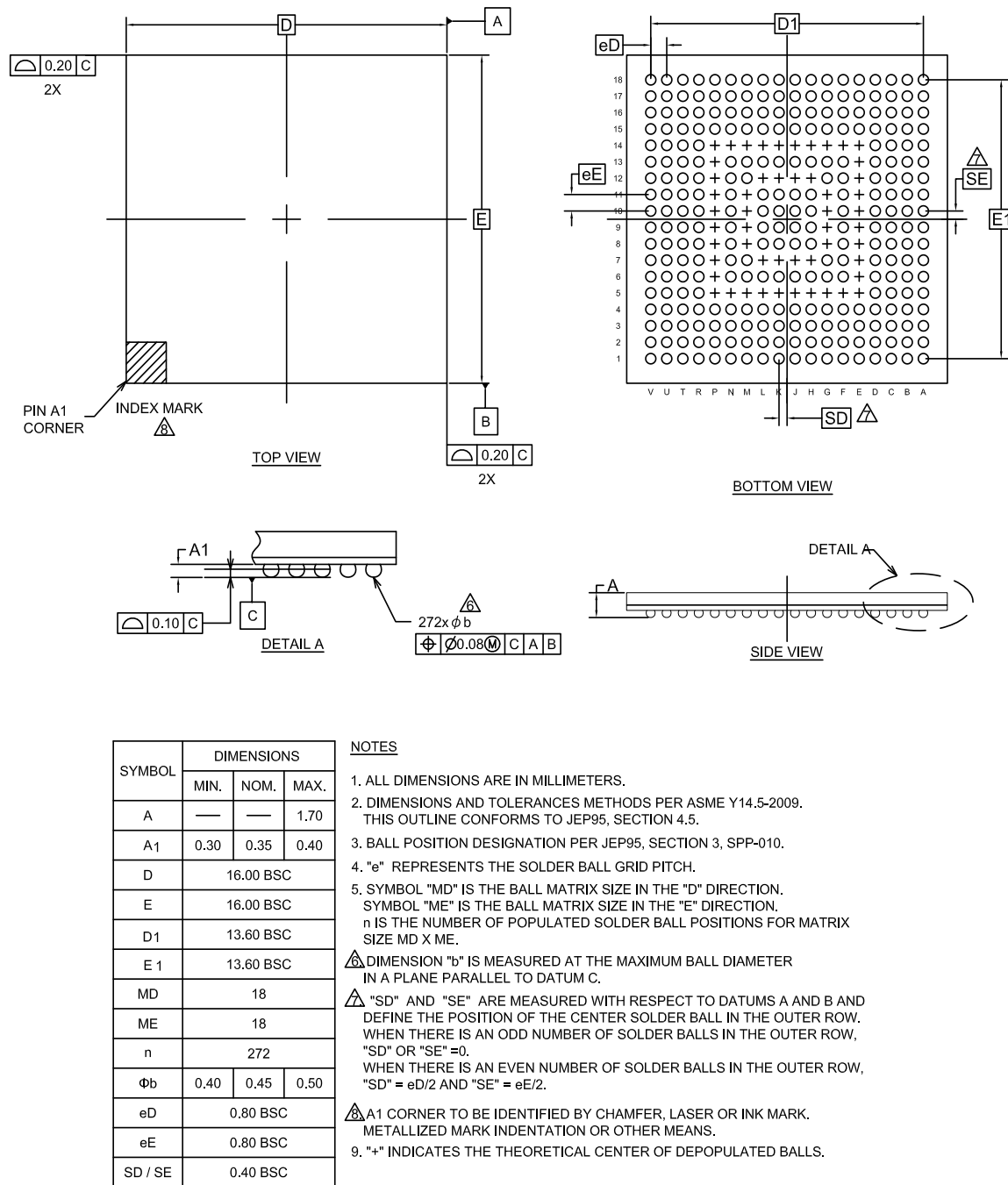
△ EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

△ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

△ A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-28241 \*B

**Figure 28-3 Package outline - 176-TEQFP**



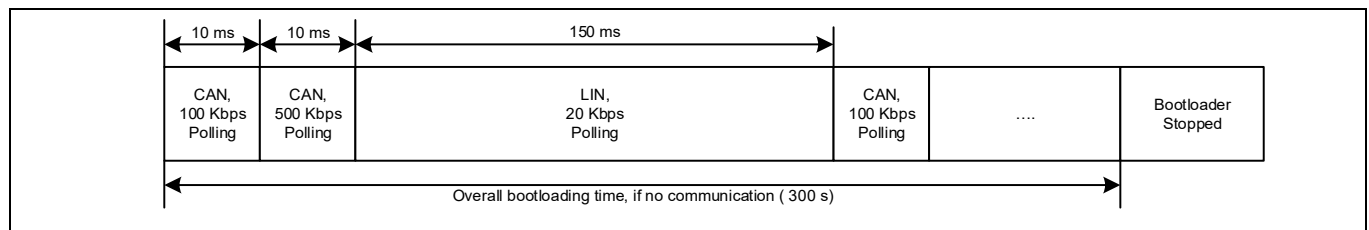
002-24865 \*A

**Figure 28-4 Package outline - 272-BGA**

## 29 Appendix

### 29.1 Bootloading or End-of-line (EoL) Programming

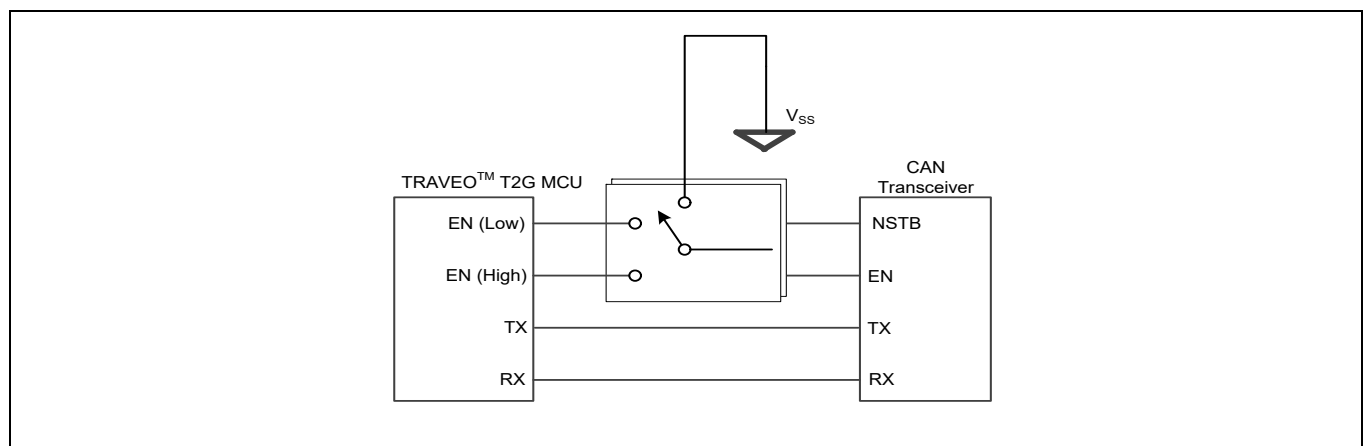
- Triggered at device startup, if a trigger condition is applied
- Either CAN or LIN communication may be used
- Bootloader polls for the communication on CAN or LIN at separate time frames, until the overall 300-second timeout is reached
- If a bootloader command is received on either communication interface, the polling stops and bootloader starts using this interface



**Figure 29-1 Bootloading sequence**

**Table 29-1 CAN interface details**

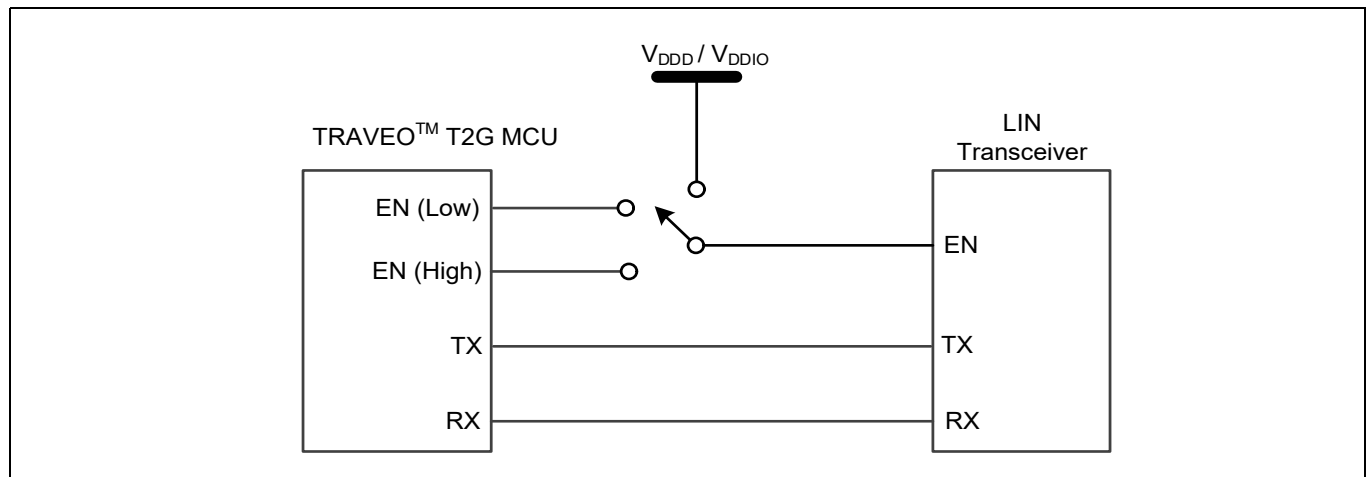
| Sl. No. | CAN interface                   | Configuration               |
|---------|---------------------------------|-----------------------------|
| 1       | CAN Mode                        | Classic CAN                 |
| 2       | CAN Instance                    | CAN0, Channel#1             |
| 3       | CAN TX                          | P0.2 / CAN0_1_TX            |
| 4       | CAN RX                          | P0.3 / CAN0_1_RX            |
| 5       | CAN Transceiver NSTB / EN (Low) | P23.3 (optional)            |
| 6       | CAN Transceiver EN / EN (High)  | P2.1 (optional)             |
| 7       | CAN RX Message ID               | 0x1A1                       |
| 8       | CAN TX Message ID               | 0x1B1                       |
| 9       | Baud                            | 100 or 500 kbps alternating |



**Figure 29-2 MCU to CAN transceiver connections**

**Table 29-2 LIN interface details**

| Sl. No. | LIN Interface          | Configuration    |
|---------|------------------------|------------------|
| 1       | LIN Type               | LIN0, Channel#1  |
| 2       | LIN Mode               | Slave            |
| 3       | LIN Checksum Type      | Classic          |
| 4       | LIN TX                 | P0.1 / LIN1_TX   |
| 5       | LIN RX                 | P0.0 / LIN1_RX   |
| 6       | LIN EN / EN (High)     | P2.1 (optional)  |
| 7       | LIN EN (Low)           | P23.3 (optional) |
| 8       | LIN TX PID             | 0x46             |
| 9       | LIN RX PID             | 0x45             |
| 10      | Baud                   | 20 or 115.2 kbps |
| 11      | Break Field Length     | 11               |
| 12      | Break Delimiter Length | 1 bit            |



**Figure 29-3 MCU to LIN transceiver connections**

## 29.2 External IP revisions

**Table 29-3 IP revisions**

| Module           | IP             | Revision                       | Vendor   |
|------------------|----------------|--------------------------------|----------|
| SDHC             | mxsdhc         | version 1.70a                  | Synopsys |
| CANFD            | mxttcanfd      | M_TTCAN IP revision: Rev.3.2.3 | Bosch    |
| Arm® Cortex®-M0+ | armcm0p        | Cortex-M0+-r0p1                | Arm®     |
| Arm® Cortex®-M7  | armcm7         | Cortex-M7-r1p2                 | Arm®     |
| Arm® Coresight   | armcoresighttk | CoreSight-SoC-TM100-r3p2       | Arm®     |
| Ethernet         | mxeth          | GEM_GXL r1p09                  | Cadence  |

## 30 Acronyms

**Table 30-1 Acronyms used in the document**

| Acronym          | Description                                                                                   | Acronym | Description                                            |
|------------------|-----------------------------------------------------------------------------------------------|---------|--------------------------------------------------------|
| A/D              | Analog to Digital                                                                             | PLL     | Phase Locked Loop                                      |
| ABS              | Absolute                                                                                      | POR     | Power-on reset                                         |
| ADC              | Analog to Digital converter                                                                   | PPU     | Peripheral protection unit                             |
| AES              | Advanced encryption standard                                                                  | PRNG    | Pseudo-random number generator                         |
| AHB              | AMBA (advanced microcontroller bus architecture) high-performance bus, Arm® data transfer bus | PSoC    | Programmable system on chip                            |
| Arm®             | Advanced RISC machine, a CPU architecture                                                     | PWM     | Pulse-width modulation                                 |
| ASIL             | Automotive safety integrity level                                                             | MCU     | Microcontroller Unit                                   |
| BOD              | Brown-out detection                                                                           | MCWDT   | Multi-counter watchdog timer                           |
| CAN FD           | Controller Area Network with Flexible Data rate                                               | M-DMA   | Memory-Direct Memory Access                            |
| CMOS             | Complementary metal-oxide-semiconductor                                                       | MISO    | Master-in slave-out                                    |
| CPU              | Central Processing Unit                                                                       | MMIO    | Memory mapped I/O                                      |
| CRC              | Cyclic redundancy check, an error-checking protocol                                           | MOSI    | Master-out slave-in                                    |
| CSV              | Clock supervisor                                                                              | MPU     | Memory protection unit                                 |
| CTI              | Cross Trigger Interface                                                                       | NVIC    | Nested vectored interrupt controller                   |
| DES              | Data encryption standard                                                                      | RAM     | Random access memory                                   |
| ECC              | Error correcting code                                                                         | RISC    | Reduced-instruction-set computing                      |
| ECO              | External crystal oscillator                                                                   | ROM     | Read only memory                                       |
| ETM              | Embedded Trace Macrocell                                                                      | RTC     | Real-time clock                                        |
| FLL              | Frequency Locked Loop                                                                         | SAR     | Successive approximation register                      |
| FPU              | Floating point unit                                                                           | SCB     | Serial communication block                             |
| GHS              | Green hills tool chain with IDE                                                               | SCL     | I <sup>2</sup> C serial clock                          |
| GPIO             | General-purpose input/output                                                                  | SDA     | I <sup>2</sup> C serial data                           |
| HSM              | Hardware security module                                                                      | SHA     | Secure hash algorithm                                  |
| I/O              | Input/output                                                                                  | SHE     | Secure hardware extension                              |
| I <sup>2</sup> C | Inter-Integrated Circuit, a communications protocol                                           | SMPU    | Shared memory protection unit                          |
| I <sup>2</sup> S | Inter-Integrated Circuit Sound                                                                | SPI     | Serial peripheral interface, a communications protocol |
| ILO              | Internal low-speed oscillator                                                                 | SRAM    | Static random access memory                            |
| IMO              | Internal main oscillator                                                                      | SWD     | Single wire debug                                      |
| IPC              | Inter-processor communication                                                                 | TCM     | Tightly Coupled Memory                                 |
| IrDA             | Infrared interface                                                                            | TCPWM   | Timer/Counter Pulse-width modulator                    |
| IRQ              | Interrupt request                                                                             | TTL     | Transistor-transistor logic                            |
| JTAG             | Joint test action group                                                                       | TRNG    | True random number generator                           |

Acronyms

**Table 30-1 Acronyms used in the document**

| <b>Acronym</b> | <b>Description</b>                                    | <b>Acronym</b> | <b>Description</b>                                                     |
|----------------|-------------------------------------------------------|----------------|------------------------------------------------------------------------|
| LIN            | Local Interconnect Network, a communications protocol | UART           | Universal Asynchronous Transmitter Receiver, a communications protocol |
| LVD            | Low voltage detection                                 | WCO            | Watch crystal oscillator                                               |
| OTA            | Over-the-air programming                              | WDT            | Watchdog timer reset                                                   |
| OTP            | One-time programmable                                 | XIP            | eXecute In Place                                                       |
| OVD            | Overvoltage detection                                 | XTAL           | Crystal                                                                |
| PASS           | Programmable Analog Subsystem                         |                |                                                                        |
| P-DMA          | Peripheral-Direct Memory Access                       |                |                                                                        |

## 31 Errata

This section describes the errata for the CYT3BB/4BB product family. Details include trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Infineon Sales Representative if you have further questions.

### Part numbers affected

| Part numbers         |
|----------------------|
| All CYT3BB/4BB parts |

### CYT3BB/4BB qualification status

Production samples

### CYT3BB/4BB errata summary

The following table defines the errata applicability to available CYT3BB/4BB family devices.

| Items                                                                                                                                                    | Errata ID | CYT3BB/4BB                                                                                                                                                                                                                                                                                                                                   | Silicon rev. | Fix status                                                                                                                                                                                                                                                                                     |
|----------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [1] CAN FD RX FIFO top pointer feature does not function as expected                                                                                     | 96        | CYT3BB5CEBQ0AESGS<br>CYT3BB5CEBQ0AEEGS<br>CYT3BB7CEBQ0AESGS<br>CYT3BB7CEBQ0AEEGS<br>CYT3BB8CEBQ0AESGS<br>CYT3BB8CEBQ0AEEGS<br>CYT3BBBCEBQ0BZSGS<br>CYT3BBBCEBQ0BZEGS<br>CYT4BB5CEBQ0AESGS<br>CYT4BB5CEBQ0AEEGS<br>CYT4BB7CEBQ0AESGS<br>CYT4BB7CEBQ0AEEGS<br>CYT4BB8CEBQ0AESGS<br>CYT4BB8CEBQ0AEEGS<br>CYT4BBBCEBQ0BZSGS<br>CYT4BBBCEBQ0BZEGS | B            | No silicon fix planned. Use workaround.                                                                                                                                                                                                                                                        |
| [2] CAN FD debug message handling state machine is not reset to Idle state when CANFD_CH_CCCR.INIT is set                                                | 97        |                                                                                                                                                                                                                                                                                                                                              |              | No silicon fix planned. Use workaround.                                                                                                                                                                                                                                                        |
| [3] Limitation of the memory hole in SCB register space                                                                                                  | 124       |                                                                                                                                                                                                                                                                                                                                              |              | No silicon fix planned. Use workaround.                                                                                                                                                                                                                                                        |
| [4] Limitation of the memory hole in Ethernet (ETH) register space                                                                                       | 128       |                                                                                                                                                                                                                                                                                                                                              |              | No silicon fix planned. Use workaround.                                                                                                                                                                                                                                                        |
| [5] CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID                                | 147       |                                                                                                                                                                                                                                                                                                                                              |              | No silicon fix planned. Use workaround.                                                                                                                                                                                                                                                        |
| [6] CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID | 167       |                                                                                                                                                                                                                                                                                                                                              |              | No silicon fix planned. Use workaround. TRM was updated.                                                                                                                                                                                                                                       |
| [7] Misleading status is returned for Flash and eFuse system calls, if there are pending NC ECC faults in SRAM controller #0                             | 175       |                                                                                                                                                                                                                                                                                                                                              |              | No silicon fix planned. TRM will be updated.                                                                                                                                                                                                                                                   |
| [8] WDT reset causes loss of SRAM retention                                                                                                              | 176       |                                                                                                                                                                                                                                                                                                                                              |              | No silicon fix planned. TRM will be updated.                                                                                                                                                                                                                                                   |
| [9] RMII TX output maximum delay spec change for GPIO_STD                                                                                                | 177       |                                                                                                                                                                                                                                                                                                                                              |              | No silicon fix planned.                                                                                                                                                                                                                                                                        |
| [10] Crypto ECC errors may be set after boot with application authentication                                                                             | 185       |                                                                                                                                                                                                                                                                                                                                              |              | No silicon fix planned. TRM will be updated.                                                                                                                                                                                                                                                   |
| [11] Incomplete erase of Code Flash cells could happen Erase Suspend / Erase Resume is used along with Erase Sector operation in Non-Blocking mode       | 198       |                                                                                                                                                                                                                                                                                                                                              |              | Will be fixed to update the Flash settings, via Manufacturing Test Program Update for Code Flash setting; this fix is transferred to TRAVEO™ T2G devices during Infineon Factory Test Flow. Fixed devices will be identified by Device Date Code, which is marked on every TRAVEO™ T2G device. |
| [12] Limitation for keeping the port state from peripheral IP after wakeup from DeepSleep                                                                | 199       |                                                                                                                                                                                                                                                                                                                                              |              | No silicon fix planned. TRM will be updated.                                                                                                                                                                                                                                                   |

### 1. CAN FD RX FIFO top pointer feature does not function as expected

|                             |                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Problem definition</b>   | RX FIFO top pointer function calculates the address for received messages in Message RAM by hardware. This address should restart back from the start address after reading all messages of RX FIFO n size (n: 0 or 1). However, the address does not restart back from the start address when RX FIFO n size is set to 1 (CANFD_CH_RXFnC.FnS = 0x01). This results in CPU/DMA reading messages from the wrong address in Message RAM. |
| <b>Parameters affected</b>  | NA                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <b>Trigger condition(s)</b> | The RX FIFO top pointer function is used when RX FIFO n size is set to 1 element (CANFD_CH_RXFnC.FnS = 0x01).                                                                                                                                                                                                                                                                                                                          |
| <b>Scope of impact</b>      | Received message cannot be correctly read by using the RX FIFO top pointer function, when RX FIFO n size is set to 1 element.                                                                                                                                                                                                                                                                                                          |
| <b>Workaround</b>           | Any of the following can be used as a workaround:<br>1) Set RX FIFO n size to 2 or more when using RX FIFO top pointer function.<br>2) Do not use the RX FIFO top pointer function when RX FIFO n size is set to 1 element. Instead of RX FIFO top pointer, read received messages from the Message RAM directly.                                                                                                                      |
| <b>Fix status</b>           | No silicon fix planned. Use workaround.                                                                                                                                                                                                                                                                                                                                                                                                |

### 2. CAN FD debug message handling state machine is not reset to Idle state when CANFD\_CH\_CCCR.INIT is set

|                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Problem definition</b>   | If either of the CANFD_CH_CCCR.INIT bits is set by the Host or when the M_TTCAN module enters Bus-off state, the debug message handling state machine stays in its current state instead of being reset to Idle state. Configuring the bit CANFD_CH_CCCR.CCE does not change CANFD_CH_RXF1S.DMS.                                                                                                                                                                                                                                                                                                              |
| <b>Parameters affected</b>  | NA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>Trigger condition(s)</b> | Either of the CANFD_CH_CCCR.INIT bits is set by the Host or when the M_TTCAN module enters Bus-off state.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <b>Scope of impact</b>      | The errata is limited to the use case when the debug on CAN functionality is active. Normal operation of the CAN module is not affected, in which case the debug message handling state machine always remains in Idle state. In the described use case, the debug message handling state machine is stopped and remains in the current state signaled by the CANFD_CH_RXF1S.DMS bit. In case CANFD_CH_RXF1S.DMS is set to 0b11, the DMA request remains active.<br>Bosch classifies this as a non-critical error with low severity, there is no fix for the IP. Bosch recommends the workaround listed here. |
| <b>Workaround</b>           | In case the debug message handling state machine has stopped while CANFD_CH_RXF1S.DMS is 0b01 or 0b10, it can be reset to Idle state by hardware reset or by reception of debug messages after CANFD_CH_CCCR.INIT is reset to zero.                                                                                                                                                                                                                                                                                                                                                                           |
| <b>Fix status</b>           | No silicon fix planned. Use workaround.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

### 3. Limitation of the memory hole in SCB register space

|                             |                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Problem definition</b>   | The memory hole [offset address: 0x1000 to 0xFFFF] inside SCB register space is not aligned to the below defined spec. The offset address bits [15:12] are ignored and treated as 4'b0000, so write/read access to offset address [0x1000 to 0xFFFF], will actually happen to [0x0000 to 0x0FFF].<br>- Access to address gaps in memory mapped space: writes are ignored and any read returns a zero. |
| <b>Parameters affected</b>  | NA                                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>Trigger condition(s)</b> | Access to the memory hole [offset address: 0x1000 to 0xFFFF] in SCB register space.                                                                                                                                                                                                                                                                                                                   |
| <b>Scope of impact</b>      | The memory hole [offset address: 0x1000 to 0xFFFF] in SCB register space is not aligned to other IP registers.                                                                                                                                                                                                                                                                                        |
| <b>Workaround</b>           | Do not access to the memory hole [offset address: 0x1000 to 0xFFFF] in SCB register space.                                                                                                                                                                                                                                                                                                            |
| <b>Fix status</b>           | No silicon fix planned.                                                                                                                                                                                                                                                                                                                                                                               |

| <b>4. Limitation of the memory hole in Ethernet (ETH) register space</b>                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Problem definition</b>                                                                                                       | <p>The memory hole [offset address: 0x2000 to 0xFFFF] in ETH register space has the below mentioned original spec. However, when accessing to address gaps within [0x1000 to 0x1FFF], the offset address bits [15:13] are ignored and treated as 3'b000, so write/read access to offset address [0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF], will actually happen to [0x1000 to 0x1FFF].</p> <ul style="list-style-type: none"> <li>- Access to address gaps within [0x0000 to 0x0FFF]: writes are ignored and any read returns a zero.</li> <li>- Access to address gaps within [0x1000 to 0x1FFF]: returns AHB ERROR.</li> </ul>                                                                                      |
| <b>Parameters affected</b>                                                                                                      | NA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>Trigger condition(s)</b>                                                                                                     | Access to the memory hole [offset address: 0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF] in ETH register space.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>Scope of impact</b>                                                                                                          | Write/read access to offset address [0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF], will actually happen to [0x1000 to 0x1FFF].                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>Workaround</b>                                                                                                               | Do not access to the memory hole [offset address: 0x3000 to 0x3FFF, 0x5000 to 0x5FFF, 0x7000 to 0x7FFF, 0x9000 to 0x9FFF, 0xB000 to 0xBFFF, 0xD000 to 0xDFFF, 0xF000 to 0xFFFF] in ETH register space.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <b>Fix status</b>                                                                                                               | No silicon fix planned.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>5. CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>Problem definition</b>                                                                                                       | <p><b>Configuration:</b><br/> Several Tx Buffers are configured with same Message ID. Transmission of these Tx Buffers is requested sequentially with a delay between the individual Tx requests.</p> <p><b>Expected behavior:</b><br/> When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests, they shall be transmitted in ascending order of their Tx Buffer numbers. The Tx Buffer with lowest buffer number and pending Tx request is transmitted first.</p> <p><b>Observed behavior:</b><br/> It may happen, depending on the delay between the individual Tx requests, that in the case where multiple Tx Buffers are configured with the same Message ID the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first).</p>    |
| <b>Parameters affected</b>                                                                                                      | NA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>Trigger condition(s)</b>                                                                                                     | When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>Scope of impact</b>                                                                                                          | In the case described it may happen, that Tx Buffers configured with the same Message ID and pending Tx request are not transmitted with lowest Tx Buffer number first (message order inversion).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <b>Workaround</b>                                                                                                               | <p>Any of the following:</p> <ol style="list-style-type: none"> <li>1) First write the group of Tx message with the same Message ID to the Message RAM and then afterwards request transmission of all these messages concurrently by a single write access to CANFDx_CHy_TXBAR. Before requesting a group of Tx messages with this Message ID ensure that no message with this Message ID has a pending Tx request.</li> <li>2) Use the Tx FIFO instead of dedicated Tx Buffers for the transmission of several messages with the same Message ID in a specific order.</li> </ol> <p>Applications not able to use workaround #1 or #2 can implement a counter within the data section of their messages sent with same ID in order to allow the recipients to determine the correct sending sequence.</p> |
| <b>Fix status</b>                                                                                                               | No silicon fix planned. Use workaround.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

| <b>6. CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Problem definition</b>                                                                                                                                      | <p>The following are the updated description in the sections "Dedicated Tx Buffers" and "Tx Queue" of the architecture TRM related to the transmission from multiple buffers configured with the same Message ID.</p> <p>Dedicated Tx buffers</p> <ul style="list-style-type: none"> <li>- TRM statement: If multiple Tx buffers are configured with the same Message ID, the Tx buffer with the lowest buffer number is transmitted first.</li> <li>- Enhancement: These Tx buffers shall be requested in ascending order with lowest buffer number first. Alternatively all Tx buffers configured with the same Message ID can be requested simultaneously by a single write access to CANFDx_CHy_TXBAR.</li> </ul> <p>Tx queue</p> <ul style="list-style-type: none"> <li>- TRM statement: If multiple queue buffers are configured with the same Message ID, the queue buffer with the lowest buffer number is transmitted first.</li> <li>- Replacement: In case that multiple Tx queue buffers are configured with the same Message ID, the transmission order depends on numbers of the buffers where the messages were stored for transmission. As these buffer numbers depend on the then current states of the PUT Index, a prediction of the transmission order is not possible.</li> <li>- TRM statement: An Add Request cyclically increments the Put Index to the next free Tx Buffer.</li> <li>- Replacement: The PUT Index always points to that free buffer of the Tx Queue with the lowest number.</li> </ul> |
| <b>Parameters affected</b>                                                                                                                                     | NA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <b>Trigger condition(s)</b>                                                                                                                                    | Using multiple dedicated Tx buffers or Tx queue buffers configured with the same Message ID.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>Scope of impact</b>                                                                                                                                         | In the case the dedicated Tx buffers with the same Message ID are not requested in ascending order or at the same time or in case of multiple Tx Queue Buffers with the same Message ID, it cannot be guaranteed, that these messages are transmitted in ascending order with lowest buffer number first.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>Workaround</b>                                                                                                                                              | In case a defined order of transmission is required the Tx FIFO shall be used for transmission of messages with the same Message ID. Alternatively dedicated Tx Buffers with the same Message ID shall be requested in ascending order with lowest buffer number first or by a single write access to CANFDx_CHy_TXBAR. Alternatively a single Tx Buffer can be used to transmit those messages one after the other.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>Fix status</b>                                                                                                                                              | No silicon fix planned. Use workaround. TRM was updated accordingly.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

| <b>7. Misleading status is returned for Flash and eFuse system calls, if there are pending NC ECC faults in SRAM controller #0</b> |                                                                                                                                                                                                                                                          |
|------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Problem Definition</b>                                                                                                          | Flash and eFuse system calls will return misleading status of 0xF0000005 ("Page is write protected") even for non-protected row, or 0xF0000002 ("Invalid eFuse address") for valid eFuse address in case of pending NC ECC faults in SRAM controller #0. |
| <b>Parameters Affected</b>                                                                                                         | Return status of Flash and eFuse system calls.                                                                                                                                                                                                           |
| <b>Trigger Condition(s)</b>                                                                                                        | NC ECC fault(s) pending in SRAM controller #0 and SWPUs are populated in the design.                                                                                                                                                                     |
| <b>Scope of Impact</b>                                                                                                             | Flash and eFuse system calls will not work until the NC ECC fault(s) pending in SRAM controller #0 is/are properly handled.                                                                                                                              |
| <b>Workaround</b>                                                                                                                  | If the NC ECC fault(s) are not due to HW malfunction (i.e. if the faults are due to usage of non-initialized SRAM or improper SRAM initialization), then clearing of these pending faults will resolve the issue.                                        |
| <b>Fix Status</b>                                                                                                                  | No silicon fix planned. TRM will be updated.                                                                                                                                                                                                             |

| <b>8. WDT reset causes loss of SRAM retention</b> |                                                                                                                                                                                                                                              |
|---------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Problem Definition</b>                         | Architecture TRM Table on “Reset Cause Distribution” shows that, the WDT reset can retain SRAM if there is an orderly shutdown of the SRAM only during a warning interrupt. However, this is wrong. WDT reset causes loss of SRAM retention. |
| <b>Parameters Affected</b>                        | NA                                                                                                                                                                                                                                           |
| <b>Trigger Condition(s)</b>                       | WDT reset                                                                                                                                                                                                                                    |
| <b>Scope of Impact</b>                            | WDT reset causes loss of SRAM retention.                                                                                                                                                                                                     |
| <b>Workaround</b>                                 | None                                                                                                                                                                                                                                         |
| <b>Fix Status</b>                                 | No silicon fix planned. TRM will be updated.                                                                                                                                                                                                 |

| <b>9. RMII TX output maximum delay spec change for GPIO_STD</b> |                                                                                                                                                                                                         |
|-----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Problem Definition</b>                                       | RMII TX output maximum delay specification has been changed from 14 ns to 14.6 ns for GPIO_STD.                                                                                                         |
| <b>Parameters Affected</b>                                      | SID393                                                                                                                                                                                                  |
| <b>Trigger Condition(s)</b>                                     | Using GPIO_STD as RMII                                                                                                                                                                                  |
| <b>Scope of Impact</b>                                          | This spec change will cause that the PCB delay budget between MCU and PHY cut down to 1.4 ns from 2 ns. [PCB delay budget = REF_CLK period (e.g. 20 ns) – SID393 (14.6 ns) – PHY RXD setup (e.g. 4 ns)] |
| <b>Workaround</b>                                               | None                                                                                                                                                                                                    |
| <b>Fix Status</b>                                               | No silicon fix planned.                                                                                                                                                                                 |

| <b>10. Crypto ECC errors may be set after boot with application authentication</b> |                                                                                                                                                                                                                           |
|------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Problem Definition</b>                                                          | Due to the improper initialization of the Crypto memory buffer, Crypto ECC errors may be set after boot with application authentication. In spite of the Crypto ECC errors, the result of the authentication is reliable. |
| <b>Parameters Affected</b>                                                         | N/A                                                                                                                                                                                                                       |
| <b>Trigger Condition(s)</b>                                                        | Boot device with application authentication.                                                                                                                                                                              |
| <b>Scope of Impact</b>                                                             | Crypto ECC errors may be set after boot with application authentication.                                                                                                                                                  |
| <b>Workaround</b>                                                                  | Clear or ignore Crypto ECC errors which were generated during boot with application authentication.                                                                                                                       |
| <b>Fix Status</b>                                                                  | No silicon fix planned. TRM will be updated.                                                                                                                                                                              |

| <b>11. Incomplete erase of Code Flash cells could happen Erase Suspend / Erase Resume is used along with Erase Sector operation in Non-Blocking mode</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Problem Definition</b>                                                                                                                                | Code Flash memory can be erased in “Non-Blocking” mode; a Non-Blocking mode supported option allows users to suspend an ongoing erase sector operation. When an ongoing erase operation is interrupted using “Erase Suspend” and “Erase Resume”, Flash cells may not have been erased completely, even after the erase operation complete is indicated by FLASHC_STATUS register. Only Code Flash is impacted by this issue; Work Flash and Supervisory Flash (SFlash) are not impacted. |
| <b>Parameters Affected</b>                                                                                                                               | N/A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <b>Trigger Condition(s)</b>                                                                                                                              | Using EraseSector System Call in Non-Blocking mode for CM0+ to erase Code Flash and the ongoing erase operation is interrupted using EraseSuspend and EraseResume System calls.                                                                                                                                                                                                                                                                                                          |
| <b>Scope of Impact</b>                                                                                                                                   | When Code Flash sectors are erased in Non-Blocking mode and the ongoing erase operation is interrupted by Erase Suspend / Erase Resume, it cannot be guaranteed that the Code Flash cells are fully erased. Any read on the Code Flash area after the erase is complete or read on the programmed data after ProgramRow is complete can trigger ECC errors.                                                                                                                              |

Errata

|                   |                                                                                                                                                                                                                                                                                                                                                                                           |
|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Workaround</b> | Use any of the following:<br>1) User can use Non-Blocking mode for EraseSector, but must not interrupt the erase operation using Erase Suspend / Erase Resume.<br>2) If a Code Flash sector erase operation is interrupted using Erase Suspend / Erase Resume, then erase the same sector again without Erase Suspend / Erase Resume before reading the sector or programming the sector. |
| <b>Fix Status</b> | Will be fixed to update the Flash settings, via Manufacturing Test Program Update for Code Flash setting; this fix is transferred to TRAVEO™ T2G devices during Infineon Factory Test Flow. Fixed devices will be identified by Device Date Code, which is marked on every TRAVEO™ T2G device.                                                                                            |

| <b>12.Limitation for keeping the port state from peripheral IP after wakeup from DeepSleep</b> |                                                                                                                                                                                                                                                                                                                                                                     |
|------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Problem Definition</b>                                                                      | The port state is not retained when the port selects peripheral IP (except for LIN or CAN FD) and MCU wakes up from DeepSleep.                                                                                                                                                                                                                                      |
| <b>Parameters Affected</b>                                                                     | N/A                                                                                                                                                                                                                                                                                                                                                                 |
| <b>Trigger Condition(s)</b>                                                                    | The port selects peripherals (except for LIN or CAN-FD), and MCU wakes up from DeepSleep.                                                                                                                                                                                                                                                                           |
| <b>Scope of Impact</b>                                                                         | Unexpected port output change might affect user system.                                                                                                                                                                                                                                                                                                             |
| <b>Workaround</b>                                                                              | If the port selects peripherals (except for LIN or CAN FD), and the port output value needed to be maintained after wakeup from DeepSleep, set HSIOM_PRTx_PORT_SEL.IOy_SEL = 0 (GPIO) before DeepSleep and set the required output value in GPIO configuration registers. After wakeup, change HSIOM_PRTx_PORT_SEL.IOy_SEL back to the peripheral module as needed. |
| <b>Fix Status</b>                                                                              | No silicon fix planned. TRM will be updated to add above workaround.                                                                                                                                                                                                                                                                                                |

## Revision history

| Document revision | Date       | Description of changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| **                | 2019-03-27 | New datasheet                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| *A                | 2019-07-23 | Updated <a href="#">Features list</a> , <a href="#">CYT3BB/4BB address map</a> , <a href="#">Peripheral I/O map</a> .<br>Updated <a href="#">Pin assignment</a> , <a href="#">Alternate function pin assignments</a> .<br>Updated Trigger Group tables.<br>Updated <a href="#">Peripheral clocks</a> and <a href="#">Peripheral protection unit fixed structure pairs</a> .<br>Updated <a href="#">Bus masters</a> and <a href="#">Miscellaneous configuration</a> .<br>Updated <a href="#">Electrical specifications</a> .<br>Updated <a href="#">Reset sequence</a> and SPI Diagrams.<br>Added <a href="#">Table 26-20</a> .<br>Updated <a href="#">Ordering information</a> and <a href="#">Packaging</a> . |
| *B                | 2019-09-06 | Updated <a href="#">Functional description</a> .<br>Updated <a href="#">Peripheral I/O map</a> .<br>Updated <a href="#">Pin assignment</a> .<br>Updated <a href="#">Alternate function pin assignments</a> and <a href="#">Power pin assignments</a> .<br>Updated <a href="#">Miscellaneous configuration</a> .<br>Updated <a href="#">Development support</a> .<br>Updated <a href="#">Electrical specifications</a> .<br>Updated <a href="#">Ordering information</a> .<br>Updated <a href="#">Packaging</a> .                                                                                                                                                                                               |
| *C                | 2019-11-15 | Updated Ethernet MAC in <a href="#">Features list</a> .<br>Updated SRAM details in <a href="#">CYT3BB/4BB address map</a> .<br>Added <a href="#">Bootloading or End-of-line (EoL) Programming</a> .<br>Updated values of the following SIDs: 676B, 26C, 33C, 33D, 333, 216, 342A1, 342D1 to 345D1, 345E1, 342E1, 342, 343, 344, 345A1, 345, 342B1, 342A, 780C, 782C, 190A to 231A, 342E1, 679B, 683B, 342D1, 343D1, 344D1, 345E1, 345D1, 748B/C, 749B, 706/A                                                                                                                                                                                                                                                   |
| *D                | 2020-05-04 | Updated <a href="#">Features list</a> .<br>Updated <a href="#">Functional description</a> .<br>Updated <a href="#">Power pin assignments</a> .<br>Updated <a href="#">Alternate function pin assignments</a> .<br>Updated <a href="#">Fault assignments</a> .<br>Updated ECO spec from 3.988 MHz to 8 MHz.<br>Updated <a href="#">Electrical specifications</a> .<br>Updated <a href="#">Ordering information</a> .                                                                                                                                                                                                                                                                                            |
| *E                | 2020-09-23 | Updated <a href="#">Features</a> and <a href="#">Features list</a> .<br>Updated <a href="#">Regulators</a> .<br>Updated <a href="#">Clock system</a> .<br>Updated <a href="#">Peripheral I/O map</a> .<br>Updated <a href="#">Pin function description</a> .<br>Updated <a href="#">Smoothing capacitor should be placed as close as possible to the VCCD pin..</a><br>Updated <a href="#">Packaging</a> .<br>Updated <a href="#">Appendix</a> .<br>Added <a href="#">Errata</a><br>Updated <a href="#">Electrical specifications</a> .<br>Please refer to Revision history change log.                                                                                                                        |

## Revision history

| Document revision | Date       | Description of changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| *F                | 2021-10-27 | Updated <a href="#">Features</a><br>Updated <a href="#">Clock system</a><br>Updated <a href="#">Power modes</a><br>Updated <a href="#">Audio interface</a><br>Updated <a href="#">I/Os</a><br>Updated <a href="#">Pin assignment</a><br>Updated <a href="#">High-speed I/O matrix connections</a><br>Updated <a href="#">Alternate function pin assignments</a><br>Updated <a href="#">Interrupts and wake-up assignments</a><br>Updated <a href="#">Faults</a><br>Updated <a href="#">Bus masters</a><br>Updated <a href="#">Electrical specifications</a><br>Updated <a href="#">Part number nomenclature</a><br>Updated <a href="#">Errata</a> |
| *G                | 2022-02-18 | Updated <a href="#">System resources</a> .<br>Updated <a href="#">Serial memory interface specifications</a> .<br>Updated <a href="#">Part number nomenclature</a> .<br>Updated TQFP package diagrams.<br>Updated <a href="#">Errata</a> .                                                                                                                                                                                                                                                                                                                                                                                                        |
| *H                | 2022-09-08 | Updated <a href="#">Functional description</a> .<br>Updated <a href="#">Peripheral I/O map</a> .<br>Updated <a href="#">Electrical specifications</a> .<br>Updated <a href="#">Errata</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

## Revision history change log

### Rev. \*H Section updates

| Section                                 | Change Description           | Current Spec (002-26591 Rev. *G)                                                                                                                                                                                                                                                                                                                                     | New Spec (002-26591 Rev. *H)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Reason for change |
|-----------------------------------------|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|
| 3.2.2.2 Core internal                   | Updated current value        | 280 mA                                                                                                                                                                                                                                                                                                                                                               | 300 mA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Corrected         |
| 3.3.9 External memory interface         | Updated description          | (single, dual, quad, or octal SPI at up to 90 MHz)                                                                                                                                                                                                                                                                                                                   | (single, dual, quad, or octal SPI)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Corrected         |
| Table 6-1 CYT3BB/4BB peripheral I/O map | Updated TCPWM base addresses | 0x4038 0000<br>0x4038 8000<br>0x4039 0000                                                                                                                                                                                                                                                                                                                            | 0x4058 0000<br>0x4058 8000<br>0x4059 0000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Corrected         |
| SID40<br>(Power supply voltage)         | Updated Note                 | [57]: 5.0 V ±10% is supported with a higher OVD setting option for VDDD and VDDA. This setting provides robust protection for internal and interface timing, but OVD reset occurs at a voltage above the specified operating conditions. A lower OVD setting option is available (consistent with up to 5.0 V) and guarantees that all operating conditions are met. | [57]: 5.0 V ±10% is supported with a higher OVD setting option for VDDD and VDDA. This setting provides robust protection for internal and interface timing, but OVD reset occurs at a voltage above the specified operating conditions. A lower OVD setting option is available (consistent with up to 5.0 V) and guarantees that all operating conditions are met. Voltage overshoot to a higher OVD setting range for VDDD and VDDA is permissible, provided the duration is less than 2 hours cumulated. Note that during overshoot voltage condition electrical parameters are not guaranteed. | Corrected         |
| 26.11 Clock specifications              | Updated table                | (none)                                                                                                                                                                                                                                                                                                                                                               | - Addition of FLL source<br>- Maximum permitted clock frequency setting for both PLL and FLL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Improvement       |
| 31. Errata                              | Added errata                 | (none)                                                                                                                                                                                                                                                                                                                                                               | Added errata ID 185, 198, 199                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | New addition      |

#### Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2022-09-08**  
**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**

**© 2022 Infineon Technologies AG.**  
**All Rights Reserved.**

**Do you have a question about this document?**

Go to [www.infineon.com/support](http://www.infineon.com/support)

**Document reference**  
**002-26591 Rev. \*H**

#### IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenhheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office ([www.infineon.com](http://www.infineon.com)).

#### WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.