

# ANTREX Electronics

Electronic Components Sourcing Information

---

## Product Reference Information

|                      |                                |
|----------------------|--------------------------------|
| <b>Part Number:</b>  | CY2304SXC-2T                   |
| <b>Manufacturer:</b> | Infineon Technologies          |
| <b>Package:</b>      | 8-SOIC (0.154" , 3.90mm Width) |
| <b>Availability:</b> | Please confirm with sales      |

### Product Page:

<https://antrexco.com/product/details/infineon-technologies/cy2304sxc-2t.html>

### Request a Quote:

[Submit RFQ for this part](#)



Scan for product page

## Contact Information

Email: [info@antrexco.com](mailto:info@antrexco.com)

WhatsApp: +86-186-8066-5326

Website: <https://antrexco.com>

## Quality & Trust

New & Original Components

Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

Secure sourcing support for OEM / EMS projects

### Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

---



**Please note that Cypress is an Infineon Technologies Company.**

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

**Continuity of document content**

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

**Continuity of ordering part numbers**

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

## 3.3 V Zero Delay Buffer

### Features

- Zero input-output propagation delay, adjustable by capacitive load on FBK input
- Multiple configurations
- Multiple low-skew outputs
- 10 MHz to 133 MHz operating range
- 90 ps typical peak cycle-to-cycle jitter at 15 pF, 66 MHz
- Space-saving 8-pin 150-mil small outline integrated circuit (SOIC) package
- 3.3 V operation
- Industrial temperature available

### Functional Description

The CY2304 is a 3.3 V zero delay buffer designed to distribute high-speed clocks in PC, workstation, datacom, telecom, and other high performance applications.

The part has an on-chip phase-locked loop (PLL) that locks to an input clock presented on the REF pin. The PLL feedback is

required to be driven into the FBK pin, and can be obtained from one of the outputs. The input-to-output skew is guaranteed to be less than 250 ps, and output-to-output skew is guaranteed to be less than 200 ps.

The CY2304 has two banks of two outputs each.

The CY2304 PLL enters a power down state when there are no rising edges on the REF input. In this mode, all outputs are three-stated and the PLL is turned off, resulting in less than 25  $\mu$ A of current draw.

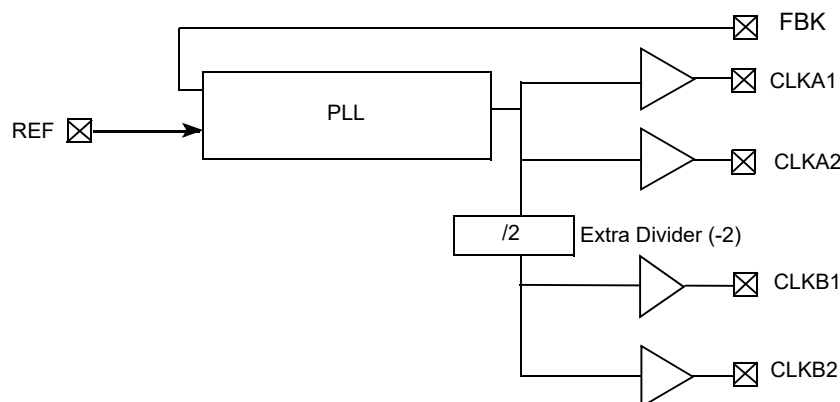
Multiple CY2304 devices can accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is guaranteed to be less than 500 ps.

The CY2304 is available in two different configurations, as shown in [Available Configurations](#). The CY2304-1 is the base part, where the output frequencies equal the reference if there is no counter in the feedback path.

The CY2304-2 allows the user to obtain Ref and 1/2x or 2x frequencies on each output bank. The exact configuration and output frequencies depends on which output drives the feedback pin.

For a complete list of related documentation, click [here](#).

### Logic Block Diagram



### Available Configurations

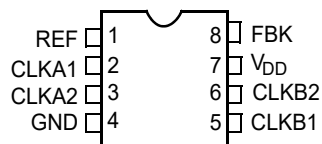
| Device   | FBK from    | Bank A Frequency | Bank B Frequency |
|----------|-------------|------------------|------------------|
| CY2304-1 | Bank A or B | Reference        | Reference        |
| CY2304-2 | Bank A      | Reference        | Reference/2      |
| CY2304-2 | Bank B      | 2 × Reference    | Reference        |

## Contents

|                                          |           |                                                      |           |
|------------------------------------------|-----------|------------------------------------------------------|-----------|
| <b>Pin Configurations</b> .....          | <b>3</b>  | <b>Acronyms</b> .....                                | <b>13</b> |
| <b>Pin Definitions</b> .....             | <b>3</b>  | <b>Document Conventions</b> .....                    | <b>13</b> |
| <b>Zero Delay and Skew Control</b> ..... | <b>4</b>  | Units of Measure .....                               | 13        |
| <b>Maximum Ratings</b> .....             | <b>5</b>  | <b>Appendix: Silicon Errata for the Zero Delay</b>   |           |
| <b>Operating Conditions</b> .....        | <b>5</b>  | <b>Clock Buffers, CY2304</b> .....                   | <b>14</b> |
| <b>Electrical Characteristics</b> .....  | <b>5</b>  | Part Numbers Affected .....                          | 14        |
| <b>Switching Characteristics</b> .....   | <b>6</b>  | CY2304 Errata Summary .....                          | 14        |
| <b>Operating Conditions</b> .....        | <b>7</b>  | CY2303 Qualification Status of fixed silicon .....   | 14        |
| <b>Electrical Characteristics</b> .....  | <b>7</b>  | <b>Document History Page</b> .....                   | <b>16</b> |
| <b>Thermal Resistance</b> .....          | <b>8</b>  | <b>Sales, Solutions, and Legal Information</b> ..... | <b>17</b> |
| <b>Test Circuit</b> .....                | <b>8</b>  | Worldwide Sales and Design Support .....             | 17        |
| <b>Switching Characteristics</b> .....   | <b>9</b>  | Products .....                                       | 17        |
| <b>Switching Waveforms</b> .....         | <b>10</b> | PSoC® Solutions .....                                | 17        |
| <b>Ordering Information</b> .....        | <b>11</b> | Cypress Developer Community .....                    | 17        |
| Ordering Code Definitions .....          | 11        | Technical Support .....                              | 17        |
| <b>Package Diagram</b> .....             | <b>12</b> |                                                      |           |

## Pin Configurations

Figure 1. 8-pin SOIC pinout



## Pin Definitions

8-pin SOIC

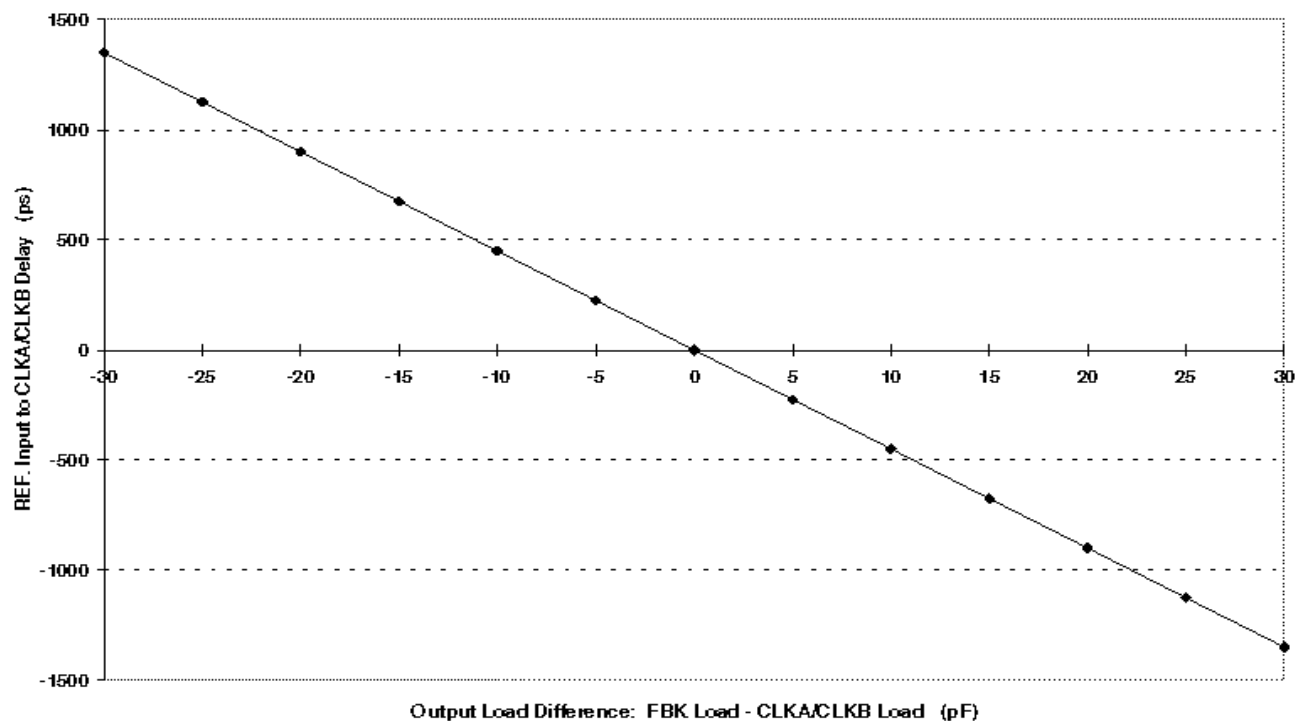
| Pin | Signal               | Description                                   |
|-----|----------------------|-----------------------------------------------|
| 1   | REF <sup>[1]</sup>   | Input reference frequency, 5 V tolerant input |
| 2   | CLKA1 <sup>[2]</sup> | Clock output, Bank A                          |
| 3   | CLKA2 <sup>[2]</sup> | Clock output, Bank A                          |
| 4   | GND                  | Ground                                        |
| 5   | CLKB1 <sup>[2]</sup> | Clock output, Bank B                          |
| 6   | CLKB2 <sup>[2]</sup> | Clock output, Bank B                          |
| 7   | V <sub>DD</sub>      | 3.3 V supply                                  |
| 8   | FBK                  | PLL feedback input                            |

### Notes

1. Weak pull-down.
2. Weak pull-down on all outputs.

## Zero Delay and Skew Control

Figure 2. REF. Input to CLKA/CLKB Delay vs. Difference in Loading Between FBK Pin and CLKA/CLKB Pins



To close the feedback loop of the CY2304, the FBK pin can be driven from any of the four available output pins. The output driving the FBK pin is driving a total load of 7 pF, with any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input-output delay. This is shown in [Figure 2](#).

For applications requiring zero input-output delay, all outputs including the one providing feedback must be equally loaded. If input-output delay adjustments are required, use the graph shown in [Figure 2](#) to calculate loading differences between the feedback output and remaining outputs.

For zero output-output skew, be sure to load outputs equally. For further information on using CY2304, refer to the application note [AN1234 - Understanding Cypress's Zero Delay Buffers](#).

## Maximum Ratings

Supply voltage to ground potential ..... -0.5 V to +7.0 V  
 DC input voltage (except Ref) ..... -0.5 V to  $V_{DD} + 0.5$  V  
 DC input voltage REF ..... -0.5 V to 7 V

Storage temperature ..... -65 °C to +150 °C  
 Junction temperature ..... 150 °C  
 Static discharge voltage  
 (per MIL-STD-883, Method 3015) ..... > 2000 V

## Operating Conditions

For CY2304SXC Commercial Temperature Devices

| Parameter | Description                                                                                         | Min  | Max | Unit |
|-----------|-----------------------------------------------------------------------------------------------------|------|-----|------|
| $V_{DD}$  | Supply voltage                                                                                      | 3.0  | 3.6 | V    |
| $T_A$     | Operating temperature (ambient temperature)                                                         | 0    | 70  | °C   |
| $C_L$     | Load capacitance (below 100 MHz)                                                                    | —    | 30  | pF   |
|           | Load capacitance (from 100 MHz to 133 MHz)                                                          | —    | 15  | pF   |
| $C_{IN}$  | Input capacitance [3]                                                                               | —    | 7   | pF   |
| $t_{PU}$  | Power-up time for all $V_{DD}$ s to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | 50  | ms   |

## Electrical Characteristics

For CY2304SXC Commercial Temperature Devices

| Parameter          | Description               | Test Conditions                                                 | Min | Max   | Unit |
|--------------------|---------------------------|-----------------------------------------------------------------|-----|-------|------|
| $V_{IL}$           | Input LOW voltage         |                                                                 | —   | 0.8   | V    |
| $V_{IH}$           | Input HIGH voltage        |                                                                 | 2.0 | —     | V    |
| $I_{IL}$           | Input LOW current         | $V_{IN} = 0$ V                                                  | —   | 50.0  | μA   |
| $I_{IH}$           | Input HIGH current        | $V_{IN} = V_{DD}$                                               | —   | 100.0 | μA   |
| $V_{OL}$           | Output LOW voltage [4]    | $I_{OL} = 8$ mA (-1, -2)                                        | —   | 0.4   | V    |
| $V_{OH}$           | Output HIGH voltage [4]   | $I_{OH} = -8$ mA (-1, -2)                                       | 2.4 | —     | V    |
| $I_{DD}$ (PD mode) | Power-down supply current | REF = 0 MHz                                                     | —   | 12.0  | μA   |
| $I_{DD}$           | Supply current            | Unloaded outputs, 100 MHz REF, Select inputs at $V_{DD}$ or GND | —   | 45.0  | mA   |
|                    |                           | Unloaded outputs, 66 MHz REF (-1, -2)                           | —   | 32.0  | mA   |
|                    |                           | Unloaded outputs, 33 MHz REF (-1, -2)                           | —   | 18.0  | mA   |

### Notes

- Applies to both REF clock and FBK.
- Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Switching Characteristics

For CY2304SXC Commercial Temperature Devices

| Parameter <sup>[5]</sup> | Name                                                       | Test Conditions                                                 | Min  | Typ  | Max       | Unit |
|--------------------------|------------------------------------------------------------|-----------------------------------------------------------------|------|------|-----------|------|
| $t_1$                    | Output frequency                                           | 30 pF load, all devices                                         | 10   | —    | 100       | MHz  |
| $t_1$                    | Output frequency                                           | 15 pF load, -1, -2 devices                                      | 10   | —    | 133.3     | MHz  |
| $t_{DC}$                 | Duty cycle <sup>[6]</sup> = $t_2 \div t_1$ (-1, -2)        | Measured at 1.4 V,<br>$F_{OUT} = 66.66$ MHz, 30-pF load         | 40.0 | 50.0 | 60.0      | %    |
| $t_{DC}$                 | Duty cycle <sup>[6]</sup> = $t_2 \div t_1$ (-2)            | Measured at 1.4 V,<br>$F_{OUT} = 83.0$ MHz, 15-pF load          | 40.0 | 50.0 | 60.0      | %    |
| $t_{DC}$                 | Duty cycle <sup>[6]</sup> = $t_2 \div t_1$ (-1, -2)        | Measured at 1.4 V,<br>$F_{OUT} < 50$ MHz, 15-pF load            | 45.0 | 50.0 | 55.0      | %    |
| $t_3$                    | Rise time <sup>[6]</sup> (-1, -2)                          | Measured between 0.8 V and 2.0 V,<br>30-pF load                 | —    | —    | 2.20      | ns   |
| $t_3$                    | Rise time <sup>[6]</sup> (-1, -2)                          | Measured between 0.8 V and 2.0 V,<br>15-pF load                 | —    | —    | 1.50      | ns   |
| $t_4$                    | Fall time <sup>[6]</sup> (-1, -2)                          | Measured between 0.8 V and 2.0 V,<br>30-pF load                 | —    | —    | 2.20      | ns   |
| $t_4$                    | Fall time <sup>[6]</sup> (-1, -2)                          | Measured between 0.8 V and 2.0 V,<br>15 pF load                 | —    | —    | 1.50      | ns   |
| $t_5$                    | Output-to-output skew on same Bank (-1, -2) <sup>[6]</sup> | All outputs equally loaded                                      | —    | —    | 200       | ps   |
|                          | Output bank A to output bank B skew (-1)                   | All outputs equally loaded                                      | —    | —    | 200       | ps   |
|                          | Output bank A to output bank B skew (-2)                   | All outputs equally loaded                                      | —    | —    | 400       | ps   |
| $t_6$                    | Skew, REF rising edge to FBK rising edge <sup>[6]</sup>    | Measured at $V_{DD}/2$                                          | —    | 0    | $\pm 250$ | ps   |
| $t_7$                    | Device-to-device skew <sup>[6]</sup>                       | Measured at $V_{DD}/2$ on the FBK pins of devices               | —    | 0    | 500       | ps   |
| $t_J$                    | Cycle-to-cycle jitter <sup>[6]</sup> (-1)                  | Measured at 66.67 MHz, loaded outputs, 15-pF load               | —    | 90   | 175       | ps   |
|                          |                                                            | Measured at 66.67 MHz, loaded outputs, 30-pF load               | —    | —    | 200       | ps   |
|                          |                                                            | Measured at 133.3 MHz, loaded outputs, 15-pF load               | —    | —    | 100       | ps   |
| $t_J$                    | Cycle-to-cycle jitter <sup>[6]</sup> (-2)                  | Measured at 66.67 MHz, loaded outputs 30-pF load                | —    | —    | 400       | ps   |
|                          |                                                            | Measured at 66.67 MHz, loaded outputs 15-pF load                | —    | —    | 375       | ps   |
| $t_{LOCK}$               | PLL lock time <sup>[6]</sup>                               | Stable power supply, valid clocks presented on REF and FBK pins | —    | —    | 1.0       | ms   |

### Notes

5. All parameters are specified with loaded output.
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Operating Conditions

For CY2304SXI Industrial Temperature Devices

| Parameter | Description                                 | Min | Max | Unit |
|-----------|---------------------------------------------|-----|-----|------|
| $V_{DD}$  | Supply voltage                              | 3.0 | 3.6 | V    |
| $T_A$     | Operating temperature (ambient temperature) | -40 | 85  | °C   |
| $C_L$     | Load capacitance (below 100 MHz)            | –   | 30  | pF   |
|           | Load capacitance (from 100 MHz to 133 MHz)  | –   | 15  | pF   |
| $C_{IN}$  | Input capacitance                           | –   | 7   | pF   |

## Electrical Characteristics

For CY2304SXI Industrial Temperature Devices

| Parameter          | Description                        | Test Conditions                                             | Min | Max   | Unit |
|--------------------|------------------------------------|-------------------------------------------------------------|-----|-------|------|
| $V_{IL}$           | Input LOW voltage                  |                                                             | –   | 0.8   | V    |
| $V_{IH}$           | Input HIGH voltage                 |                                                             | 2.0 | –     | V    |
| $I_{IL}$           | Input LOW current                  | $V_{IN} = 0$ V                                              | –   | 50.0  | μA   |
| $I_{IH}$           | Input HIGH current                 | $V_{IN} = V_{DD}$                                           | –   | 100.0 | μA   |
| $V_{OL}$           | Output LOW voltage <sup>[7]</sup>  | $I_{OL} = 8$ mA (-1, -2)                                    | –   | 0.4   | V    |
| $V_{OH}$           | Output HIGH voltage <sup>[7]</sup> | $I_{OH} = -8$ mA (-1, -2)                                   | 2.4 | –     | V    |
| $I_{DD}$ (PD mode) | Power-down supply current          | REF = 0 MHz                                                 | –   | 25.0  | μA   |
| $I_{DD}$           | Supply current                     | Unloaded outputs, 100 MHz, Select inputs at $V_{DD}$ or GND | –   | 45.0  | mA   |
|                    |                                    | Unloaded outputs, 66 MHz REF (-1, -2)                       | –   | 35.0  | mA   |
|                    |                                    | Unloaded outputs, 33 MHz REF (-1, -2)                       | –   | 20.0  | mA   |

### Note

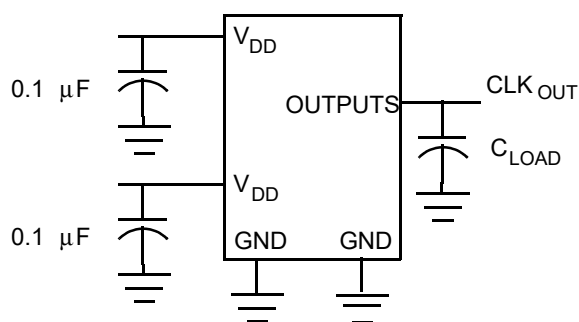
7. Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Thermal Resistance

| Parameter <sup>[8]</sup> | Description                              | Test Conditions                                                                                                             | 8-pin SOIC | Unit |
|--------------------------|------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|------------|------|
| $\theta_{JA}$            | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 140        | °C/W |
| $\theta_{JC}$            | Thermal resistance (junction to case)    |                                                                                                                             | 54         | °C/W |

## Test Circuit

Figure 3. Test Circuit # 1



Test circuit for all parameters

### Note

8. These parameters are guaranteed by design and are not tested.

## Switching Characteristics

for CY2304SXI Industrial Temperature Devices

| Parameter <sup>[9]</sup> | Name                                                        | Test Conditions                                                 | Min  | Typ  | Max       | Unit |
|--------------------------|-------------------------------------------------------------|-----------------------------------------------------------------|------|------|-----------|------|
| $t_1$                    | Output frequency                                            | 30-pF load, All devices                                         | 10   | –    | 100       | MHz  |
| $t_1$                    | Output frequency                                            | 15-pF load, All devices                                         | 10   | –    | 133.3     | MHz  |
| $t_{DC}$                 | Duty cycle <sup>[10]</sup> = $t_2 \div t_1$ (-1, -2)        | Measured at 1.4 V, $F_{OUT} = 66.66$ MHz, 30-pF load            | 40.0 | 50.0 | 60.0      | %    |
| $t_{DC}$                 | Duty cycle <sup>[10]</sup> = $t_2 \div t_1$ (-2)            | Measured at 1.4 V, $F_{OUT} = 83.0$ MHz, 15-pF load             | 40.0 | 50.0 | 60.0      | %    |
| $t_{DC}$                 | Duty cycle <sup>[10]</sup> = $t_2 \div t_1$ (-1, -2)        | Measured at 1.4 V, $F_{OUT} < 50$ MHz, 15-pF load               | 45.0 | 50.0 | 55.0      | %    |
| $t_3$                    | Rise time <sup>[10]</sup> (-1, -2)                          | Measured between 0.8 V and 2.0 V, 30-pF load                    | –    | –    | 2.50      | ns   |
| $t_3$                    | Rise time <sup>[10]</sup> (-1, -2)                          | Measured between 0.8 V and 2.0 V, 15-pF load                    | –    | –    | 1.50      | ns   |
| $t_4$                    | Fall time <sup>[10]</sup> (-1, -2)                          | Measured between 0.8 V and 2.0 V, 30-pF load                    | –    | –    | 2.50      | ns   |
| $t_4$                    | Fall time <sup>[10]</sup> (-1, -2)                          | Measured between 0.8 V and 2.0 V, 15-pF load                    | –    | –    | 1.50      | ns   |
| $t_5$                    | Output-to-output skew on same bank (-1, -2) <sup>[10]</sup> | All outputs equally loaded                                      | –    | –    | 200       | ps   |
|                          | Output bank A to output bank B skew (-1)                    | All outputs equally loaded                                      | –    | –    | 200       | ps   |
|                          | Output bank A to output bank B skew (-2)                    | All outputs equally loaded                                      | –    | –    | 400       | ps   |
| $t_6$                    | Skew, REF rising edge to FBK rising edge <sup>[10]</sup>    | Measured at $V_{DD}/2$                                          | –    | 0    | $\pm 250$ | ps   |
| $t_7$                    | Device-to-device skew <sup>[10]</sup>                       | Measured at $V_{DD}/2$ on the FBK pins of devices               | –    | 0    | 500       | ps   |
| $t_J$                    | Cycle-to-cycle jitter <sup>[10]</sup> (-1)                  | Measured at 66.67 MHz, loaded outputs, 15-pF load               | –    | –    | 180       | ps   |
|                          |                                                             | Measured at 66.67 MHz, loaded outputs, 30-pF load               | –    | –    | 200       | ps   |
|                          |                                                             | Measured at 133.3 MHz, loaded outputs, 15-pF load               | –    | –    | 100       | ps   |
| $t_J$                    | Cycle-to-cycle jitter <sup>[10]</sup> (-2)                  | Measured at 66.67 MHz, loaded outputs, 30-pF load               | –    | –    | 400       | ps   |
|                          |                                                             | Measured at 66.67 MHz, loaded outputs, 15-pF load               | –    | –    | 380       | ps   |
| $t_{LOCK}$               | PLL lock time <sup>[10]</sup>                               | Stable power supply, valid clocks presented on REF and FBK pins | –    | –    | 1.0       | ms   |

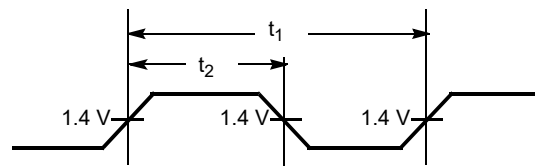
### Notes

9. All parameters are specified with loaded output.

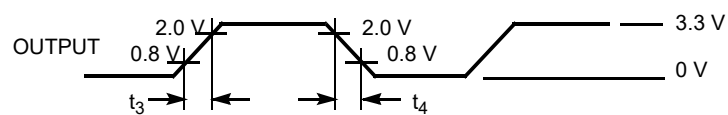
10. Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Switching Waveforms

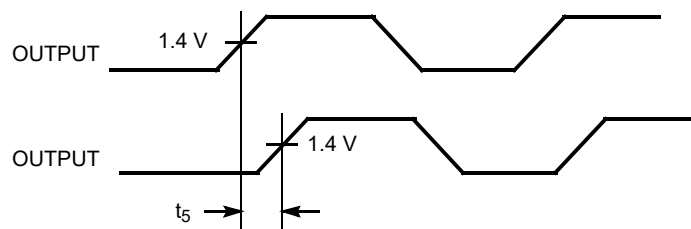
**Figure 4. Duty Cycle Timing**



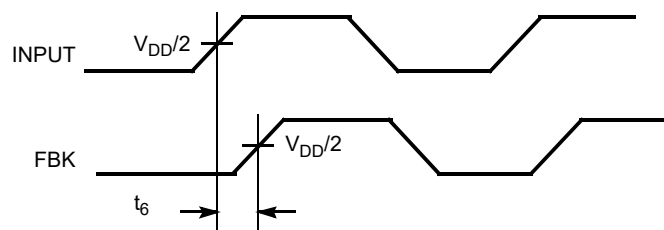
**Figure 5. All Outputs Rise/Fall Time**



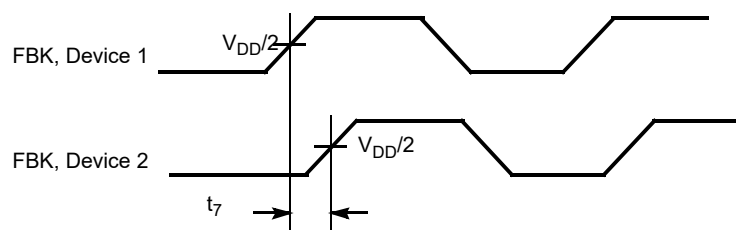
**Figure 6. Output-Output Skew**



**Figure 7. Input-Output Skew**



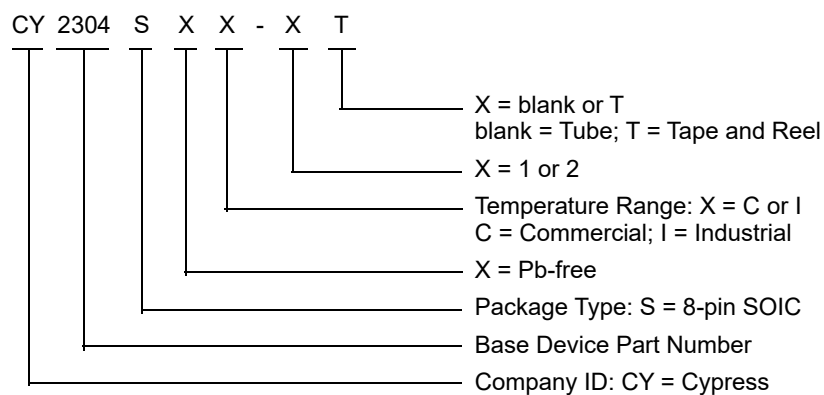
**Figure 8. Device-Device Skew**



## Ordering Information

| Ordering Code  | Package Type                          | Operating Range |
|----------------|---------------------------------------|-----------------|
| <b>Pb-free</b> |                                       |                 |
| CY2304SXC-1    | 8-pin SOIC (150 Mils)                 | Commercial      |
| CY2304SXC-1T   | 8-pin SOIC (150 Mils) – Tape and Reel | Commercial      |
| CY2304SXI-1    | 8-pin SOIC (150 Mils)                 | Industrial      |
| CY2304SXI-1T   | 8-pin SOIC (150 Mils) – Tape and Reel | Industrial      |
| CY2304SXC-2    | 8-pin SOIC (150 Mils)                 | Commercial      |
| CY2304SXC-2T   | 8-pin SOIC (150 Mils) – Tape and Reel | Commercial      |
| CY2304SXI-2    | 8-pin SOIC (150 Mils)                 | Industrial      |
| CY2304SXI-2T   | 8-pin SOIC (150 Mils) – Tape and Reel | Industrial      |

## Ordering Code Definitions

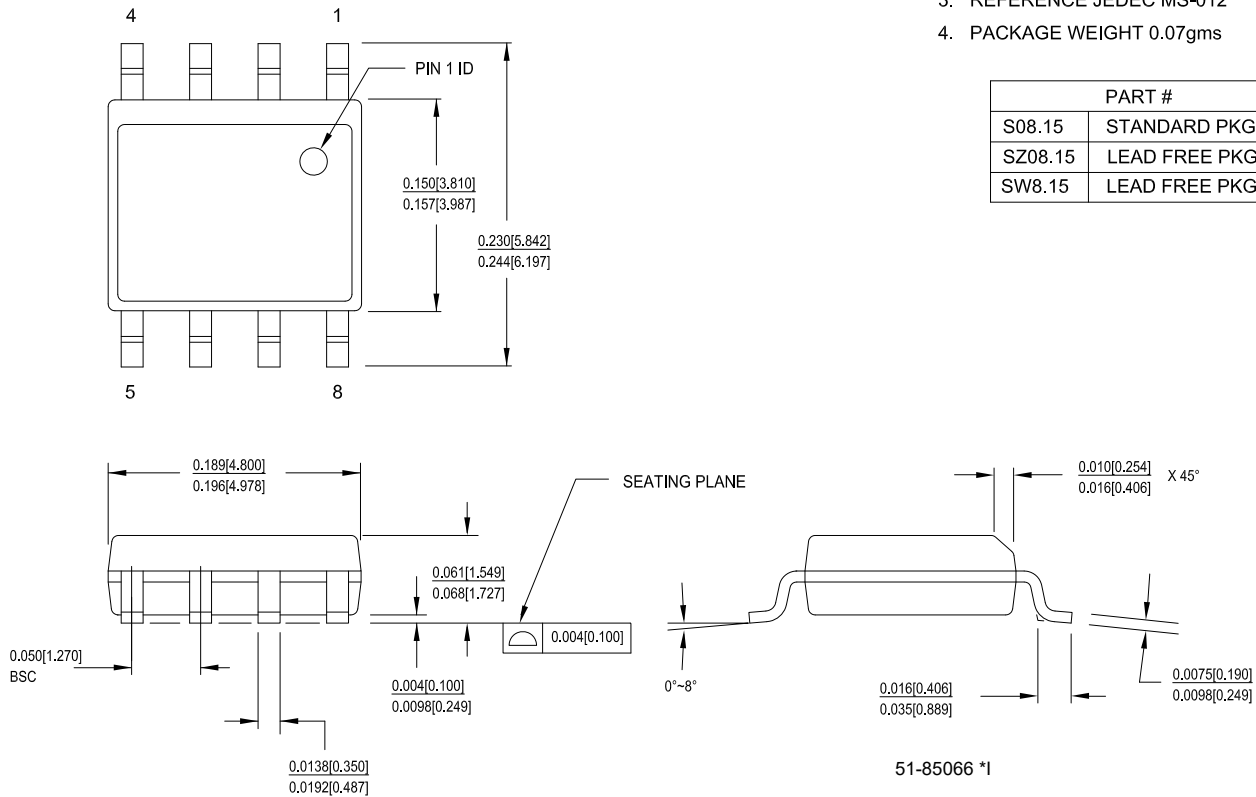


## Package Diagram

**Figure 9. 8-pin SOIC (150 Mils) Package Outline, 51-85066**

1. DIMENSIONS IN INCHES[MM] MIN. MAX.
2. PIN 1 ID IS OPTIONAL,  
ROUND ON SINGLE LEADFRAME  
RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

| PART #  |               |
|---------|---------------|
| S08.15  | STANDARD PKG  |
| SZ08.15 | LEAD FREE PKG |
| SW8.15  | LEAD FREE PKG |



## Acronyms

| Acronym | Description                      |
|---------|----------------------------------|
| PLL     | Phase Locked Loop                |
| SOIC    | Small Outline Integrated Circuit |

## Document Conventions

### Units of Measure

| Symbol | Units of Measure |
|--------|------------------|
| °C     | degree Celsius   |
| MHz    | megahertz        |
| μA     | microampere      |
| mA     | milliampere      |
| ms     | millisecond      |
| ns     | nanosecond       |
| pF     | picofarad        |
| ps     | picosecond       |
| V      | volt             |

## Appendix: Silicon Errata for the Zero Delay Clock Buffers, CY2304

This section describes the errors, workaround solution and silicon design fixes for Cypress zero delay clock buffers belonging to the families CY2304. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

### Part Numbers Affected

**Table 1. Part Numbers Affected**

| Part Number  | Device Variants |
|--------------|-----------------|
| CY2304SXC-1  | All Variants    |
| CY2304SXC-1T | All Variants    |
| CY2304SXC-2  | All Variants    |
| CY2304SXC-2T | All Variants    |
| CY2304SXI-1  | All Variants    |
| CY2304SXI-1T | All Variants    |
| CY2304SXI-2  | All Variants    |
| CY2304SXI-2T | All Variants    |

### CY2304 Errata Summary

| Items                             | Part Number | Fix Status                                              |
|-----------------------------------|-------------|---------------------------------------------------------|
| Start up lock time issue [CY2304] | All         | Silicon fixed. New silicon available from WW 10 of 2013 |

### CY2303 Qualification Status of fixed silicon

Product Status: In production

Qualification report last updated on 11/27/2012

<http://www.cypress.com/?rID=72595>

#### 1. Start up lock time issue

##### ■ Problem Definition

Output of CY2304 fails to locks within 1 ms upon power up (as per datasheet spec)

##### ■ Parameters Affected

PLL lock time

##### ■ Trigger Condition(s)

Start up

##### ■ Scope of Impact

It can impact the performance of system and its throughput

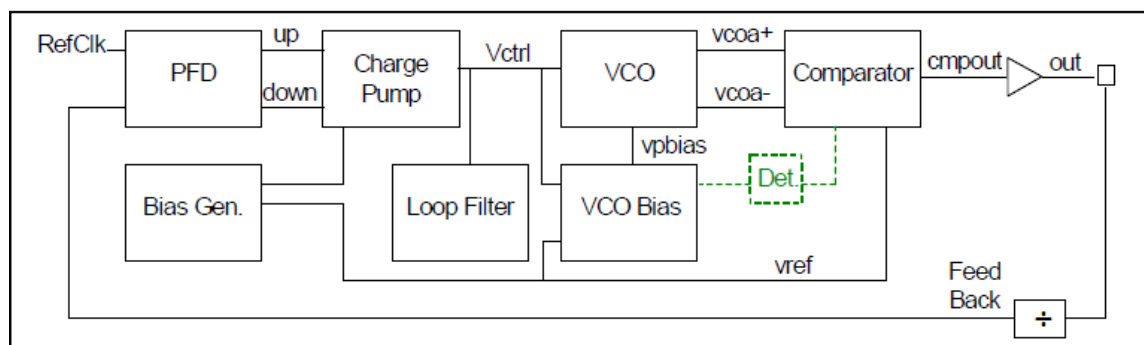
##### ■ Workaround

Apply reference input (RefClk) before power up ( $V_{DD}$ ). If RefClk is applied after power up, noise gets coupled on the output and propagates back to the PLL causing it to take higher time to acquire lock. If reference input is present during power up, noise will not propagate to the PLL and device will start up normally without problems.

##### ■ Fix Status

This issue is due to design marginality. Two minor design modifications have been made to address this problem.

- Addition of VCO bias detector block as shown in the following figure keeps comparator power down till VCO bias is present and thereby eliminating the propagation of noise to feedback.
- Bias generator enhancement for successful initialization.



## Document History Page

| Document Title: CY2304, 3.3 V Zero Delay Buffer<br>Document Number: 38-07247 |         |                 |                                                                                                                                                                                                                                                                                                          |
|------------------------------------------------------------------------------|---------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev.                                                                         | ECN     | Submission Date | Description of Change                                                                                                                                                                                                                                                                                    |
| **                                                                           | 110512  | 12/11/01        | Change from Spec number: 38-01010 to 38-07247                                                                                                                                                                                                                                                            |
| *A                                                                           | 112294  | 03/04/02        | On Pin Configuration Diagram (p.1), swapped CLKA2 and CLKA1                                                                                                                                                                                                                                              |
| *B                                                                           | 113934  | 05/01/02        | Added Operating Conditions for CY2304SI-X Industrial Temperature Devices, p. 4                                                                                                                                                                                                                           |
| *C                                                                           | 121851  | 12/14/02        | Power up requirements added to Operating Conditions Information                                                                                                                                                                                                                                          |
| *D                                                                           | 308436  | 01/26/05        | Added Lead-free Devices                                                                                                                                                                                                                                                                                  |
| *E                                                                           | 2542331 | 09/18/08        | Updated template. Added Note "Not recommended for new designs."<br>Removed part number CY2304SI-2 and CY2304SI-2T.<br>Changed Lead-Free to Pb-Free.<br>Changed IDD (PD mode) from 12.0 to 25.0 $\mu$ A.<br>Deleted Duty Cycle parameters for $F_{OUT} < 50.0$ MHz for commercial and industrial devices. |
| *F                                                                           | 2673353 | 03/13/09        | Reverted IDD (PD mode) and Duty Cycle parameters back to the values in revision *D:<br>Changed IDD (PD mode) from 25 to 12 $\mu$ A for commercial devices.<br>Added Duty Cycle parameters for $F_{OUT} < 50.0$ MHz for commercial and industrial devices.                                                |
| *G                                                                           | 2906571 | 04/07/10        | Removed parts CY2304SC-1, CY2304SC-1T, CY2304SC-2, CY2304SC-2T, CY2304SI-1, CY2304SI-1T from the ordering information table.<br>Updated Package Diagram.                                                                                                                                                 |
| *H                                                                           | 3072674 | 10/27/2010      | Corrected part number in all table titles (pages 3 to 5) from CY2304SC-X and CY2304SI-X to CY2304SXC and CY2304SXI.<br>Removed "except $t_g$ " from Figure 7                                                                                                                                             |
| *I                                                                           | 3162681 | 02/04/2011      | Updated to new template.                                                                                                                                                                                                                                                                                 |
| *J                                                                           | 3204827 | 03/24/2011      | Added duty cycle spec for 83.0 MHz output condition.                                                                                                                                                                                                                                                     |
| *K                                                                           | 4018186 | 06/10/2013      | Updated <a href="#">Package Diagram</a> :<br>spec 51-85066 – Changed revision from *D to *F.<br>Added <a href="#">Appendix: Silicon Errata for the Zero Delay Clock Buffers, CY2304</a> .                                                                                                                |
| *L                                                                           | 4291190 | 02/25/2014      | Updated to new template.<br>Completing Sunset Review.                                                                                                                                                                                                                                                    |
| *M                                                                           | 4578443 | 11/25/2014      | Updated <a href="#">Functional Description</a> :<br>Added "For a complete list of related documentation, click <a href="#">here</a> ." at the end.                                                                                                                                                       |
| *N                                                                           | 5270465 | 05/13/2016      | Added <a href="#">Thermal Resistance</a> .<br>Updated <a href="#">Package Diagram</a> :<br>spec 51-85066 – Changed revision from *F to *H.<br>Updated to new template.                                                                                                                                   |
| *O                                                                           | 5663902 | 03/17/2017      | Updated to new template.<br>Completing Sunset Review.                                                                                                                                                                                                                                                    |
| *P                                                                           | 6866984 | 04/24/2020      | Spec 51-85066 – Changed revision from *H to *I.                                                                                                                                                                                                                                                          |

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

|                               |                                                                    |
|-------------------------------|--------------------------------------------------------------------|
| Arm® Cortex® Microcontrollers | <a href="http://cypress.com/arm">cypress.com/arm</a>               |
| Automotive                    | <a href="http://cypress.com/automotive">cypress.com/automotive</a> |
| Clocks & Buffers              | <a href="http://cypress.com/clocks">cypress.com/clocks</a>         |
| Interface                     | <a href="http://cypress.com/interface">cypress.com/interface</a>   |
| Internet of Things            | <a href="http://cypress.com/iot">cypress.com/iot</a>               |
| Memory                        | <a href="http://cypress.com/memory">cypress.com/memory</a>         |
| Microcontrollers              | <a href="http://cypress.com/mcu">cypress.com/mcu</a>               |
| PSoC                          | <a href="http://cypress.com/psoc">cypress.com/psoc</a>             |
| Power Management ICs          | <a href="http://cypress.com/pmic">cypress.com/pmic</a>             |
| Touch Sensing                 | <a href="http://cypress.com/touch">cypress.com/touch</a>           |
| USB Controllers               | <a href="http://cypress.com/usb">cypress.com/usb</a>               |
| Wireless Connectivity         | <a href="http://cypress.com/wireless">cypress.com/wireless</a>     |

### PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

### Cypress Developer Community

[Community](#) | [Code Examples](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

### Technical Support

[cypress.com/support](http://cypress.com/support)

© Cypress Semiconductor Corporation, 2001-2020. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.