ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	CY2XP24ZXI
Manufacturer:	Cypress Semiconductor Corp
Package:	8-TSSOP (0.173", 4.40mm Width)
Availability:	Please confirm with sales

Product Page:

https://antrexco.com/product/details/cypress-semiconductor-corp/cy2xp24zxi.html

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

CY2XP24

Crystal to LVPECL Clock Generator

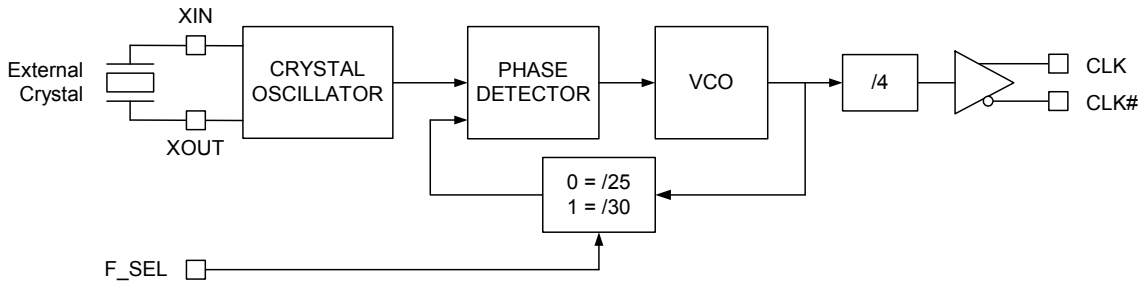
Features

- One LVPECL Output Pair
- Selectable output frequency: 156.25 MHz or 187.5 MHz
- External crystal frequency: 25 MHz
- Low root mean square (RMS) phase jitter at 156.25 MHz, using 25 MHz crystal (1.875 MHz to 20 MHz): 0.33 ps (typical)
- Pb-free 8-Pin thin shrunk small outline package (TSSOP) Package
- Supply voltage: 3.3 V or 2.5 V
- Commercial and industrial temperature ranges

Functional Description

The CY2XP24 is a PLL (phase locked loop) based high performance clock generator. It is optimized to generate 10 Gb Ethernet, Fibre Channel, and other high performance clock frequencies. It produces an output frequency that is either 6.25 times or 7.5 times the crystal frequency. It uses Cypress's low noise VCO technology to achieve low phase jitter, that meets both 10 Gb Ethernet, Fibre Channel, and SATA jitter requirements. The CY2XP24 has a crystal oscillator interface input and one LVPECL output pair.

Logic Block Diagram



Contents

Pinouts

Figure 1. Pin Diagram - 8 Pin TSSOP

Table 1. Pin Definitions - 8 Pin TSSOP

Pin	Name	Type	Description
1, 8	VDD	Power	3.3 V or 2.5 V power supply. All supply current flows through pin 1
2	VSS	Power	Ground
3, 4	XOUT, XIN	XTAL output and input	Parallel resonant crystal interface
5	F_SEL	CMOS input	Frequency select. When HIGH, the output frequency is 7.5 times of the crystal frequency. When LOW, the output frequency is 6.25 times of the crystal frequency
6,7	CLK#, CLK	LVPECL output	Differential clock output

Frequency Table

Inputs		PLL Multiplier Value	Output Frequency (MHz)
Crystal Frequency (MHz)	F_SEL		
25	1	7.5	187.5
25	0	6.25	156.25

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	–	–0.5	4.4	V
V_{IN}[1]	Input voltage, DC	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
T_S	Temperature, vtorage	Non operating	–65	150	°C
T_J	Temperature, junction		–	135	°C
ESD_{HBM}	ESD protection (human body model)	JEDEC STD 22-A114-B	2000	–	V
UL–94	Flammability rating	At 1/8 in.	V–0		
Θ_{JA}[2]	Thermal resistance, junction to ambient	0 m/s airflow	100		°C / W
		1 m/s airflow	91		
		2.5 m/s airflow	87		

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	3.3 V supply voltage	3.135	3.465	V
	2.5 V supply voltage	2.375	2.625	V
T_A	Ambient temperature, commercial	0	70	°C
	Ambient temperature, industrial	-40	85	°C
T_{PU}	Power-up time for all V_{DD} to reach minimum specified voltage (ensure power ramps are monotonic)	0.05	500	ms

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Power supply current with output unterminated	V_{DD} = 3.465 V, F_{OUT} = 187.5 MHz, output unterminated	–	–	125	V
		V_{DD} = 2.625 V, F_{OUT} = 187.5 MHz, output unterminated	–	–	120	V
I_{DDT}	Power supply current with output terminated	V_{DD} = 3.465 V, F_{OUT} = 187.5 MHz, output terminated	–	–	150	V
		V_{DD} = 2.625V, F_{OUT} = 187.5 MHz, output terminated	–	–	145	V
V_{OH}	LVPECL output high voltage	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 50 Ω to V_{DD} – 2.0 V	V_{DD} –1.15	–	V_{DD} –0.75	V
V_{OL}	LVPECL output low voltage	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 50 Ω to V_{DD} – 2.0 V	V_{DD} –2.0	–	V_{DD} –1.625	V
V_{OD1}	LVPECL Peak-to-peak output voltage swing	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 50 Ω to V_{DD} – 2.0 V	600	–	1000	mV

Note
1. The voltage on any input or I/O pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.
2. Simulated using Apache Sentinel TI software. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.

DC Electrical Characteristics (continued)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{OD2}	LVPECL output voltage swing (V_{OH} - V_{OL})	V_{DD} = 2.5 V, R_{TERM} = 50 Ω to V_{DD} – 1.5 V	500	–	1000	mV
V_{OCM}	LVPECL output common mode voltage (V_{OH} + V_{OL})/2	V_{DD} = 2.5 V, R_{TERM} = 50 Ω to V_{DD} – 1.5 V	1.2	–	–	V
V_{IH}	Input high voltage		0.7 x V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input low voltage		–0.3	–	0.3 x V_{DD}	V
I_{IH}	Input high current	F_SEL = V_{DD}	–	–	115	µA
I_{IL}	Input low current	F_SEL = V_{SS}	–50	–	–	µA
C_{IN}[3]	Input capacitance, F_SEL		–	15	–	pF
C_{INX}[3]	Pin capacitance, XIN & XOUT		–	4.5	–	pF

AC Electrical Characteristics[4]

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{OUT}	Output frequency		156.25	–	187.5	MHz
T_R, T_F[5]	Output rise/fall time	20 % to 80 % of full swing	–	0.5	1.0	ns
$T_{Jitter(\phi)}$[6]	RMS phase jitter (random)	156.25 MHz, (1.875 – 20 MHz), 3.3 V	–	0.33	–	ps
		156.25 MHz, (12 kHz – 20 MHz), 3.3 V	–	0.6	–	ps
T_{DC}[7]	Duty cycle	Measured at zero crossing point	45	–	55	%
T_{LOCK}	Startup time	Time for CLK to reach valid frequency measured from the time V_{DD} = V_{DD}(min.)	–	–	5	ms
T_{LFS}	Re-lock time	Time for CLK to reach valid frequency from F_SEL pin change	–	–	1	ms

Recommended Crystal Specifications[7]

Parameter	Description	Min	Max	Unit
Mode	Mode of oscillation	Fundamental		
F	Frequency	25	25	MHz
ESR	Equivalent series resistance	–	50	Ω
C_0	Shunt capacitance	–	7	pF

Notes
3. Not 100% tested, guaranteed by design and characterization.
4. Characterized using an 18 pF parallel resonant crystal.
5. Refer to Figure 7 on page 7.
6. Refer to Figure 4 on page 4.
7. Refer to Figure 7 on page 7.

Parameter Measurements

Figure 2. 3.3 V Output Load AC Test Circuit

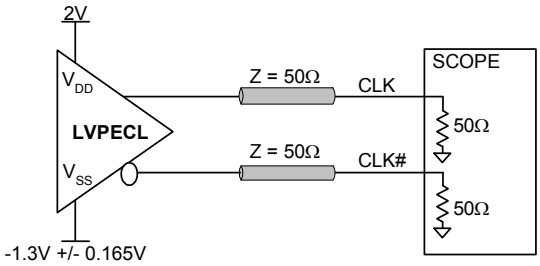


Figure 3. 2.5 V Output Load AC Test Circuit

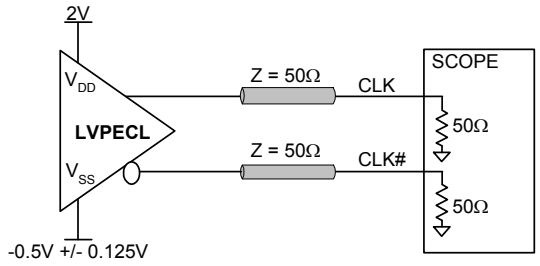


Figure 4. Output DC Parameters

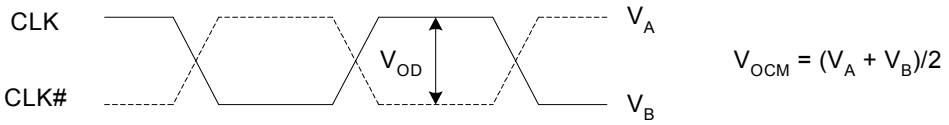


Figure 5. Output Rise and Fall Time

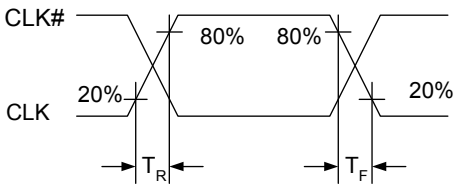


Figure 6. RMS Phase Jitter

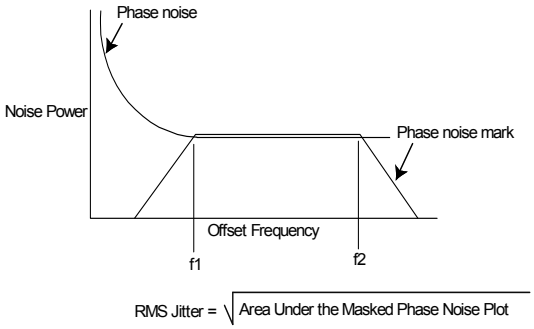
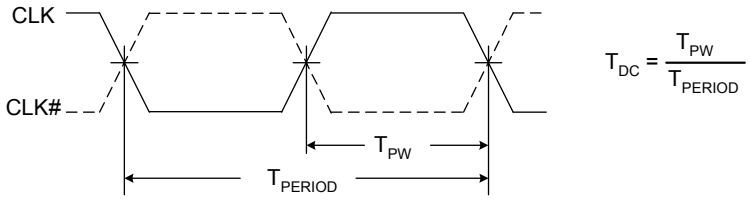


Figure 7. Output Duty Cycle

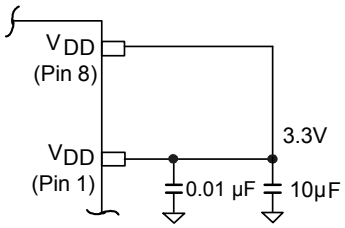


Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, noise at the power supply pins can degrade performance. To achieve optimum jitter performance, use good power supply isolation practices. Figure 8 illustrates a typical filtering scheme. Because all current flows through pin 1, the resistance and inductance between this pin and the supply is minimized. A 0.01 or 0.1 µF ceramic chip capacitor is also located close to this pin to provide a short and low impedance AC path to ground. A 1 to 10 µF ceramic or tantalum capacitor is located in the general vicinity of this device and may be shared with other devices.

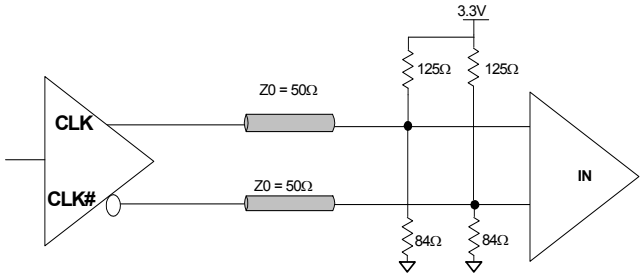
Figure 8. Power Supply Filtering



Termination for LVPECL Output

The CY2XP24 implements its LVPECL driver with a current steering design. For proper operation, it requires a 50 ohm dc termination on each of the two output signals. For 3.3 V operation, this data sheet specifies output levels for termination to V_{DD}–2.0 V. This termination voltage can also be used for V_{DD} = 2.5 V operation, or it can be terminated to V_{DD}-1.5 V. Note that it is also possible to terminate with 50 ohms to ground (V_{SS}), but the high and low signal levels differ from the data sheet values. Termination resistors are best located close to the destination device. To avoid reflections, trace characteristic impedance (Z_0) should match the termination impedance. Figure 9 shows a standard termination scheme.

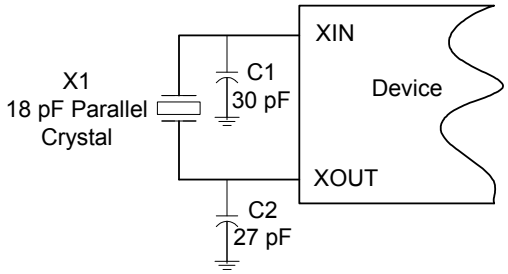
Figure 9. LVPECL Output Termination



Crystal Input Interface

The CY2XP24 is characterized with 18 pF parallel resonant crystals. The capacitor values shown in Figure 10 are determined using a 25 MHz 18 pF parallel resonant crystal and are chosen to minimize the ppm error. Note that the optimal values for C1 and C2 depend on the parasitic trace capacitance and are therefore layout dependent.

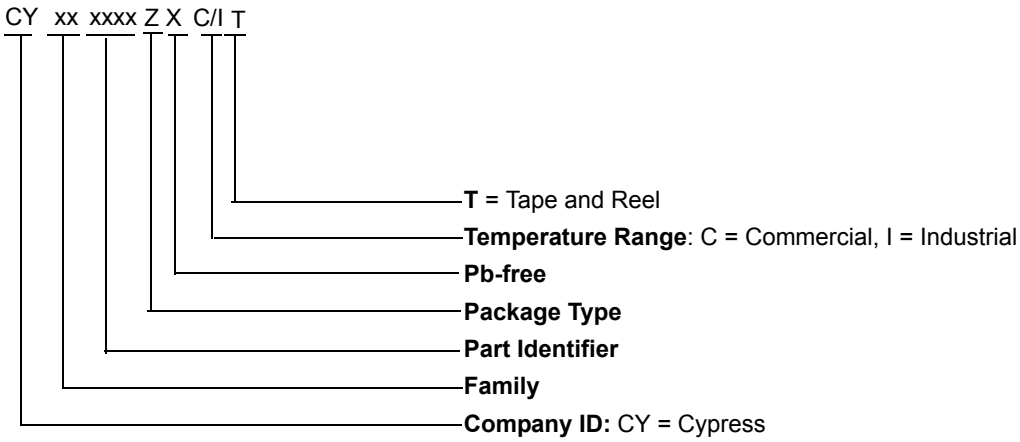
Figure 10. Crystal Input Interface



Ordering Information

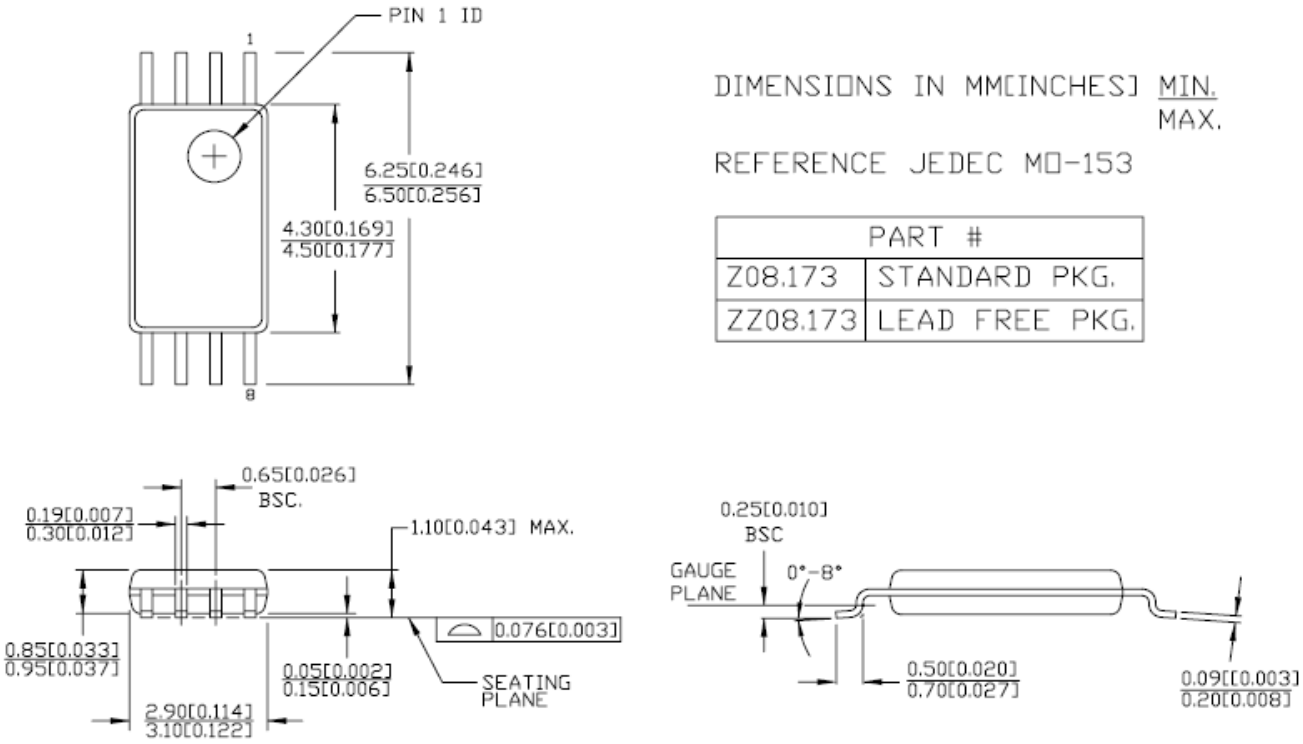
Part Number	Package Type	Product Flow
CY2XP24ZXC	8-Pin TSSOP	Commercial, 0 °C to 70 °C
CY2XP24ZXCT	8-Pin TSSOP–Tape and Reel	Commercial, 0 °C to 70 °C
CY2XP24ZXI	8-Pin TSSOP	Industrial, -40 °C to 85 °C
CY2XP24ZXIT	8-Pin TSSOP–Tape and Reel	Industrial, -40 °C to 85 °C

Ordering Code Definition



Package Drawing and Dimensions

Figure 11. 8-Pin Thin Shrunk Small Outline Package (4.40 MM Body) Z8



51-85093 *C

Acronyms

Acronym	Description
CLKOUT	Clock output
CMOS	Complementary metal oxide semiconductor
DPM	Die pick map
EPROM	Erasable programmable read only memory
LVDS	Low-voltage differential signaling
LVPECL	Low voltage positive emitter coupled logic
NTSC	National television system committee
OE	Output enable
PAL	Phase alternate line
PD	Power down
PLL	Phase locked loop
PPM	Parts per million
TTL	Transistor transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
kHz	kilohertz
kΩ	kilohms
MHz	megahertz
MΩ	megaohms
µA	microamperes
µs	microseconds
µV	microvolts
µVrms	microvolts root-mean-square
mA	milliamperes
mm	millimeters
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms

Document History Page

Document Title: CY2XP24 Crystal to LVPECL Clock Generator Document Number: 001-15705				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	1285703	See ECN	WWZ/KVM/ ARI	New data sheet
*A	1451704	See ECN	WWZ/AESA	Added I-temp devices
*B	2669117	03/05/2009	KVM/AESA	Changed crystal frequency and output frequencies Updated phase jitter value Rise & fall times changed from 350 ps to 500 ps (typ.) Junction temperature changed from 125°C to 135°C Changed IIL and IIH values Entered value for IDD Removed MSL spec Changed Data Sheet Status to Final
*C	2700242	04/30/2009	KVM/PYRS	Typos: changed VCC to VDD, changed ps to MHz Changed footnote about external power dissipation Reformatted AC and DC tables Changed LVPECL parameters from VPP to VOD and VOCM Added CINX spec Added IDD for 2.5V Added TLOCK timing Revised text in Application Information section Changed recommended crystal load capacitor values
*D	2718433	06/12/2009	WWZ/HMT	No change. Submit to ECN for product launch.
*E	2767308	09/22/2009	KVM	Add phase jitter spec for 12 kHz - 20 MHz integration range Add I_{DD} spec for unterminated outputs Change parameter name for I_{DD} (terminated outputs) from I_{DD} to I_{DDT} Remove I_{DD} footnote about externally dissipated current Add footnote reference to C_{IN} and C_{INX}:not 100% tested Add max limit for T_R, T_F: 1.0 ns Change T_{LOCK} max from 10 ms to 5 ms Split out parameter T_{LFS} from T_{LOCK}
*F	2896121	03/19/2010	KVM	Updated Package Diagram (Figure 11)
*G	3218841	03/07/2011	BASH	Updated as per template Added Acronyms and Units of Measure table Added Ordering Code Definition details Updated package diagram 51-85093 from *B to *C

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