

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: CY26580KOI-2
Manufacturer: Cypress Semiconductor Corp
Package: 20-SSOP (0.154", 3.90mm Width)
Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/cypress-semiconductor-corp/cy26580koi-2.html>

Request a Quote:

[Submit RFQ for this part](#)



Scan for product page

Contact Information

Email: info@antrexco.com

WhatsApp: +86-186-8066-5326

Website: <https://antrexco.com>

Quality & Trust

New & Original Components

Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

Secure sourcing support for OEM / EMS projects

Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

PacketClock™ Network Applications Clock

Features

- Integrated phase-locked loop (PLL)
- Low-jitter, high-accuracy outputs
- 3.3V operation

Benefits

- Internal PLL with precision operation
- Meets critical timing requirements in complex system designs
- Enables application compatibility

Table 1. Frequency Table

Part Number	Outputs	Input Frequency	Output Frequencies
CY26580-1	2	125MHz or 25-MHz driven	100 MHz, 133.33 MHz

Logic Block Diagram

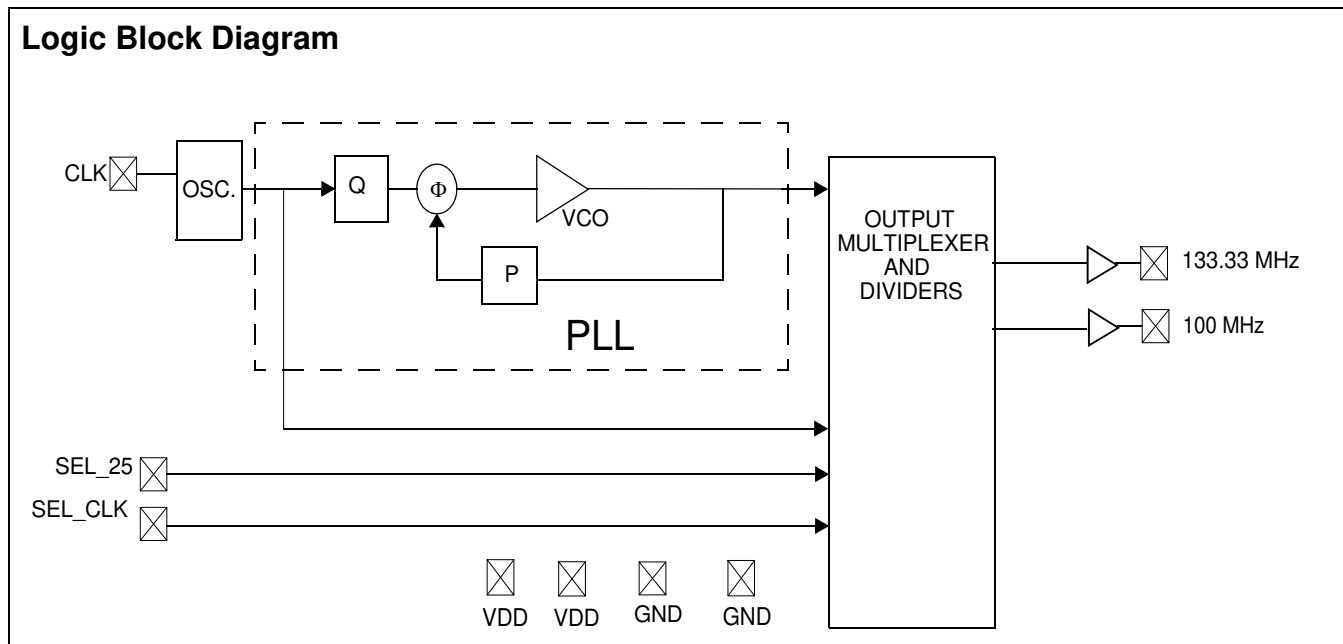


Table 2. Input Select Options

SEL_25	SEL_CLK	Input Type	Input Frequency	CLK1	CLK2	Unit
X	0	Do not use				
0	1	Driven	125	133.33	100	MHz
1	1	Driven	25	133.33	100	MHz

Pin Configuration

Figure 1. CY26580 20-pin SSOP (QSOP)

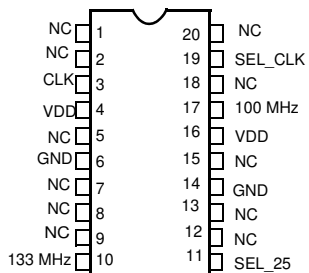


Table 3. Pin Definition

Pin Name	Pin Number	Pin Description
NC	1	No Connect
NC	2	No Connect
CLK	3	Reference Input
V _{DD}	4	Voltage Supply
NC	5	No Connect
GND	6	Ground
NC	7	No Connect
NC	8	No Connect
NC	9	No Connect
133 MHz	10	133.33-MHz Clock Output
SEL_25	11	Reference Frequency Select Input; 0 = 125 MHz, 1 = 25 MHz, weak internal pull up
NC	12	No Connect
NC	13	No Connect
GND	14	Ground
NC	15	No Connect
V _{DD}	16	Voltage Supply
100 MHz	17	100-MHz Clock Output
NC	18	No Connect
SEL_CLK	19	Reference Select Input; Set to 1 = Driven, weak internal pull up
NC	20	No Connect

Absolute Maximum Conditions^[1]

Supply Voltage (V_{DD}) -0.5 to +7.0V
 DC Input Voltage -0.5V to $V_{DD}+0.5$
 Storage Temperature (Non-condensing) -55°C to +125°C

Junction Temperature -40°C to +125°C
 Data Retention at $T_j = 125^\circ\text{C}$ > 10 years
 Package Power Dissipation 350 mW
 ESD (Human Body Model) MIL-STD-883 2000V

Recommended Operating Conditions

Parameter	Description	Min	Typ.	Max	Unit
V_{DD}	Supply Voltage	3.14	3.3	3.47	V
T_A , I-grade	Ambient Temperature, Industrial	-40	—	85	°C
C_{LOAD}	Max. Load Capacitance	—	—	15	pF
f_{REF}	Reference Frequency	—	125, 25	—	MHz

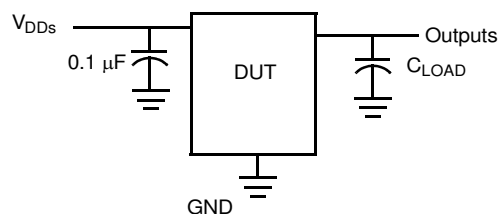
DC Electrical Specifications

Parameter ^[2]	Description	Conditions	Min	Typ.	Max	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} - 0.5$, $V_{DD} = 3.3\text{V}$	12	24	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3\text{V}$	12	24	—	mA
I_{IH}	Input High Current	$V_{IH} = V_{DD}$	—	5	10	μA
I_{IL}	Input Low Current	$V_{IL} = 0\text{V}$	—	—	50	μA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7	—	—	V_{DD}
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}	—	—	0.3	V_{DD}
I_{DD}	Supply Current	V_{DD} Current, no load	—	35	50	mA
R_{UP}	Pull up resistor on Inputs	$V_{DD} = 3.14$ to 3.47V , measured $V_{IN} = 0\text{V}$	—	100	150	kΩ

AC Electrical Specifications

Parameter ^[2]	Description	Conditions	Min	Typ.	Max	Unit
F_{error}	Frequency Error	All clocks			0	ppm
DC	Output Duty Cycle	Duty Cycle is defined in Figure 3 , 50% of V_{DD}	45	50	55	%
ER	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD} , $C_{LOAD} = 15\text{ pF}$. See Figure 4 .	0.8	1.4	2	V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD} , $C_{LOAD} = 15\text{ pF}$. See Figure 4 .	0.8	1.4	2	V/ns
t_9	Clock Jitter	CLK1, CLK2 Peak-Peak period jitter	—	100	—	ps
t_{10}	PLL Lock Time		—	—	3	ms

Figure 2. Test and Measurement Setup



Notes

1. Above which the useful life may be impaired. For user guidelines, not tested.
2. Guaranteed by characterization, not 100% tested.

Voltage and Timing Definitions

Figure 3. Duty Cycle Definition

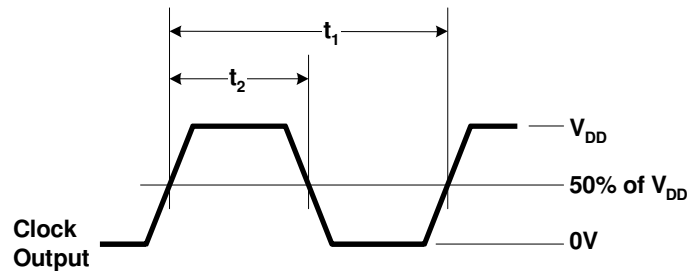
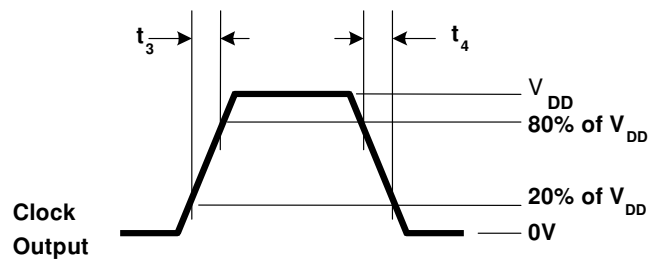


Figure 4. $ER = (0.6 \times V_{DD}) / t_3$, $EF = (0.6 \times V_{DD}) / t_4$



Ordering Information

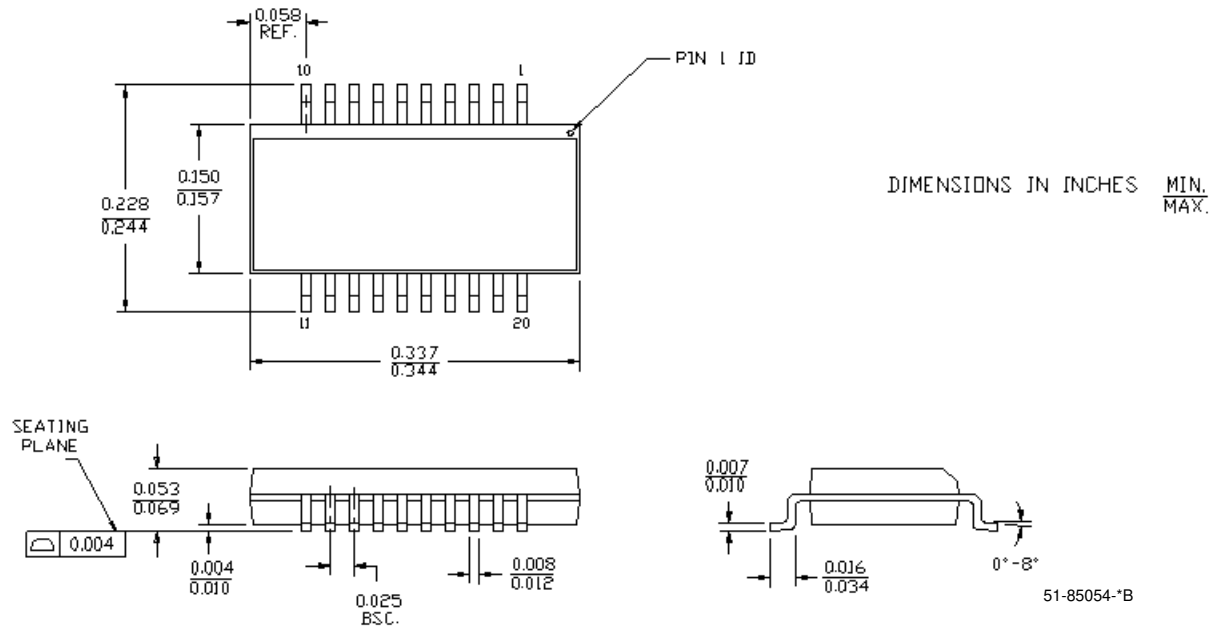
Ordering Code ^[3]	Package Type	Temperature Range	Operating Voltage
CY26580OI-2 ^[4]	20-pin SSOP (QSOP)	Industrial	3.3V
CY26580OI-2T ^[4]	20-pin SSOP (QSOP) – Tape and Reel	Industrial	3.3V
CY26580KOI-2	20-pin SSOP (QSOP)	Industrial	3.3V
CY26580KOI-2T	20-pin SSOP (QSOP) – Tape and Reel	Industrial	3.3V
Pb-Free			
CY26580KQXI-2	20-pin SSOP (QSOP)	Industrial	3.3V
CY26580KQXI-2T	20-pin SSOP (QSOP) – Tape and Reel	Industrial	3.3V

Notes

- Part numbers ending in -1 and -1T have been replaced by part numbers ending in -2 and -2T. Specifications for -1, -1T, -2 and -2T part numbers are identical.
- Not recommended for new designs.

Package Drawing and Dimensions

Figure 5. 20-lead QSOP O201 and SQ201



Document History Page

Document Title: CY26580 PacketClock™ Network Applications Clock Document #: 38-07536 Rev. *C				
REV.	ECN NO.	Submission Date	Orig. of Change	Description of Change
**	127357	06/17/03	RGL	New Data Sheet
*A	128564	09/12/03	IJA	Change pin 1 to NC and pin 3 to CLK
*B	216828	See ECN	RGL	Removed Preliminary
*C	2442066	See ECN	KVM/AESA	Updated template. Added Note "Not recommended for new designs." Added Note explaining "-1" and "-2" part numbers. Removed part numbers CY26580OI-1 and CY26580OI-1T. Added part number CY26580OI-2T, CY26580KOI-2, CY26580KOI-2T, CY26580KQXI-2, and CY26580KQXI-2T in ordering information table. Updated figure caption for package drawing.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

PSoC	psoc.cypress.com
Clocks & Buffers	clocks.cypress.com
Wireless	wireless.cypress.com
Memories	memory.cypress.com
Image Sensors	image.cypress.com

PSoC Solutions

General	psoc.cypress.com/solutions
Low Power/Low Voltage	psoc.cypress.com/low-power
Precision Analog	psoc.cypress.com/precision-analog
LCD Drive	psoc.cypress.com/lcd-drive
CAN 2.0b	psoc.cypress.com/can
USB	psoc.cypress.com/usb

© Cypress Semiconductor Corporation, 2008. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and/or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.