

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: CY26114ZCT
Manufacturer: Cypress Semiconductor Corp
Package: 16-TSSOP (0.173", 4.40mm Width)
Availability: Please confirm with sales

Product Page:

<https://antrexco.com/product/details/cypress-semiconductor-corp/cy26114zct.html>

Request a Quote:

[Submit RFQ for this part](#)



Scan for product page

Contact Information

Email: info@antrexco.com

WhatsApp: +86-186-8066-5326

Website: <https://antrexco.com>

Quality & Trust

New & Original Components

Supplier verification and packaging condition review

CoC / RoHS / REACH documents available on request

Secure sourcing support for OEM / EMS projects

Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

One-PLL Clock Generator

Features

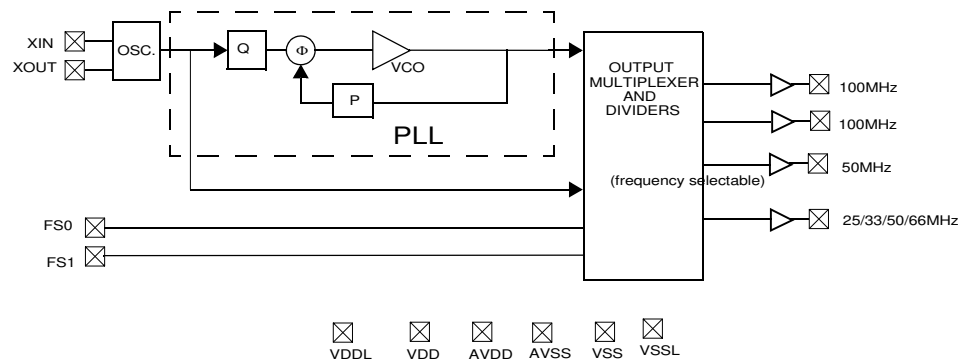
- Integrated phase-locked loop
- Low skew, low jitter, high accuracy outputs
- 3.3V operation with 2.5 V output option

Benefits

- Internal PLL with up to 333 MHz internal operation.
- Meets critical timing requirements in complex system designs.
- Enables application compatibility.

Part Number	Outputs	Input Frequency	Output Frequency Range
CY26114	4	25 MHz Crystal Input	2 copies of 100 MHz, 1 copy of 50 MHz, 1 copy 25, 33, 50, and 66 MHz (frequency selectable)

Logic Block Diagram



CLK4 Frequency Select Options

FS1	FS0	CLK 4	Units
0	0	25	MHz
0	1	33	MHz
1	0	50	MHz
1	1	66	MHz

Pin Configurations

Figure 1. CY26114, 16-Pin TSSOP

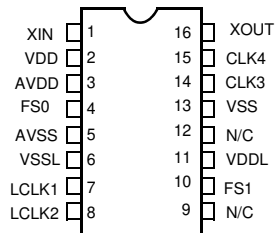


Table 1. Pin Definitions

Name	Pin Number	Description
XIN	1	Reference Crystal Input
V _{DD}	2	Voltage Supply
AV _{DD}	3	Analog Voltage Supply
FS0	4	Frequency Select 0
AV _{SS}	5	Analog Ground
V _{SSL}	6	LCLK Ground
LCLK1	7	100 MHz Output clock at V _{DDL} Level
LCLK2	8	100 MHz Output clock at V _{DDL} Level
N/C	9	No Connect
FS1	10	Frequency Select 1
V _{DDL}	11	LCLK Voltage Supply (2.5V or 3.3V)
N/C	12	No Connect
VSS	13	Ground
CLK3	14	50 MHz Output Clock
CLK4	15	25, 33, 50, and 66 MHz Clock Output (frequency selectable)
XOUT ^[1]	16	Reference Crystal Output

Note

1. Float XOUT if XIN is externally driven.

Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	-0.5	7.0	V
V_{DDL}	IO Supply Voltage		7.0	V
T_J	Junction Temperature		125	°C
	Digital Inputs	$AV_{SS} - 0.3$	$AV_{DD} + 0.3$	V
	Digital Outputs Referred to V_{DD}	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
	Digital Outputs Referred to V_{DDL}	$V_{SS} - 0.3$	$V_{DDL} + 0.3$	V
	Electro-Static Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Operating Voltage	3.0	3.3	3.6	V
V_{DDL}	Operating Voltage	2.375	2.5	2.625	V
T_A	Ambient Temperature	0		70	°C
C_{LOAD}	Maximum Load Capacitance			15	pF
f_{REF}	Reference Frequency		25		MHz
t_{PU}	Power Up Time—for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

DC Electrical Characteristics

Parameter ^[2]	Name	Description	Min	Typ	Max	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} - 0.5$, $V_{DD}/V_{DDL} = 3.3V$	12	24		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD}/V_{DDL} = 3.3V$	12	24		mA
I_{OH}	Output High Current	$V_{OH} = V_{DDL} - 0.5$, $V_{DDL} = 2.5V$	8	16		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DDL} = 2.5V$	8	16		mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7			VDD
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}			0.3	VDD
I_{VDD}	Supply Current	AV_{DD}/V_{DD} Current			25	mA
I_{VDDL}	Supply Current	V_{DDL} Current ($V_{DDL} = 3.6V$)			20	mA
I_{VDDL}	Supply Current	V_{DDL} Current ($V_{DDL} = 2.625V$)			15	mA

AC Electrical Characteristics

Parameter ^[2]	Name	Description	Min	Typ	Max	Unit
DC	Output Duty Cycle	Duty cycle is defined in Figure 2; t_1/t_2 , 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Rate	Output clock rise time, 20%–80% of $V_{DD}/V_{DDL} = 3.3V$	0.8	1.4		V/ns
t_3	Rising Edge Rate	Output clock rise time, 20%–80% of $V_{DDL} = 2.5V$	0.6	1.2		V/ns
t_4	Falling Edge Rate	Output clock fall time, 80%–20% of $V_{DD}/V_{DDL} = 3.3V$	0.8	1.4		V/ns
t_4	Falling Edge Rate	Output clock fall time, 80%–20% of $V_{DDL} = 2.5V$	0.6	1.2		V/ns
t_5	Skew	Delay between related outputs at rising edge			250	ps
t_9	Clock Jitter	Peak to peak period jitter			200	ps
t_{10}	PLL Lock Time				3	ms

Note

2. Not 100% tested.

Figure 2. Duty Cycle Definitions: $DC = t_2/t_1$

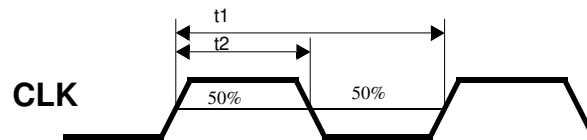


Figure 3. Rise Time and Fall Time Definitions

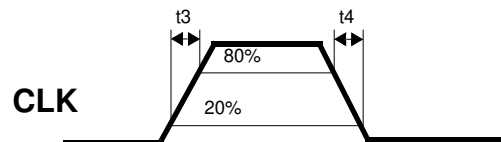
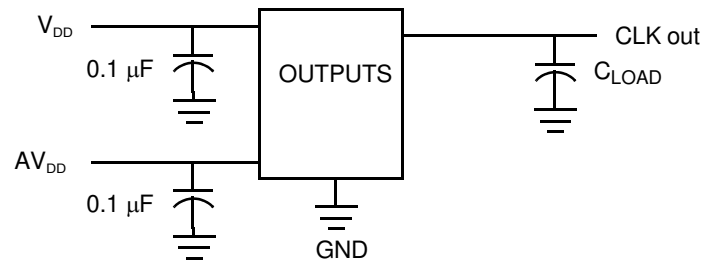


Figure 4. Test Circuit



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY26114ZC ^[3]	Z16	16-Pin TSSOP	Commercial	3.3V
CY26114KZC	Z16	16-Pin TSSOP	Commercial	3.3V
CY26114KZCT	Z16	16-Pin TSSOP- Tape and Reel	Commercial	3.3V

Note

3. Not recommended for new designs.

Document History Page

Document Title: CY26114 One-PLL Clock Generator Document Number: 38-07098				
Revision	ECN No.	Origin of Change	Submission Date	Description of Change
**	107333	CKN	12/14/02	New Data Sheet
*A	121867	RBI	08/28/01	Power up requirements added to Operating Conditions Information
*B	2441946	AESA	05/15/08	Updated template. Added Note "Not recommended for new designs." Added part number CY26114KZC, and CY26114KZCT in ordering information table.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

PSoC	psoc.cypress.com
Clocks & Buffers	clocks.cypress.com
Wireless	wireless.cypress.com
Memories	memory.cypress.com
Image Sensors	image.cypress.com

PSoC Solutions

General	psoc.cypress.com/solutions
Low Power/Low Voltage	psoc.cypress.com/low-power
Precision Analog	psoc.cypress.com/precision-analog
LCD Drive	psoc.cypress.com/lcd-drive
CAN 2.0b	psoc.cypress.com/can
USB	psoc.cypress.com/usb

© Cypress Semiconductor Corporation, 2002-2008. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and/or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.