

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	BLF7G22L-200,118
Manufacturer:	Ampleon USA Inc.
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

<https://antrexco.com/product/details/ampleon-usa-inc/blf7g22l-200-118.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

BLF7G22L-200; BLF7G22LS-200

Power LDMOS transistor

Rev. 5 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

200 W LDMOS power transistor for base station applications at frequencies from 2110 MHz to 2170 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ °C}$ in a common source class-AB production test circuit.

Mode of operation	f (MHz)	I_{DQ} (mA)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA	2110 to 2170	1620	28	55	18.5	31	-31 ^[1]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz.

1.2 Features and benefits

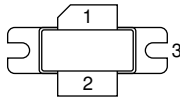
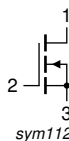
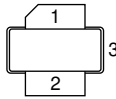
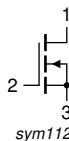
- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 2110 MHz to 2170 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF7G22L-200 (SOT502A)			
1	drain		
2	gate		
3	source		
BLF7G22LS-200 (SOT502B)			
1	drain		
2	gate		
3	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF7G22L-200	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF7G22LS-200	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$; $P_L = 80\text{ W (CW)}$; $V_{DS} = 28\text{ V}$; $I_{Dq} = 1620\text{ mA}$	0.26	K/W

6. Characteristics

Table 6. Characteristics

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1.5\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 150\text{ mA}$	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	4.2	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $V_{DS} = 10\text{ V}$	42	50.8	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	420	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 5.25\text{ A}$	-	18.9	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $I_D = 5.25\text{ A}$	-	0.054	-	Ω

7. Test information

Table 7. Functional test information

Mode of operation: 2-carrier W-CDMA; PAR = 8.4 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1-64 DPCH; $f_1 = 2112.5\text{ MHz}$; $f_2 = 2117.5\text{ MHz}$; $f_3 = 2162.5\text{ MHz}$; $f_4 = 2167.5\text{ MHz}$; RF performance at $V_{DS} = 28\text{ V}$; $I_{Dq} = 1620\text{ mA}$; $T_{case} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	55	-	W
G_p	power gain	$P_{L(AV)} = 55\text{ W}$	16.8	18.5	-	dB
RL_{in}	input return loss	$P_{L(AV)} = 55\text{ W}$	-	-15	-6	dB
η_D	drain efficiency	$P_{L(AV)} = 55\text{ W}$	27	31	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 55\text{ W}$	-	-31	-25.5	dBc

7.1 Ruggedness in class-AB operation

The BLF7G22L-200 and BLF7G22LS-200 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:

$V_{DS} = 28\text{ V}$; $I_{Dq} = 1620\text{ mA}$; $P_L = 200\text{ W}$ (CW); $f = 2110\text{ MHz}$ to 2170 MHz .

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data; $I_{DQ} = 1620$ mA; $V_{DS} = 28$ V.

f (MHz)	Z_S ^[1] (Ω)	Z_L ^[1] (Ω)
2050	$1.05 - j4.04$	$2.04 - j1.28$
2110	$1.18 - j4.17$	$1.67 - j1.52$
2140	$1.32 - j4.68$	$1.67 - j1.52$
2170	$1.58 - j4.37$	$1.62 - j1.63$
2230	$2.55 - j5.14$	$1.51 - j1.83$

[1] Z_S and Z_L defined in [Figure 1](#).

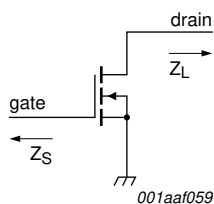
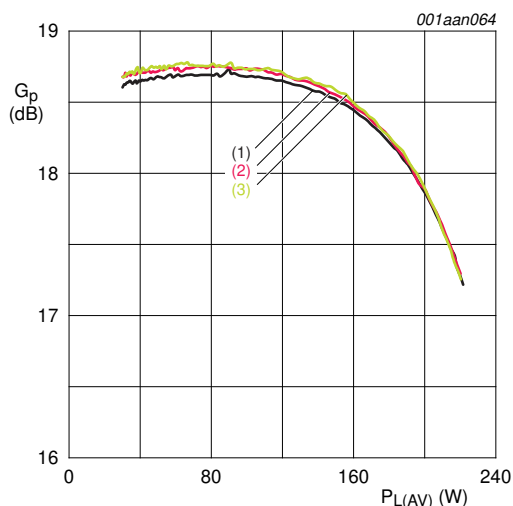


Fig 1. Definition of transistor impedance

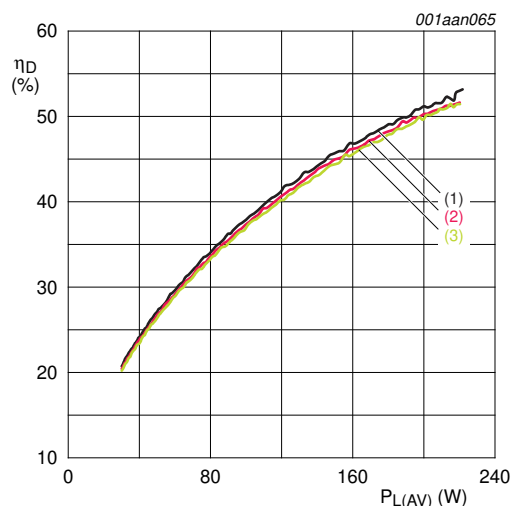
7.3 1 Tone CW



$V_{DS} = 28$ V; $I_{DQ} = 1620$ mA.

- (1) $f = 2110$ MHz
- (2) $f = 2140$ MHz
- (3) $f = 2170$ MHz

Fig 2. Power gain as a function of average load power; typical values



$V_{DS} = 28$ V; $I_{DQ} = 1620$ mA.

- (1) $f = 2110$ MHz
- (2) $f = 2140$ MHz
- (3) $f = 2170$ MHz

Fig 3. Drain efficiency as a function of average load power; typical values

7.4 1-carrier W-CDMA

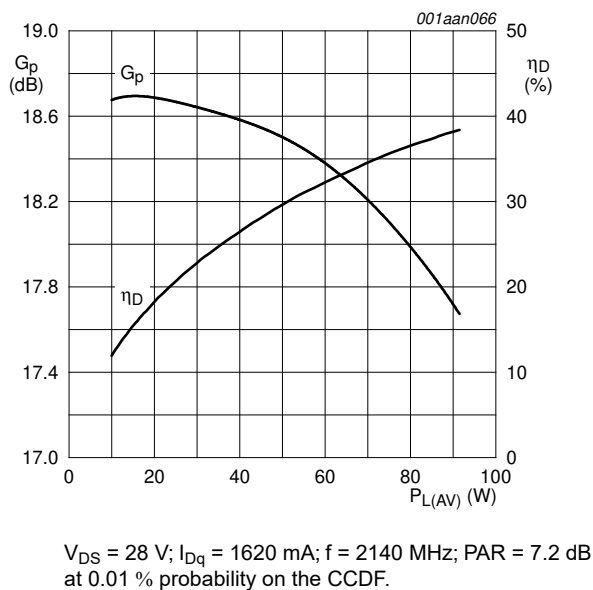


Fig 4. Power gain and drain efficiency as functions of average load power; typical values

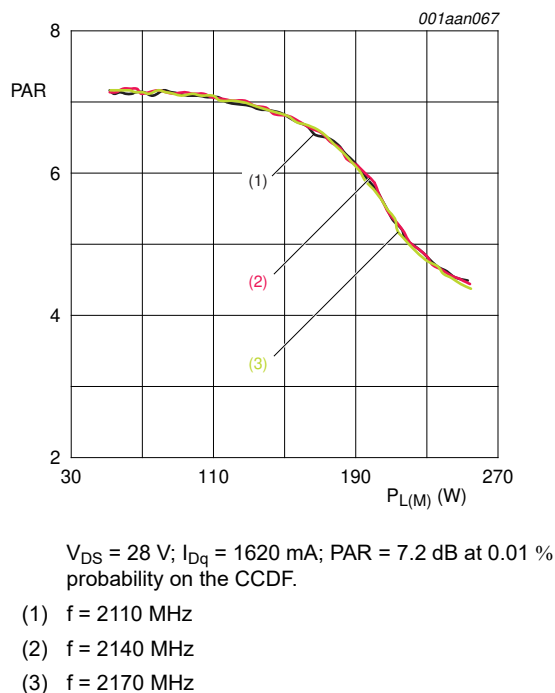


Fig 5. Peak-to-average power ratio as function of peak power; typical values

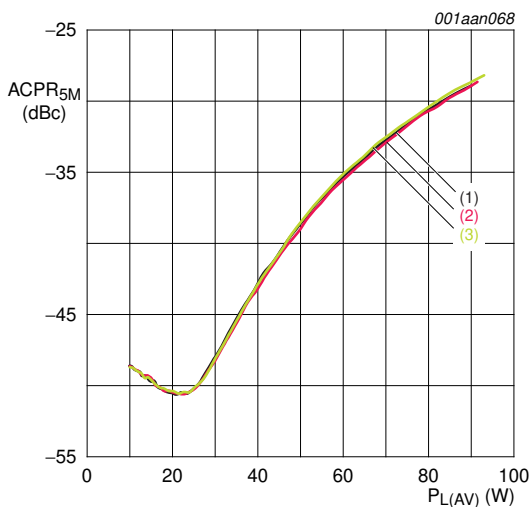
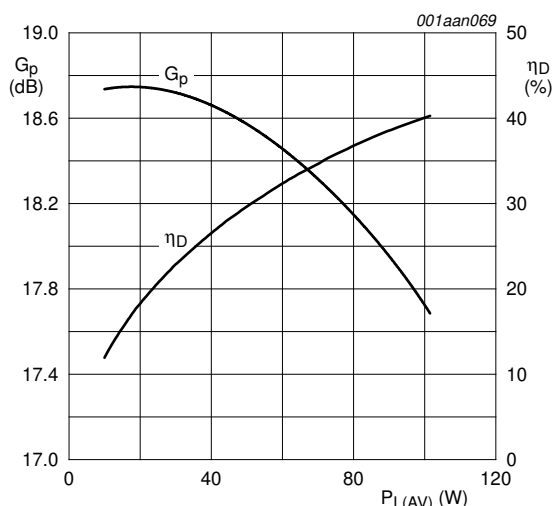


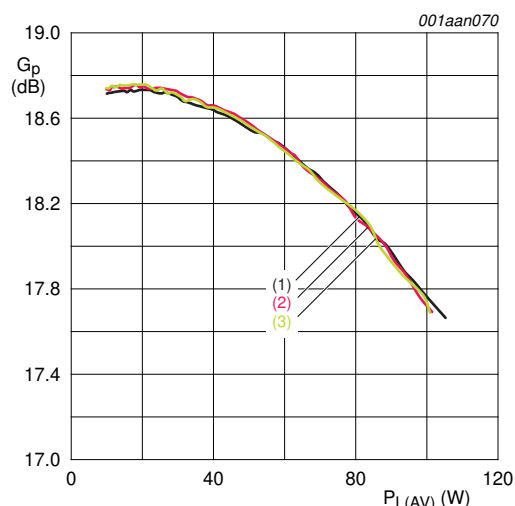
Fig 6. Adjacent power channel ratio (5 MHz) as function of average load power; typical values

7.5 2-carrier W-CDMA



$V_{DS} = 28$ V; $I_{DQ} = 1620$ mA; $f = 2140$ MHz; Channel Spacing = 5 MHz; PAR = 8.4 dB at 0.01 % probability on the CCDF.

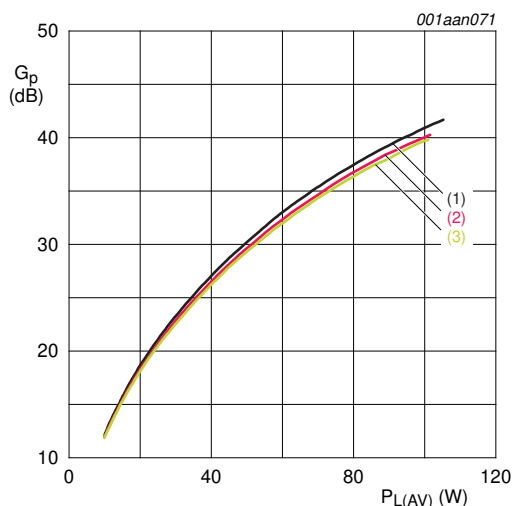
Fig 7. Power gain and drain efficiency as functions of average load power; typical values



$V_{DS} = 28$ V; $I_{DQ} = 1620$ mA; Channel Spacing = 5 MHz; PAR = 8.4 dB at 0.01 % probability on the CCDF.

- (1) $f = 2110$ MHz
- (2) $f = 2140$ MHz
- (3) $f = 2170$ MHz

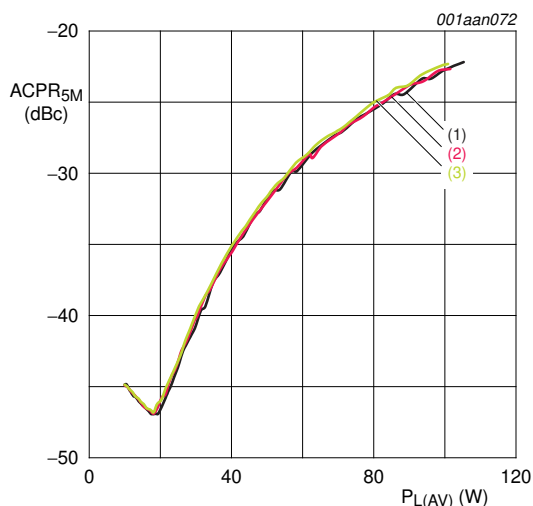
Fig 8. Power gain as a function of average load power; typical values



$V_{DS} = 28$ V; $I_{DQ} = 1620$ mA; Channel Spacing = 5 MHz; PAR = 8.4 dB at 0.01 % probability on the CCDF.

- (1) $f = 2110$ MHz
- (2) $f = 2140$ MHz
- (3) $f = 2170$ MHz

Fig 9. Drain efficiency as function of average load power; typical values

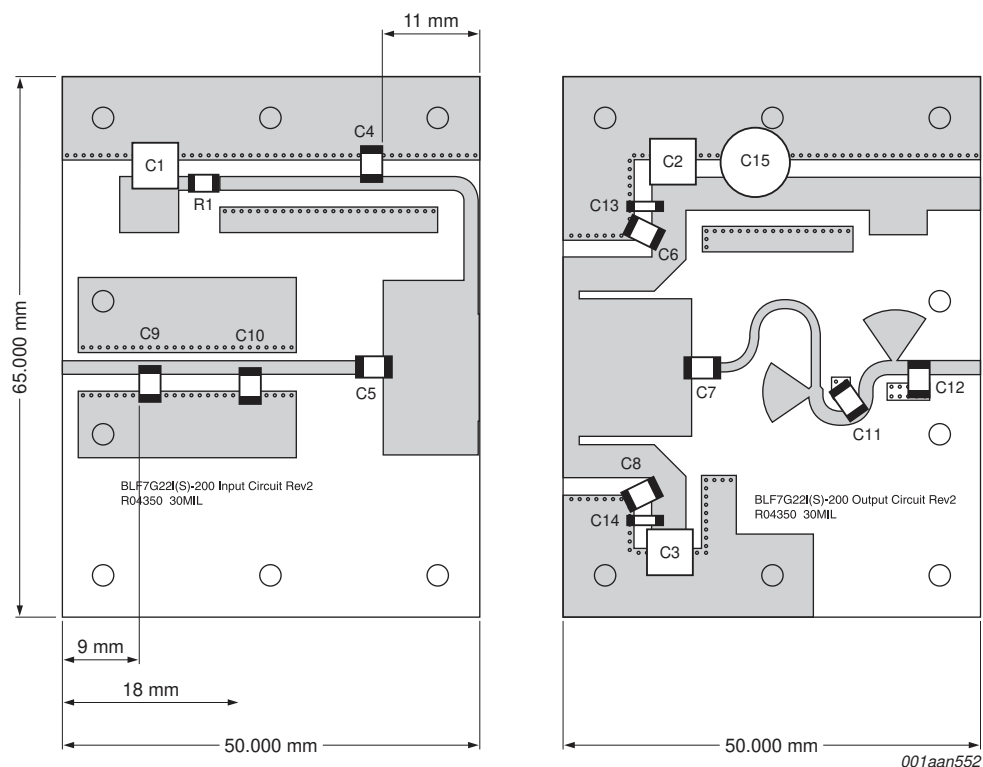


$V_{DS} = 28$ V; $I_{DQ} = 1620$ mA; Channel Spacing = 5 MHz; PAR = 8.4 dB at 0.01 % probability on the CCDF.

- (1) $f = 2110$ MHz
- (2) $f = 2140$ MHz
- (3) $f = 2170$ MHz

Fig 10. Adjacent power channel ratio (5 MHz) as function of average load power; typical values

7.6 Test circuit



See [Table 9](#) for list of components.

Fig 11. Component layout

Table 9. List of components

See [Figure 11](#) for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	10 μ F	[1] TDK
C2, C3	multilayer ceramic chip capacitor	4.7 μ F	[1] TDK
C4, C5, C6, C7, C8	multilayer ceramic chip capacitor	22 pF	[2] ATC100B
C9	multilayer ceramic chip capacitor	2.0 pF	[2] ATC100B
C10	multilayer ceramic chip capacitor	2.1 pF	[2] ATC100B
C11	multilayer ceramic chip capacitor	0.5 pF	[2] ATC100B
C12	multilayer ceramic chip capacitor	0.9 pF	[2] ATC100B
C13, C14	multilayer ceramic chip capacitor	330 nF	[1] TDK
C15	electrolytic capacitor	470 μ F; 63 V	
R1	chip resistor	10 Ω	Philips 1206

[1] TDK or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leadsSOT502A

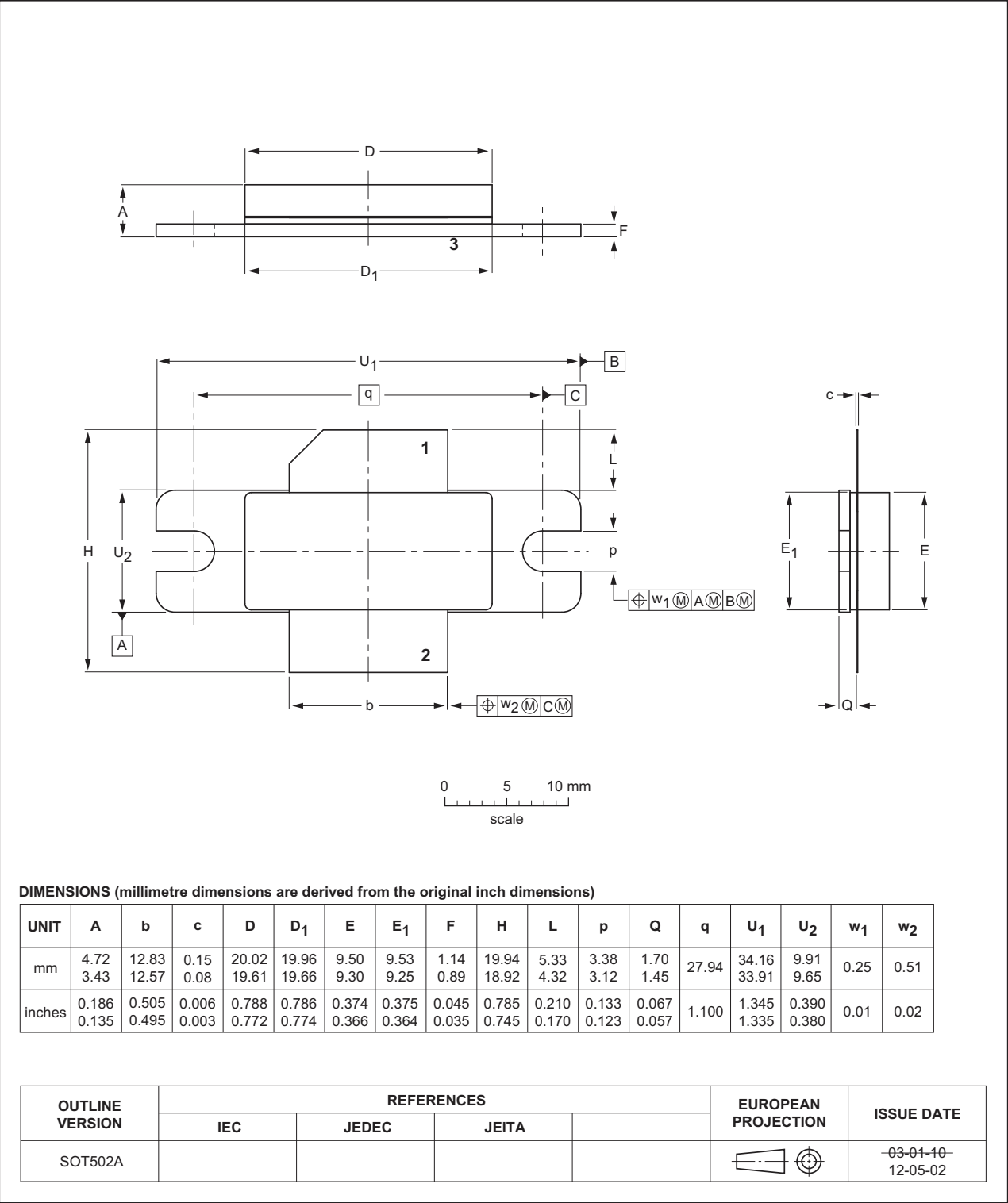


Fig 12. Package outline SOT502A

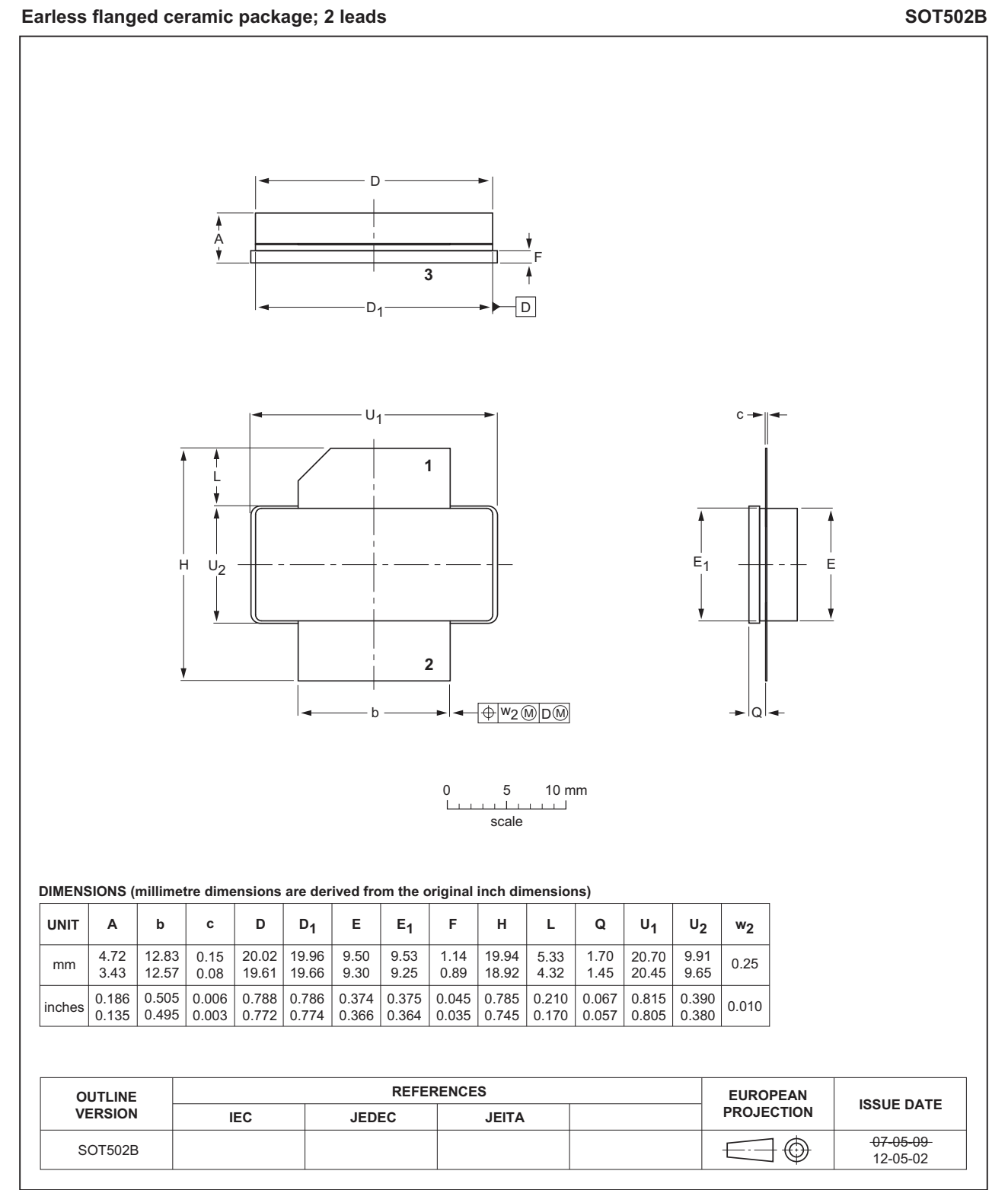


Fig 13. Package outline SOT502B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF7G22L-200_7G22LS-200#5	20150901	Product data sheet	-	BLF7G22L-200_7G22LS-200 v.4
Modifications:	- The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. - Legal texts have been adapted to the new company name where appropriate.			
BLF7G22L-200_7G22LS-200 v.4	20110722	Product data sheet	-	BLF7G22L-200_7G22LS-200 v.3
BLF7G22L-200_7G22LS-200 v.3	20110401	Preliminary data sheet	-	BLF7G22L-200_7G22LS-200 v.2
BLF7G22L-200_7G22LS-200 v.2	20101228	Preliminary data sheet	-	BLF7G22L-200_7G22LS-200 v.1
BLF7G22L-200_7G22LS-200 v.1	20100419	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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