ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number:	BLA9H0912L-700GU
Manufacturer:	Ampleon USA Inc.
Package:	Please confirm with sales
Availability:	Please confirm with sales

Product Page:

https://antrexco.com/product/details/ampleon-usa-inc/bla9h0912l-700gu.html

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

BLA9H0912L(S)-700; BLA9H0912L(S)-700G

Power LDMOS transistor

AMPLEON

Rev. 1 — 24 May 2019 **Product data sheet**

1. Product profile

1.1 General description

700 W LDMOS power transistor for avionics applications in the frequency range from 960 MHz to 1215 MHz.

Table 1. Typical information

Typical RF performance at T_{case} = 25 °C; t_p = 50 µs; δ = 2 %; I_{Dq} = 100 mA; in a class-AB demo circuit.

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	1030	50	700	20	62

1.2 Features and benefits

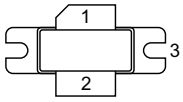
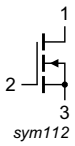
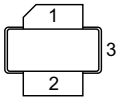
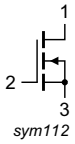
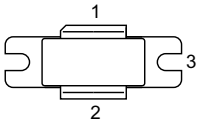
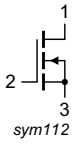
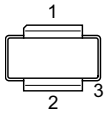
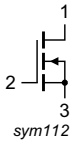
- High efficiency
- Excellent ruggedness
- Designed for avionics band operation
- Excellent thermal stability
- Easy power control
- Integrated dual sided ESD protection enables excellent off-state isolation
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Avionics transmitter applications in the frequency range from 960 MHz to 1215 MHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLA9H0912L-700 (SOT502A)			
1	drain		
2	gate		
3	source [1]		
BLA9H0912LS-700 (SOT502B)			
1	drain		
2	gate		
3	source [1]		
BLA9H0912L-700G (SOT502F)			
1	drain		
2	gate		
3	source [1]		
BLA9H0912LS-700G (SOT502E)			
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLA9H0912L-700	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLA9H0912LS-700	-	earless flanged ceramic package; 2 leads	SOT502B
BLA9H0912L-700G	-	eared flanged ceramic package; 2 leads; 2 mounting holes	SOT502F
BLA9H0912LS-700G	-	earless flanged ceramic package; 2 leads	SOT502E

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	106	V
V_{GS}	gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_{case} = 85 °C; P_L = 700 W		
		t_p = 32 μs; δ = 2 %	0.055	K/W
		t_p = 10 μs; δ = 10 %	0.068	K/W
		t_p = 64 μs; δ = 1 %	0.076	K/W
		t_p = 2.4 ms; δ = 6.4 %	0.24	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 4 mA	106	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 400 mA	1.5	2.0	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	60	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 400 mA	-	3.7	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 14 A	-	0.060	-	Ω

Table 7. RF characteristics

Test signal: pulsed RF; f = 1030 MHz; t_p = 50 μs; δ = 2 %; RF performance at V_{DS} = 50 V; I_{Dq} = 100 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 700 W	19	20	-	dB
η_D	drain efficiency	P_L = 700 W	59	62	-	%
RL_{in}	input return loss	P_L = 700 W	-	−15	-	dB
$P_{droop(pulse)}$	pulse droop power	P_L = 700 W	-	0.2	0.5	dB
$P_{L(2dB)}$	output power at 2 dB gain compression		-	725	-	W

7. Test information

7.1 Ruggedness in class-AB operation

The BLA9H0912L-700, BLA9H0912LS-700, BLA9H0912L-700G and BLA9H0912LS-700G are capable of withstanding a load mismatch corresponding to VSWR = 20 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 100 mA; P_L = 700 W; t_p = 50 μs; δ = 2 %.

7.2 Impedance information

Table 8. Typical impedance

Typical values unless otherwise specified.

f	Z_S	Z_L
(MHz)	(Ω)	(Ω)
950	0.717 – j1.793	0.965 – j1.305
1000	0.953 – j1.886	1.049 – j1.561
1050	1.091 – j1.910	1.032 – j1.780
1100	1.353 – j0.443	1.291 – j1.952
1150	1.962 – j1.061	1.474 – j2.081
1200	0.837 – j0.936	1.514 – j2.413

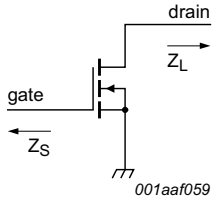
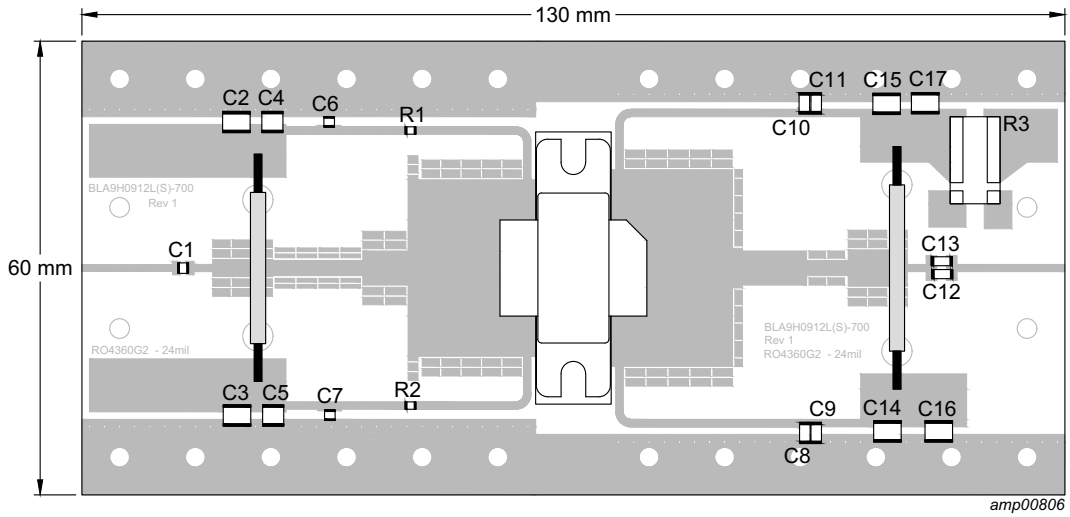


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers 4360G2; thickness = 0.61 mm; ε_r = 6.15; thickness copper plating = 35 μm.

See Table 9 for a list of components.

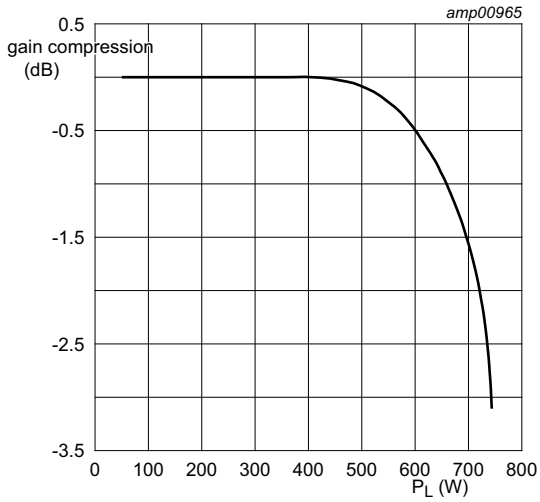
Fig 2. Component layout for class-AB production test circuit

Table 9. Demo test circuit list of components

See Figure 2 for component layout.

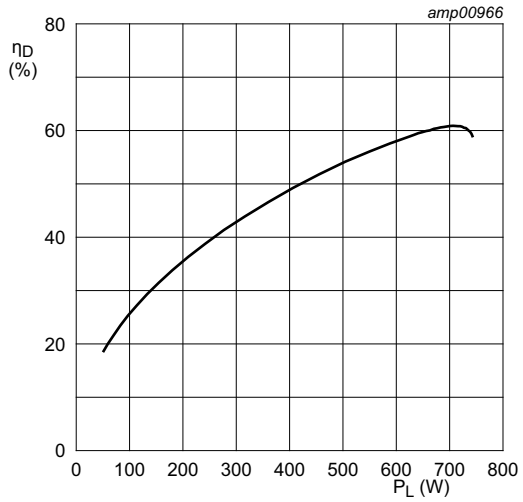
Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	62 pF	ATC 100A
C2, C3, C16, C17	multilayer ceramic chip capacitor	4.7 μF, 100 V	GMR42 258K7S 475K 100 H53
C4, C5, C14, C15	multilayer ceramic chip capacitor	1 nF	ATC 100B
C6, C7	multilayer ceramic chip capacitor	200 pF	ATC 800B
C8, C9, C10, C11, C12, C13	multilayer ceramic chip capacitor	68 pF	ATC 800B
R1, R2	resistor	5.1 kΩ	SMD 0603
R3	resistor	10 mΩ	FC4L110R010FER

7.4 Graphical data



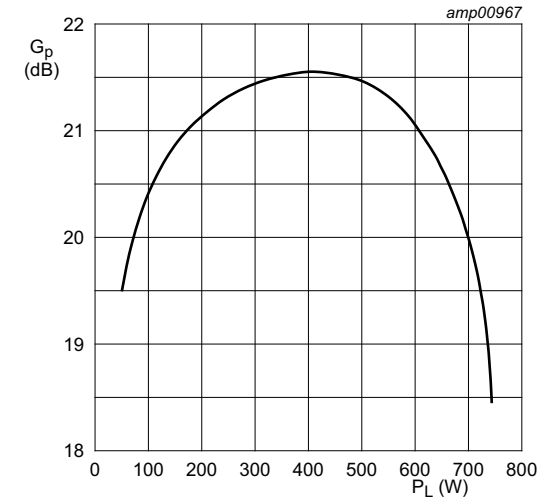
V_{DS} = 50 V; I_{Dq} = 100 mA; f = 1030 MHz; t_p = 50 μs; δ = 2 %.

Fig 3. Gain compression as a function of output power; typical values



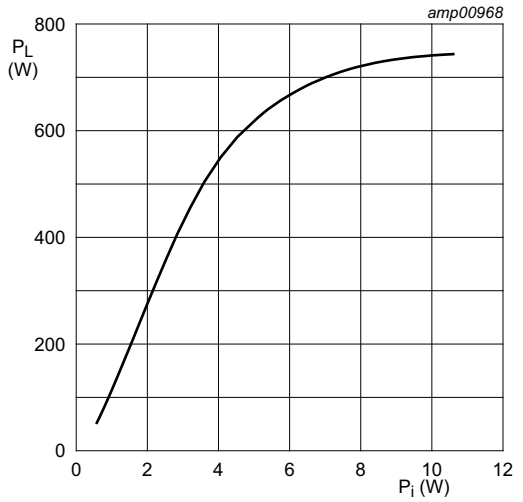
V_{DS} = 50 V; I_{Dq} = 100 mA; f = 1030 MHz; t_p = 50 μs; δ = 2 %.

Fig 4. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 100 mA; f = 1030 MHz; t_p = 50 μs; δ = 2 %.

Fig 5. Power gain as a function of output power; typical values

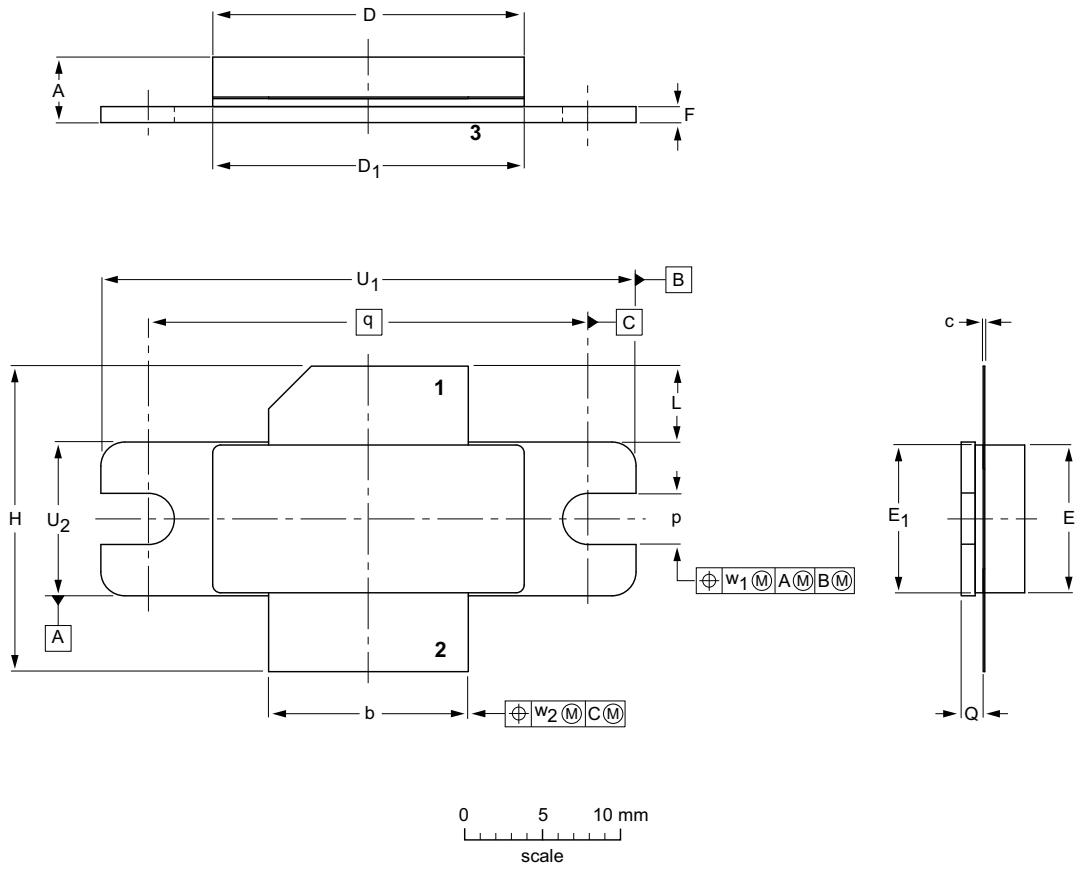


V_{DS} = 50 V; I_{Dq} = 100 mA; f = 1030 MHz; t_p = 50 μs; δ = 2 %.

Fig 6. Output power as a function of input power; typical values

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT502A**



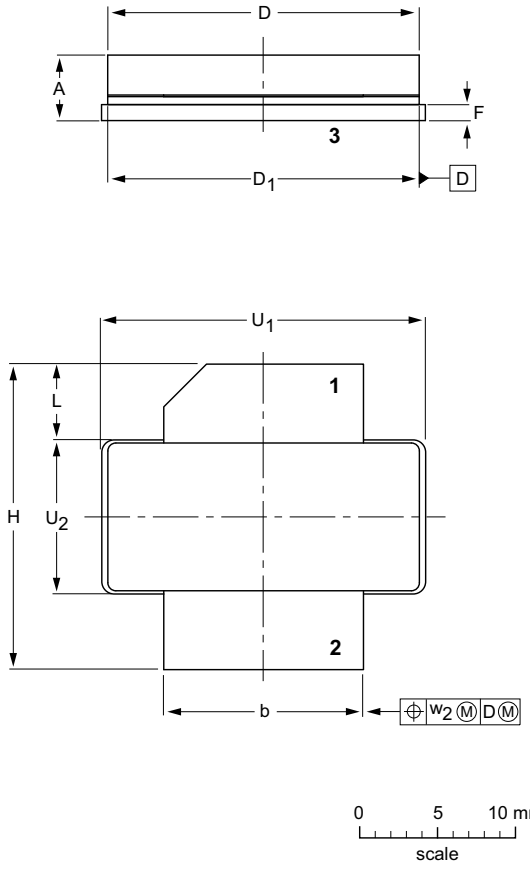
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~03-01-10~~ 12-05-02

Fig 7. Package outline SOT502A

Earless flanged ceramic package; 2 leads **SOT502B**



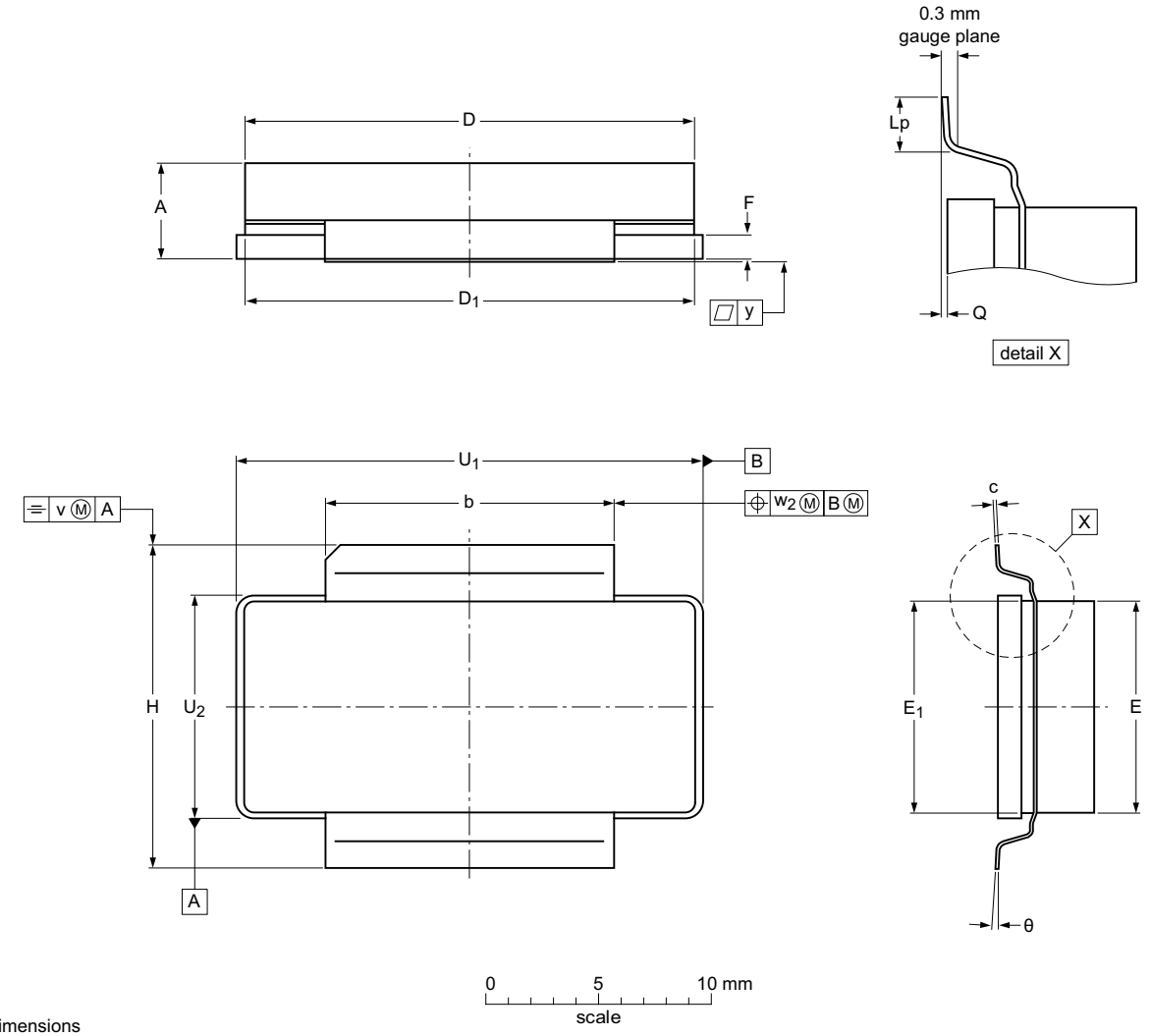
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~07-05-09~~ 12-05-02

Fig 8. Package outline SOT502B

Earless flanged ceramic package; 2 leads **SOT502E**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	F	H	L_p	Q	U_1	U_2	v	w_2	y	θ
mm	max	4.72	12.83	0.15	20.02	19.96	9.53	9.53	1.14	14.3	1.38	0.195	20.70	9.91	0.25	0.25	0.15	7°
	nom																	
	min	3.43	12.57	0.07	19.61	19.66	9.27	9.27	0.89	14.1	0.98	0.055	20.45	9.65				0°
inches	max	0.185	0.505	0.006	0.788	0.786	0.375	0.375	0.045	0.563	0.055	0.008	0.815	0.390	0.010	0.010	0.006	7°
	nom																	
	min	0.135	0.495	0.003	0.772	0.774	0.365	0.365	0.035	0.555	0.039	0.002	0.805	0.380				0°

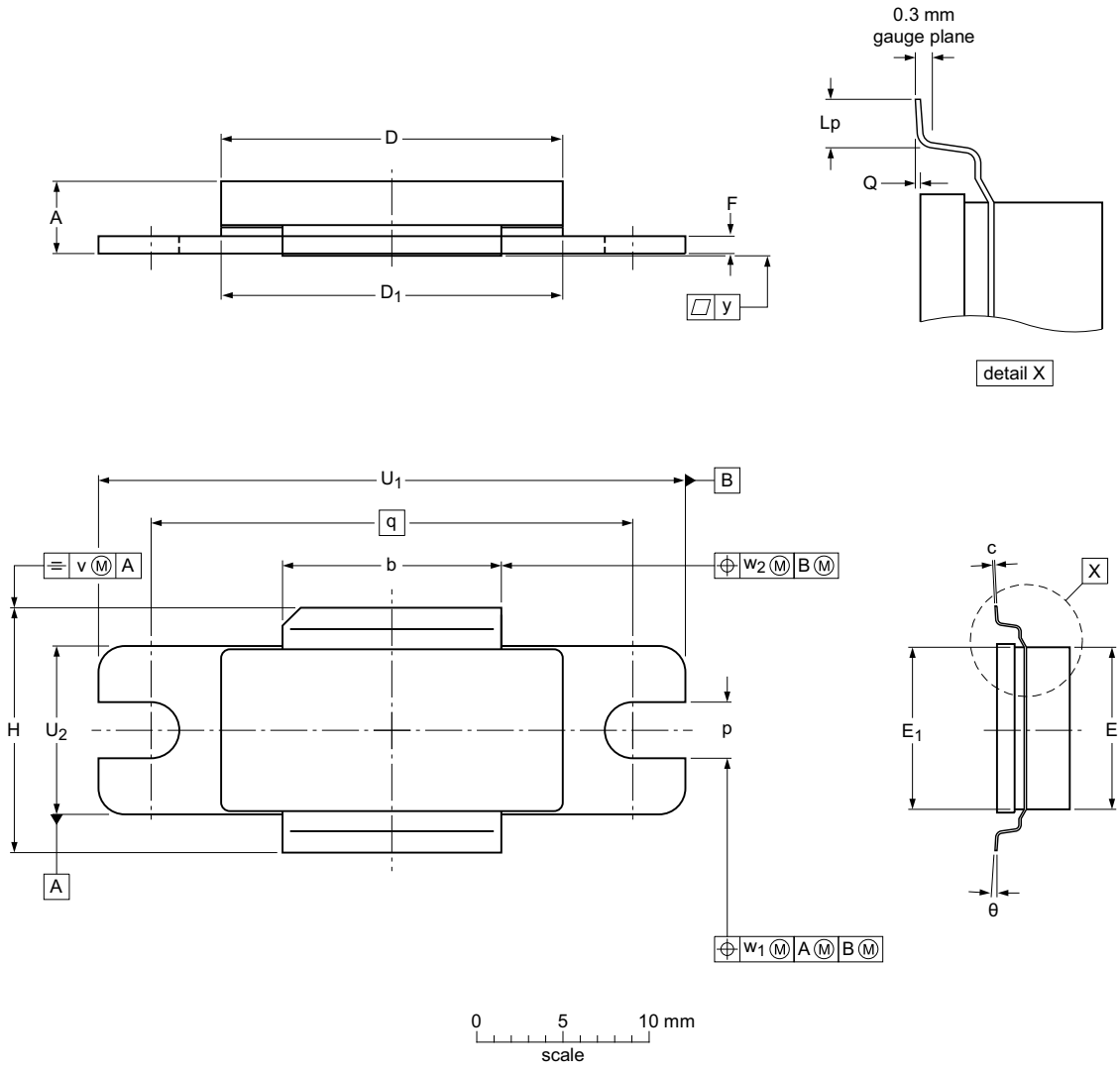
Note
1. Millimeter dimensions are derived from the original inch dimensions.

sot502e_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT502E						~~12-05-14~~ 12-05-30

Fig 9. Package outline SOT502E

Eared flanged ceramic package; 2 leads; 2 mounting holes **SOT502F**



Dimensions (mm are the original dimensions)

Unit[1]		A	b	c	D	D_1	E	E_1	F	H	L_p	p	Q	q	U_1	U_2	v	w_1	w_2	θ	U1
mm	max	4.70	12.83	0.15	20.02	19.96	9.53	9.53	1.14	14.3	1.38	3.38	0.195		34.16	9.91				7°	
	nom													27.94			0.25	0.25	0.25		0.15
	min	3.43	12.57	0.07	19.61	19.66	9.27	9.27	0.89	14.1	0.98	3.12	0.055		33.91	9.65				0°	

sot502f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT502F						~~14-02-19~~ 14-03-14

Fig 10. Package outline SOT502F

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA9H0912L-700_LS-700_L-700G_LS-700G v.1	20190524	Product data sheet		-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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13. Contact information

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