

ANTREX Electronics

Electronic Components Sourcing Information

Product Reference Information

Part Number: AO4616L_102

Manufacturer: Alpha & Omega Semiconductor Inc.

Package: Please confirm with sales

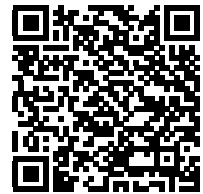
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Product Page:

<https://antrexco.com/product/details/alpha-omega-semiconductor-inc/ao4616l-102.html>

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Note:

This PDF includes an ANTREX product reference cover page.

The original manufacturer datasheet follows from the next page.

General Description

The AO4616 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This complementary N and P channel MOSFET configuration is ideal for low Input Voltage inverter applications.

Product Summary

N-Channel

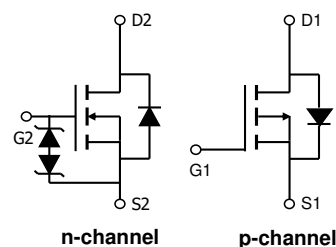
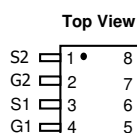
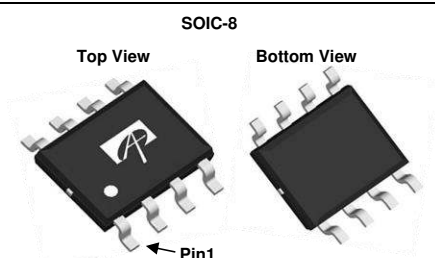
$V_{DS} = 30V$
 $I_D = 8A$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 20m\Omega$ ($V_{GS} = 10V$)
 $< 28m\Omega$ ($V_{GS} = 4.5V$)

100% UIS Tested
100% R_g Tested
ESD Protected

P-Channel

$-30V$
 $-7A$ ($V_{GS} = -10V$)
 $R_{DS(ON)} < 22m\Omega$ ($V_{GS} = -10V$)
 $< 40m\Omega$ ($V_{GS} = -4.5V$)

100% UIS Tested
100% R_g Tested



Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current $T_A = 25^\circ C$	I_D	8	-7	A
$T_A = 70^\circ C$		6.5	-6	
Pulsed Drain Current ^C	I_{DM}	40	-40	A
Avalanche Current ^C	I_{AS}, I_{AR}	19	27	A
Avalanche energy $L = 0.1mH$ ^C	E_{AS}, E_{AR}	18	36	mJ
Power Dissipation ^B $T_A = 25^\circ C$	P_D	2	2	W
$T_A = 70^\circ C$		1.3	1.3	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A $t \leq 10s$	$R_{\theta JA}$	48	62.5	$^\circ C/W$
Maximum Junction-to-Ambient ^{A D} Steady-State		74	90	$^\circ C/W$
Maximum Junction-to-Lead Steady-State	$R_{\theta JL}$	32	40	$^\circ C/W$

N-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±16V			10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.2	1.8	2.4	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	40			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =8A T _J =125°C		16.5 23	20 28	mΩ
		V _{GS} =4.5V, I _D =6A		19.5	28	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =8A		30		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.75	1	V
I _S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz	600	740	888	pF
C _{oss}	Output Capacitance		77	110	145	pF
C _{rss}	Reverse Transfer Capacitance		50	82	115	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.5	1.1	1.7	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =8A	12	15	18	nC
Q _{g(4.5V)}	Total Gate Charge		6	7.5	9	nC
Q _{gs}	Gate Source Charge			2.5		nC
Q _{gd}	Gate Drain Charge			3		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =1.8Ω, R _{GEN} =3Ω		5		ns
t _r	Turn-On Rise Time			3.5		ns
t _{D(off)}	Turn-Off DelayTime			19		ns
t _f	Turn-Off Fall Time			3.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =8A, dI/dt=500A/μs	6	8	10	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =8A, dI/dt=500A/μs	14	18	22	nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

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N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

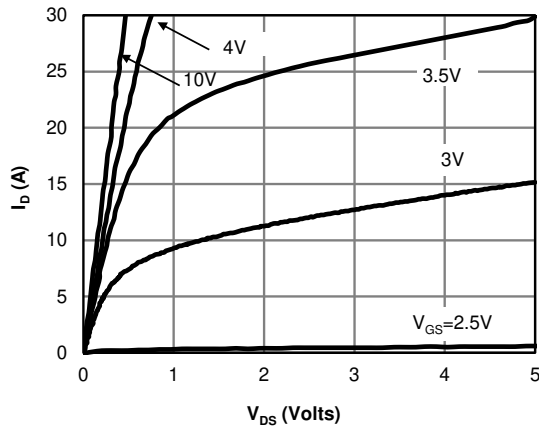


Fig 1: On-Region Characteristics (Note E)

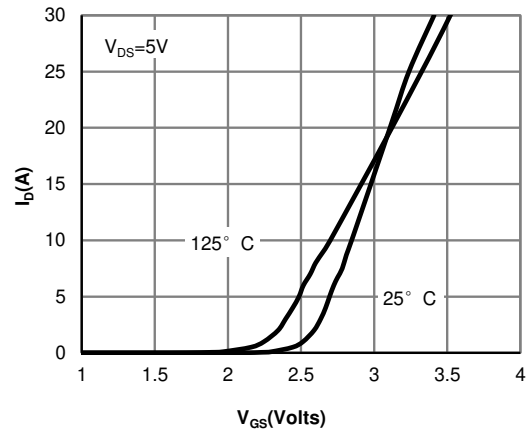


Figure 2: Transfer Characteristics (Note E)

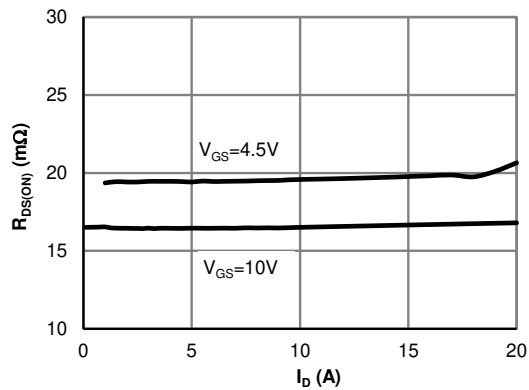


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

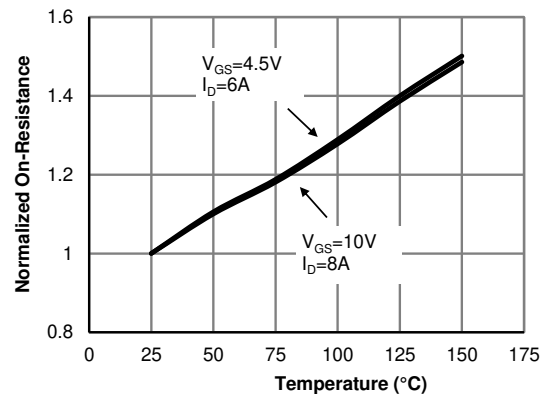


Figure 4: On-Resistance vs. Junction Temperature (Note E)

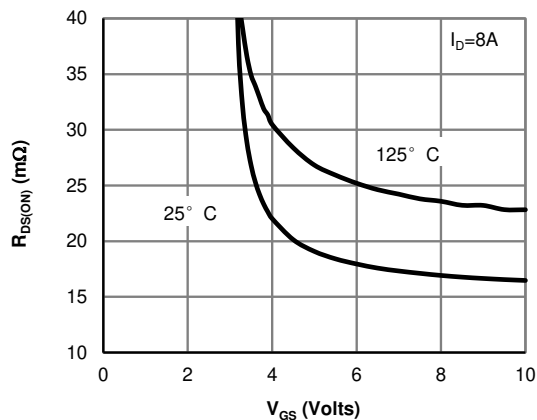


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

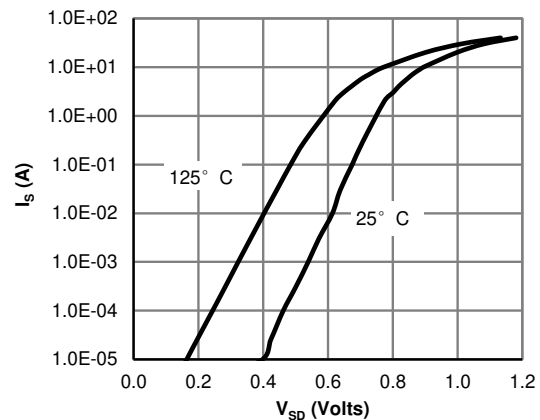


Figure 6: Body-Diode Characteristics (Note E)

N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

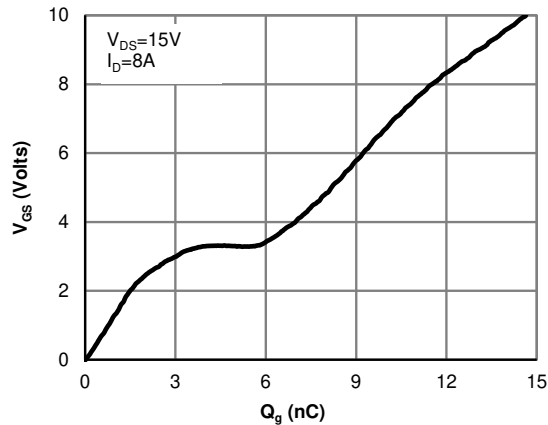


Figure 7: Gate-Charge Characteristics

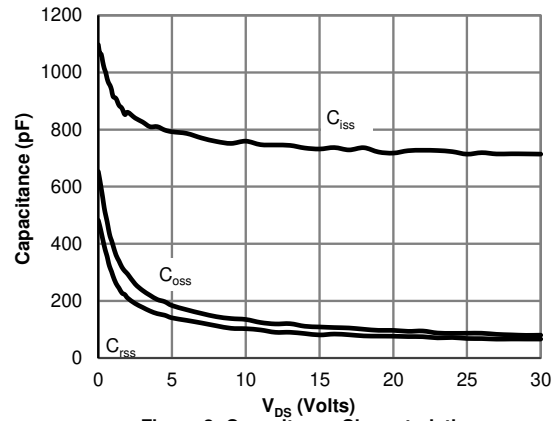


Figure 8: Capacitance Characteristics

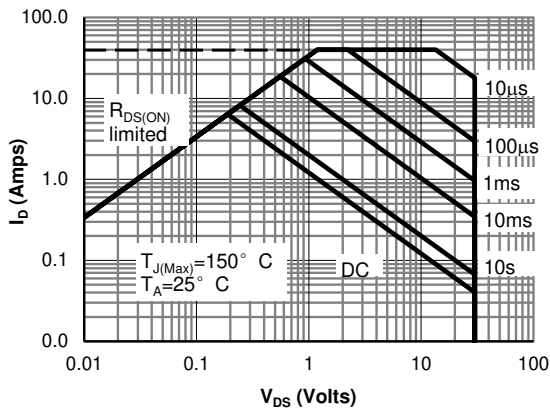


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

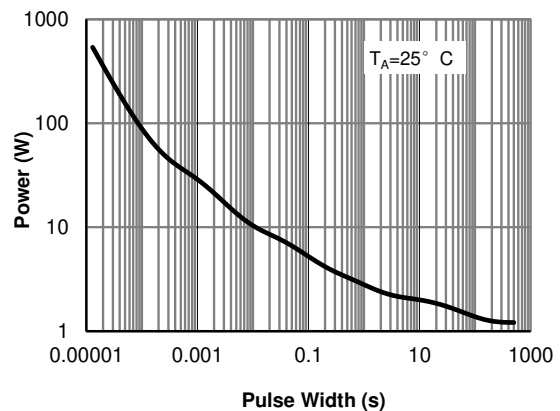


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

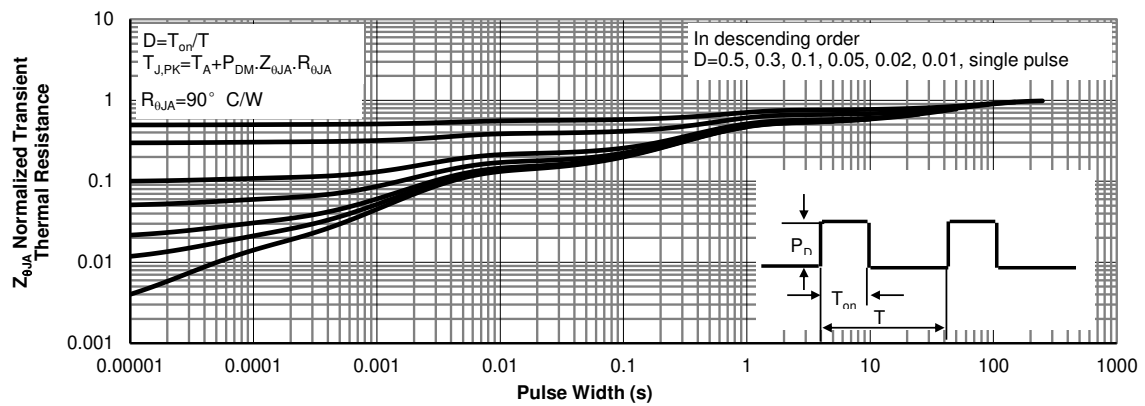
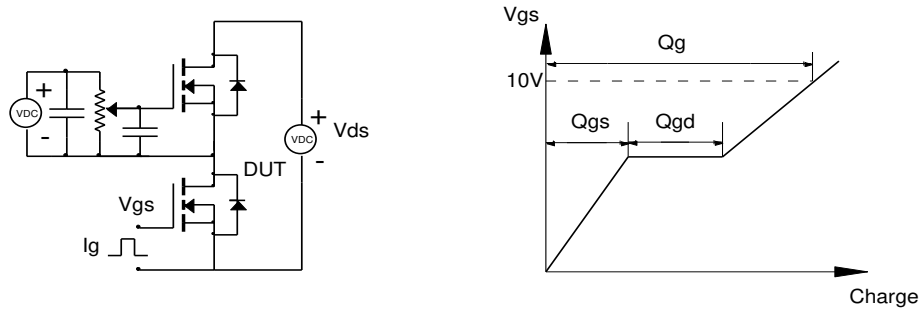
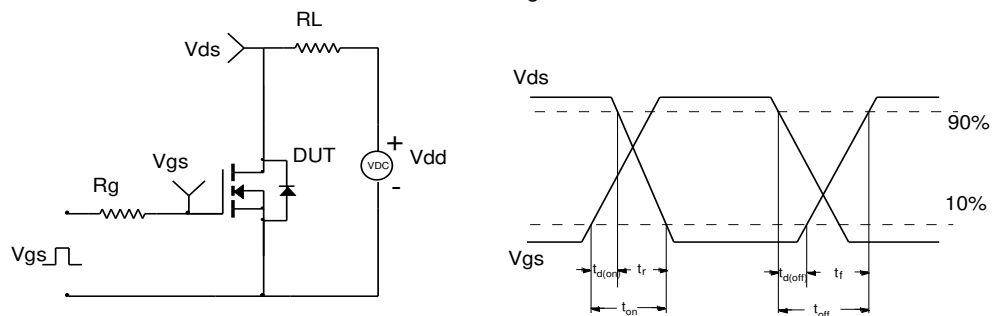


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

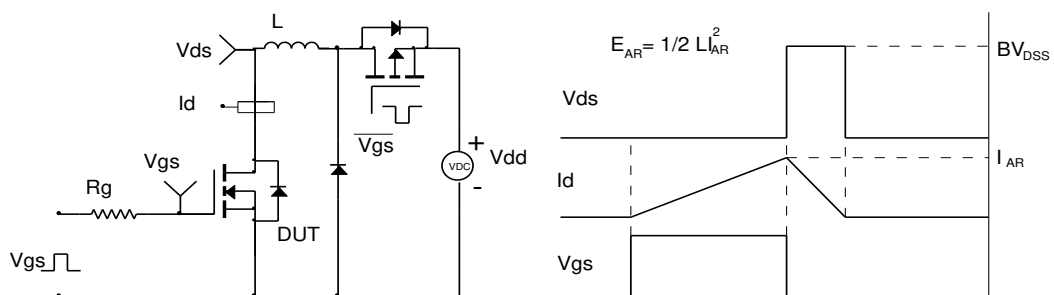
Gate Charge Test Circuit & Waveform



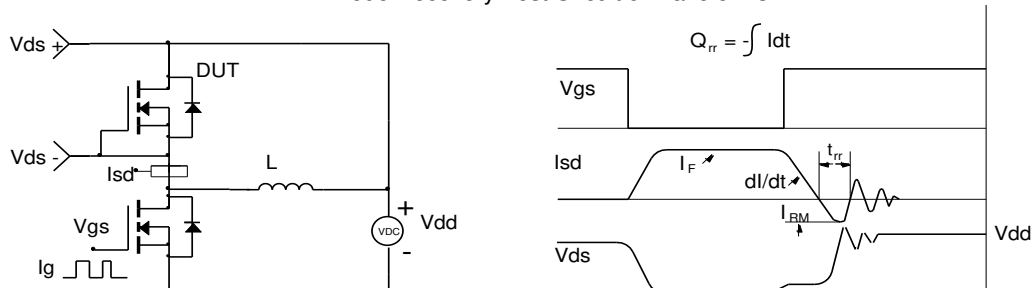
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-30\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1.4	-2.0	-2.5	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}$, $V_{DS}=-5\text{V}$	-40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$, $I_D=-7\text{A}$ $T_J=125^\circ\text{C}$		17.5 24.5	22 33	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}$, $I_D=-3.5\text{A}$		27.5	40	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-7\text{A}$		24		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$		-0.75	-1	V
I_S	Maximum Body-Diode Continuous Current				-2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-15\text{V}$, $f=1\text{MHz}$	830	1040	1250	pF
C_{oss}	Output Capacitance		125	180	235	pF
C_{rss}	Reverse Transfer Capacitance		75	125	175	pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$	2	4	6	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=-15\text{V}$, $I_D=-7\text{A}$	15	19	23	nC
$Q_g(4.5\text{V})$	Total Gate Charge		7.5	9.6	12	nC
Q_{gs}	Gate Source Charge			3.6		nC
Q_{gd}	Gate Drain Charge			4.6		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=-15\text{V}$, $R_L=2.2\Omega$, $R_{GEN}=3\Omega$		10		ns
t_r	Turn-On Rise Time			5.5		ns
$t_{D(off)}$	Turn-Off DelayTime			26		ns
t_f	Turn-Off Fall Time			9		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-7\text{A}$, $dI/dt=500\text{A}/\mu\text{s}$		11.5	15	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-7\text{A}$, $dI/dt=500\text{A}/\mu\text{s}$		25	32.5	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using $\leq 10\text{s}$ junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}=150^\circ\text{C}$. The SOA curve provides a single pulse rating.

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P-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

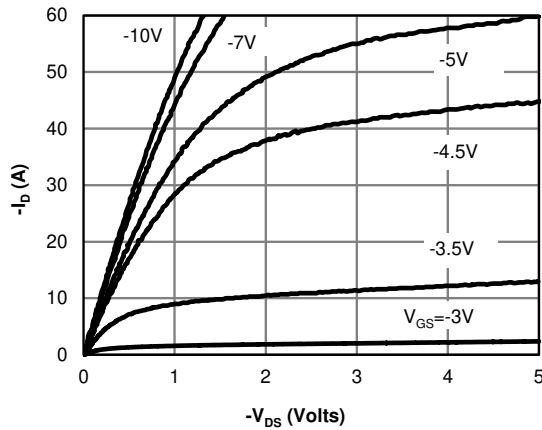


Fig 1: On-Region Characteristics (Note E)

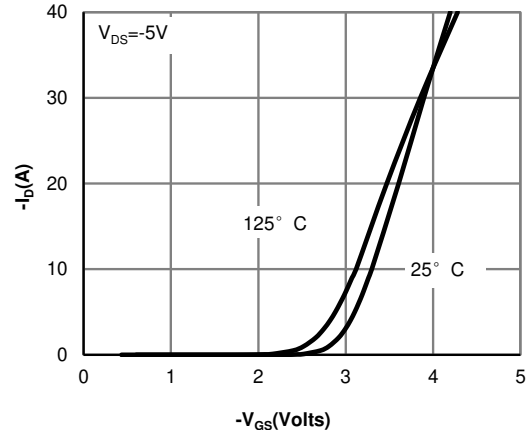


Figure 2: Transfer Characteristics (Note E)

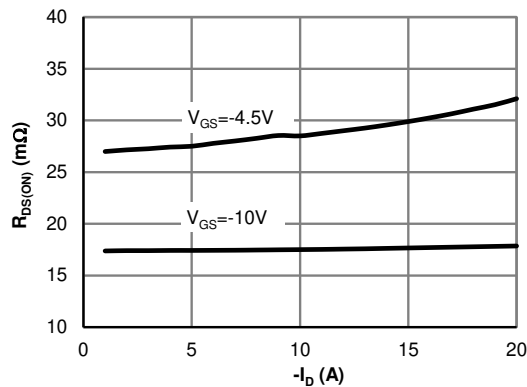


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

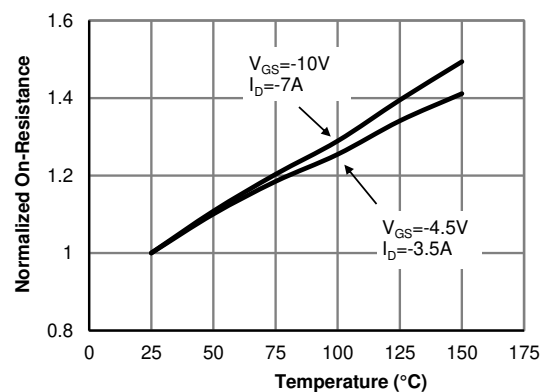


Figure 4: On-Resistance vs. Junction Temperature (Note E)

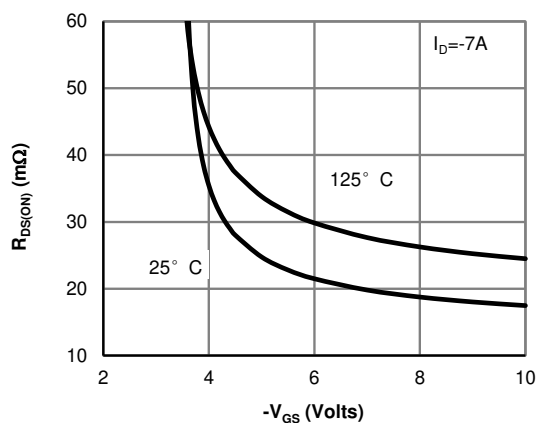


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

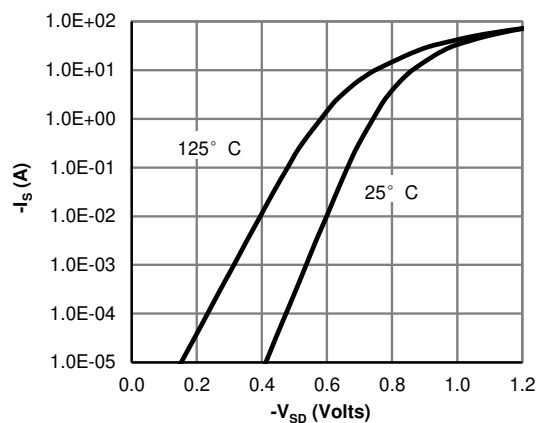


Figure 6: Body-Diode Characteristics (Note E)

P-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

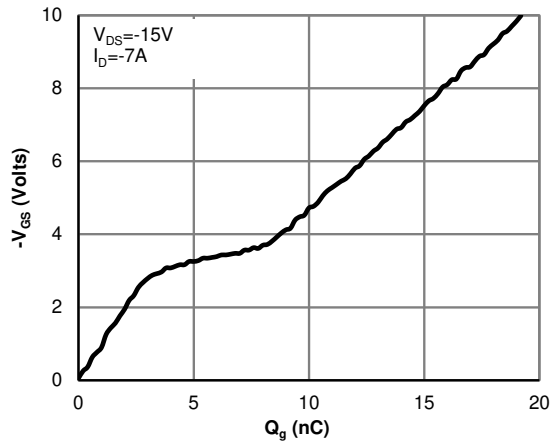


Figure 7: Gate-Charge Characteristics

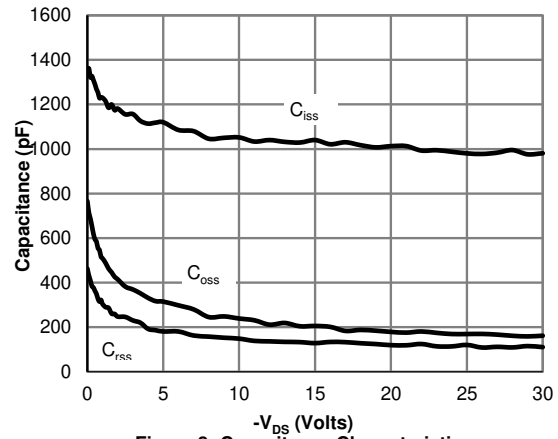


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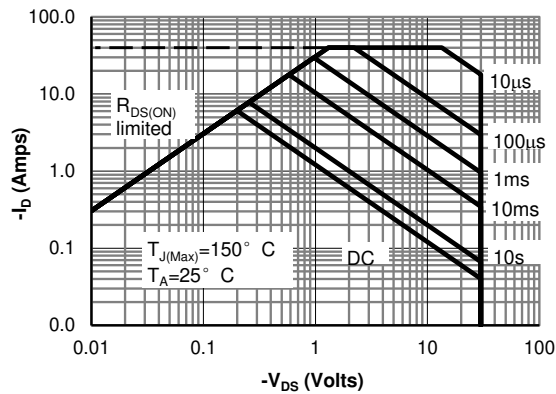


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

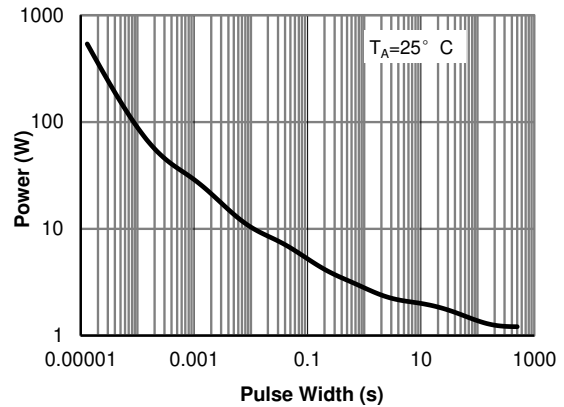


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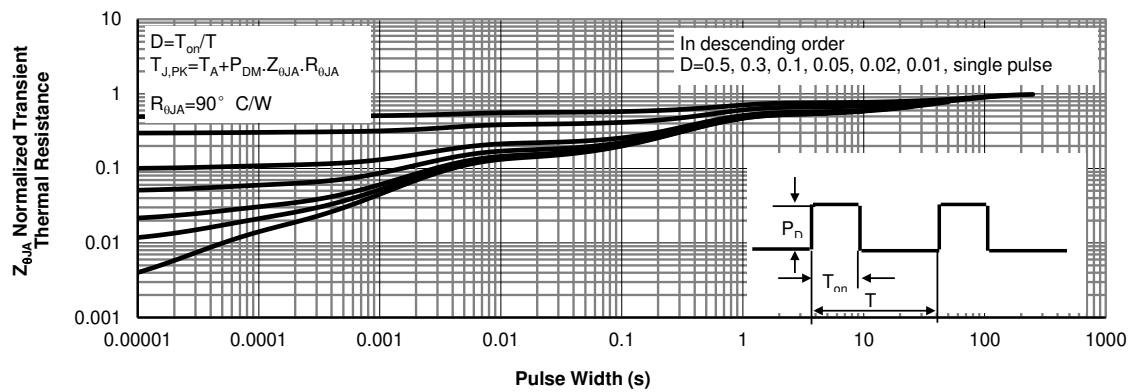
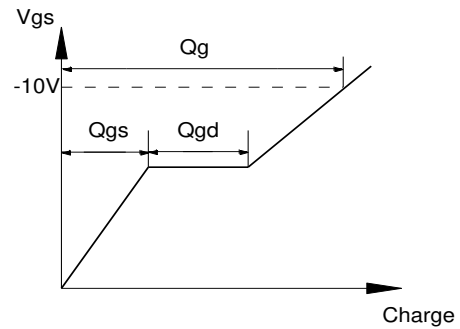
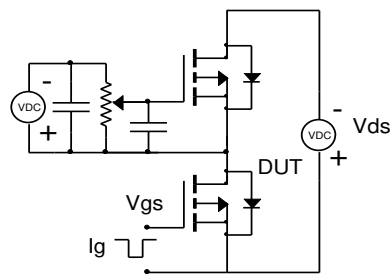
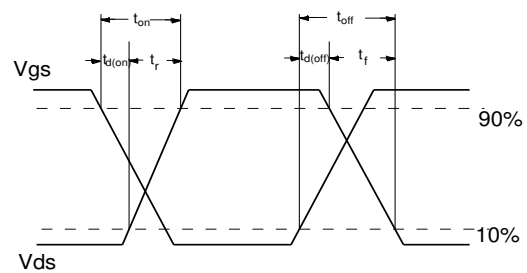
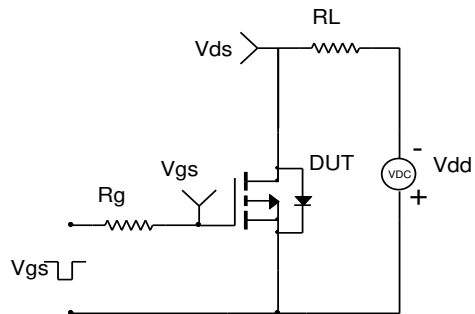


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

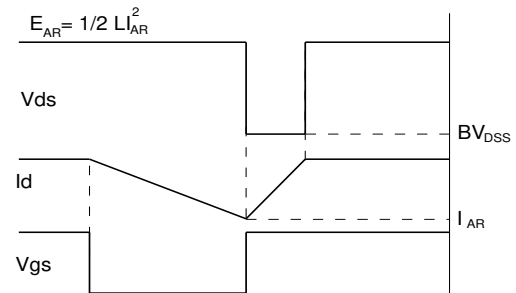
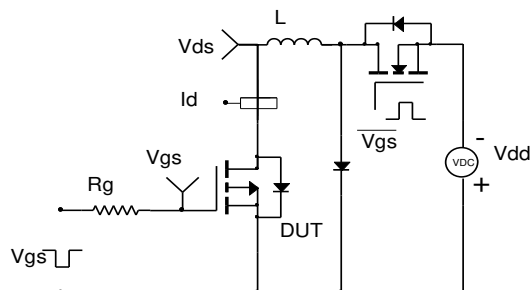
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

